CRETE SEMICONDUCTORS

RF & Microwave Power Transistors and RF Power Modules

Data Handbook SC19
2000

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RF & Microwave Power Transistors and RF Power Modules

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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RF & Microwave Power Transistors and RF Power Modules

PREFACE

Thank you for your interest in Philips Semiconductors RF power transistors & modules and microwave transistors.

This databook lists many new and exciting products for microwave, broadcast & cellular base station applications. For these applications Philips offers advanced bipolar, standard MOS as well as highly linear LDMOS transistors for effective solutions in cellular communication for the 1 GHz and 2 GHz band. Complete amplifier modules are available for high-performance and low cost solutions to enable quick and reliable system design.

In addition a broad range of transmitting transistors for the more traditional radio and TV applications from HF to UHF, and transistors for L- and S-band radars are available.

Stay up-to-date

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SELECTION GUIDES

RF POWER TRANSISTORS FOR HF AND VHF

1.6 to 30 MHz Bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER P_L (PEP) (W)	POWER GAIN G_p (dB)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-A intermodulation distortion: d_3, $d_5 < -40$ dB					
BLV10	SOT123A	1	18	12	506
BLY87C	SOT120A	1	18	12	911
BLV11	SOT123A	2	18	13.5	514
BLW87	SOT123A	6	18	13.5	866
BLV20	SOT123A	1.3	20	26	522
BLV21	SOT123A	2.5	20	26	530
BLW83	SOT123A	10	20	26	834
BLW86	SOT123A	17	22	26	854
BLW96	SOT121B	50	19	40	874
BLW50F	SOT123A	16	19.5	45	799

1.6 to 30 MHz Bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER P_L (PEP) (W)	POWER GAIN G_p (dB)	EFFICIENCY (SSB) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-AB intermodulation distortion d_3, $d_5 < -30$ dB						
BLW85	SOT123A	30	19.5	30	12.5	842
BLV11	SOT123A	10	18	–	13.5	514
BLW87	SOT123A	15	18	–	13.5	866
BLV21	SOT123A	10	20	–	28	530
BLW83	SOT123A	25	20	40	28	834
BLW86	SOT123A	42.5	19	45	28	854
BLW76	SOT121B	80	13	>35	28	808
BLW77	SOT121B	130	12	>37.5	28	820
BLW97	SOT121B	175	11.5	>40	28	885
BLW50F	SOT123A	65	18	45	50	799
BLW96	SOT121B	200	13.5	>40	50	874

1.6 to 30 MHz MOS RF power transistors

TYPE NUMBER	PACKAGE	P_L (PEP) (W)	V_{DS} (V)	G_p (dB)	EFFICIENCY (SSB) (%)	PAGE
HF SSB class-AB (28 MHz, d3, d5 < −30 dB, 28 V & 50 V supply)						
BLF145	SOT123A	30	28	typ. 20	40	109
BLF246	SOT121B	80	28	typ. 20	–	199
BLF246B	SOT161A	60	28	>14	–	208
BLF147	SOT121B	150	28	17	>35	118
BLF175	SOT123A	30	50	23	40	127
BLF177	SOT121B	150	50	20	>35	142
HF SSB class-A (1.6 to 30 MHz, d3, d5 < −40 dB, 28 V & 50 V supply)						
BLF242	SOT123A	2	28	typ. 23	–	164
BLF244	SOT123A	4	28	typ. 23	–	172
BLF145	SOT123A	8	28	24	–	109
BLF246	SOT121B	20	28	typ. 23	–	199
BLF175	SOT123A	8	50	>24	–	127

25 to 175 MHz bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER @ 175 MHZ (W)	POWER GAIN @ 175 MHZ (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-B; 12 to 13.5 V supply voltage (car mobile)						
BLW85	SOT123A	45	4.5	>75	12.5	842
BLV10	SOT123A	8	9	>70	13.5	506
BLY87C	SOT120A	8	12	>60	13.5	911
BLV11	SOT123A	15	8	>60	13.5	514
BLW87	SOT123A	25	6	>70	13.5	866
Class-B; 28 V base stations						
BLV20	SOT123A	8	12	>65	28	522
BLV21	SOT123A	15	10	>65	28	530
BLW86	SOT123A	45	7.5	>70	28	854
BLW77(1)	SOT121B	130	7.5	75	28	820

Note

1. Load power and power gain measured at 87.5 MHz.

25 to 175 MHz MOS RF transistors

TYPE NUMBER	PACKAGE	P_L (W)	V_{DS} (V)	f (MHz)	G_p (dB)	EFFICIENCY (CW) (%)	PAGE
VHF base stations (Class-B operation, 28 V & 50 V supply)							
BLF242	SOT123A	5	28	175	13	60	164
BLF244	SOT123A	15	28	175	13	65	172
BLF245	SOT123A	30	28	175	13	67	181
BLF245B	SOT279A	30	28	175	14	65	190
BLF246	SOT121B	80	28	108	16	55	199
BLF147	SOT121B	150	28	108	typ. 14	70	118
BLF248	SOT262A	300	28	175	typ. 13	67	217
BLF175	SOT123A	30	50	108	typ. 20	65	127
BLF177	SOT121B	150	50	108	typ. 19	70	142
BLF277	SOT119A	150	50	175	14	58	227
BLF278	SOT262A	300	50	108	20	70	237
VHF mobile transmitters (Class-B operation, 12.5 V supply)							
BLF244	SOT123A	6	12.5	175	typ. 15	60	172
BLF245	SOT123A	12	12.5	175	typ. 12	66	181

87 to 108 MHz FM broadcast bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER @ 108 MHZ (W)	POWER GAIN @ 108 MHZ (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-B						
BLV21	SOT123A	15	10	>65	28	530
BLW86(1)	SOT123A	45	7.5	>70	28	854
BLW76	SOT121B	80	8	70	28	808
BLV25	SOT119A	175	10	70	28	538

Note

1. Load power and power gain measured at 175 MHz.

Bipolar RF power transistors for TV transposers and transmitters

TYPE NUMBER	PACKAGE	OUTPUT POWER $P_{o\ sync}$ (W)	d_{im} (dB)	LOAD POWER (W)	POWER GAIN @ 860 MHZ (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-A bands I (41 to 68 MHz) & III (174 to 230 MHz)								
BLV33F	SOT119A	22	–55	–	14.8	–	25	560
BLV33	SOT147A	26	–55	–	9.7	–	25	546
Class-AB bands I (41 to 68 MHz) & III (174 to 230 MHz)								
BLV33F	SOT119A	–	–	85	10.5	71	28	560
BLV33	SOT147A	–	–	90	6.5	72	28	546
Class-A bands IV & V 470 to 860 MHz								
BLW32	SOT122A	0.63	–60	–	11	–	25	772
BLW33	SOT122A	1.15	–60	–	10	–	25	781
BLW34	SOT122A	2.15	–60	–	9	–	25	790
BLW898	SOT171A	3	–60	–	8.5	–	25	903
BLW98	SOT122A	4.4	–60	–	6.5	–	25	893
BLV857	SOT324B	10	–51	–	>10	–	25	645
BLV57	SOT161A	12	–60	–	9	–	25	575
BLV859	SOT262B	20	–51	–	10	–	25	654
BLV58	SOT289A	25	–45	–	10	–	25	594
Class-AB bands IV & V 470 to 860 MHz								
BLV59	SOT171A	–	–	30	7	55	25	604
BLV57	SOT161A	–	–	38	7	55	25	575
BLV861	SOT289A	–	–	100	8.5	55	28	663
BLV862	SOT262B	–	–	150	9	52	28	671

LDMOS transistors for TV transmitters

TYPE NUMBER	PACKAGE	P_L (W)	V_{DS} (V)	f (MHz)	G_p (dB)	EFFICIENCY (CW) (%)	PAGE
Class-AB bands IV & V 470 to 860 MHz							
BLF861	SOT540A	150	32	860	>14	>50	383

MOS RF power transistors for TV transposers and transmitters

TYPE NUMBER	PACKAGE	$P_{o\ sync}$ (W)	V_{DS} (V)	f (MHz)	G_p (dB)	d_{im} (dB)	I_D (mA)	EFFICIENCY (CW) (%)	PAGE
TV transposers Class-A band III (174 to 230 MHz)									
BLF346	SOT119A	25(1)	28	225	14	−52	3000	–	255
BLF348	SOT262A	67(1)	28	225	11	−52	2 × 4600	–	264
TV transmitters Class-AB band III (174 to 230 MHz)									
BLF248	SOT262A	300	28	225	10	–	2 × 250	65	217
BLF368	SOT262A	300(2)	32	225	12	–	2 × 250	62	273
BLF378	SOT262A	250(2)	50	225	14	–	2 × 500	55	284
BLF278	SOT262A	250	50	225	14	–	2 × 500	55	237

Notes

1. Typical value at heatsink temperature of 70 °C.
2. At 1 dB power gain compression.

RF POWER TRANSISTORS AND BASE STATION HYBRID AMPLIFIERS

100 to 960 MHz MOS RF power transistors

TYPE NUMBER	PACKAGE	P_L (W)	V_{DS} (V)	f (MHz)	G_P (dB)	EFFICIENCY (CW) (%)	PAGE
UHF base stations, Class-B (225 to 400 MHz)							
BLF242	SOT123A	5	28	400	typ. 13	60	164
BLF244	SOT123A	15	28	400	typ. 11	65	172
BLF245	SOT123A	30	28	400	typ. 10	67	181
UHF base stations, Class-B (100 to 500 MHz)							
BLF202	SOT409A	2	12.5	175	10	>50	155
BLF521	SOT172D	2	12.5	500	10	60	305
BLF404	SOT409A	4	12.5	500	10	50	295
BLF542	SOT171A	5	28	500	10	59	316
BLF543	SOT171A	10	28	500	12	60	325
BLF544	SOT171A	20	28	500	11	60	336
BLF545	SOT268A	40	28	500	11	60	347
BLF546	SOT268A	80	28	500	11	60	356
BLF547	SOT262A	100	28	500	10	55	365
BLF548	SOT262A	150	28	500	9	55	374

400 to 512 MHz bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER @ 470 MHz (W)	POWER GAIN @ 470 MHz (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-B 7.5 V supply; portable mobile						
BLT53	SOT122D	8	6	65	7.5	478
Class-B 12.5 V supply; car mobile						
BLU99/SL	SOT122D	5	10.5	66	12.5	493
BLU30/12	SOT119A	30	6	66	12.5	486

900 MHz bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER @ 900 MHz (W)	POWER GAIN @ 900 MHz (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-B 12.5 V car mobile						
BLU99/SL	SOT122D	4	7	60	12.5	493
BLV193	SOT171A	12	6.5	60	12.5	626
BLV194	SOT171A	16	6	57	12.5	637

900 to 960 MHz bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER @ 900 MHz (W)	POWER GAIN @ 900 MHz (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-AB and class-B 24 to 26 V base stations						
BLV99/SL	SOT172D	2	8	63 (class-B)	24	612
BLV103	SOT171A	4(1)	11.5	48	24	619
BLV904	SOT409B	5(1)	11	>50	26	679
BLV909	SOT409B	9(1)	9	57	26	688
BLV910	SOT171A	10(1)	11	>55	26	697
BLV920	SOT171A	20(1)	10	>55	26	705
BLV946	SOT273A	40(1)	9	60	26	713
BLV958	SOT391A	75(1)	8.5	55	26	731
BLV958FL	SOT391B	75(1)	8.5	55	26	731
UHF base stations, Class-B (860 to 960 MHz)						
BLF543	SOT171A	10(1)	typ . 8	50	28	325
BLF544	SOT171A	20(1)	typ. 7	50	28	336

Note

1. Load power and power gain measured at 960 MHz.

900 to 960 MHz LDMOS RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER @ 900 MHz (W)	POWER GAIN @ 900 MHz (dB)	d_{im} (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{DS} (V)	PAGE
Class-AB 26 V base stations							
BLF1043	SOT538A	10	>16	≥–30	>45	26	392
BLF1046	SOT467A	45	>14	≤–28	>45	26	396
BLF1047	SOT541A	70	>14	≤–26	>45	26	398
BLF1048	SOT502A	90	>14	≤–26	>45	26	400

1800 to 2000 MHz bipolar RF power transistors

TYPE NUMBER	PACKAGE	LOAD POWER @ 1950 MHz (W)	POWER GAIN @ 1950 MHz (dB)	EFFICIENCY (CW) (%)	SUPPLY VOLTAGE V_{CE} (V)	PAGE
Class-AB 26 V base stations						
LBE2009S	SOT441A	>0.7	8	–	26	919
BLV2042	SOT409B	4	8	45	26	739
LVE21050R	SOT445A	5.5	8	–	26	944
BLV2044	SOT437A	15	8	45	26	748
BLV2045N	SOT390A	30	≥10	≥40	26	757
BLV2047	SOT468A	60	8.5	40	26	764

1800 to 2210 MHz LDMOS RF power transistors

TYPE NUMBER	PACKAGE	P_L (W)	V_{CE} (V)	G_p (dB)	EFFICIENCY (CW) (%)	PAGE
Class-AB 26 V base stations						
BLF2047	SOT502A	65	26	>10	≥40	412
BLF2043	SOT538A	10	26	>12	≥40	402
BLF2045	SOT467A	30	26	>10	≥40	405
BLF2047L(1)	SOT502A	65	26	>10.5	≥40	419
BLF2047L/90(1)	SOT502A	90	26	>10.5	≥40	425
BLF2048	SOT539A	120	26	>10	≥40	433

Note

1. 1800 to 2000 MHz with optimized gain.

920 to 960 MHz RF amplifier modules

TYPE NUMBER	PACKAGE	LOAD POWER (W)	POWER GAIN (dB)	SUPPLY VOLTAGE V_{CE} (V)	EFFICIENCY (%)	PAGE
26 V base stations						
BGY916	SOT365A	16	≥28	26	≥35	62
BGY916/5	SOT365A	16	≥28	26	≥35	68
BGY925	SOT365A	23	≥28	26	≥30	75
BGY925/5	SOT365A	23	>28	26	≥30	82

1805 to 1880 MHz RF amplifier modules

TYPE NUMBER	PACKAGE	LOAD POWER (W)	POWER GAIN (dB)	SUPPLY VOLTAGE V_{CE} (V)	EFFICIENCY (%)	PAGE
26 V base stations						
BGY1816	SOT365A	16	>24	26	≥30	89
BGY1816S	SOT501A	>16	>29	26	≥30	94

1930 to 1990 MHz RF amplifier modules

TYPE NUMBER	PACKAGE	LOAD POWER (W)	POWER GAIN (dB)	SUPPLY VOLTAGE V_{CE} (V)	EFFICIENCY (%)	PAGE
26 V base stations						
BGY1916	SOT365	16	>24	26	>30	99

1800 to 2000 MHz RF amplifier modules

TYPE NUMBER	PACKAGE	LOAD POWER (W)	POWER GAIN (dB)	SUPPLY VOLTAGE V_{CE} (V)	EFFICIENCY (%)	PAGE
26 V base stations						
BGY2016	SOT36A5	≥16	≥28	26	≥30	104

MICROWAVE TRANSISTORS

Class-A Linear power transistors

TYPE NUMBER	PACKAGE	f (GHz)	V_{CE} (V)	I_C (mA)	P_{L1} (1) (W)	G_{po} (2) (dB)	G_p (dB)	PAGE
LBE2003S	SOT441A	2	18	30	>0.2	>10	–	919
LBE2009S	SOT441A	2	18	110	>0.7	>9	–	919
LTE21009R	SOT440A	2.1	16	150	>0.6	>10	–	929
LVE21050R	SOT445A	2.1	16	1100	5.5	8	–	944
LTE42005S	SOT440A	4.2	18	110	>0.45	>6.6	–	932
LTE42012R	SOT440A	4.2	16	400	>1	>6	–	938

Notes

1. Load power for 1 dB compressed power gain.
2. Low level power gain associated with P_{L1}.

CW power transistors

TYPE NUMBER	PACKAGE	CLASS	f (GHz)	V_{CC} (V)	P_L (1) (W)	G_p (2) (dB)	η_C (%)	PAGE
PTB23006U	SOT440A	C	2	28	>5	>9	>40	998
PTB32005X	SOT440A	B	3	24	≥4.5	>8	>35	1004

Notes

1. Load power for 1 dB compressed power gain.
2. Low level power gain associated with P_{L1}.

Pulsed power transistors for avionics

TYPE NUMBER	PACKAGE	f (GHz)	V_{CC} (V)	t_p (μS)	at δ (%)	P_L (W)	G_p (dB)	η_C (%)	PAGE
MZ0912B50Y	SOT443A	0.96 to 1.215	50	10	10	>50	>7	>42	992
MX0912B100Y	SOT439A	0.96 to 1.215	50	10	10	>100	>7	>42	959
MX0912B251Y	SOT439A	0.96 to 1.215	50	10	10	>235	>7	>42	966
MX0912B351Y	SOT439A	0.96 to 1.215	50	10	10	>325	>7	>40	973
MTB10010U	SOT440A	1.03	24	1	1	>9.5	>9.5	>50	954
MX1011B200Y	SOT439A	1.09	50	10	1	200	≥7.5	>45	980
MX1011B700Y	SOT439A	1.09	50	10	1	650	≥6	>48	986
MF1011B900Y	SOT448A	1.09	50	10	1	800	≥6	>40	947

L and S-band pulsed power transistors for radar

TYPE NUMBER	PACKAGE	f (GHz)	V_{CC} (V)	t_p (μS)	at δ (%)	P_L (W)	G_p (dB)	η_C (%)	PAGE
L-band									
RZ1214B35Y	SOT443A	1.2 to 1.4	50	150	5	≥35	≥7	>30	1032
RZ1214B65Y	SOT443A	1.2 to 1.4	50	150	5	≥70	≥7	>35	1036
RX1214B130Y	SOT439A	1.2 to 1.4	50	150	5	≥130	≥7	>35	1010
RX1214B170W	SOT439A	1.2 to 1.4	42	500	10	≥170	≥6	>40	1016
RX1214B300Y	SOT439A	1.2 to 1.4	50	150	5	≥250	≥7	>35	1021
RX1214B350Y	SOT439A	1.2 to 1.4	50	130	6	280	≥7	>40	1026
S-band									
BLS2731-10	SOT445C	2.7 to 3.1	40	100	10	≥10	typ. 9	typ. 45	440
BLS2731-20	SOT445C	2.7 to 3.1	40	100	10	≥20	typ. 8	typ. 40	446
BLS2731-50	SOT422A	2.7 to 3.1	40	100	10	>50	typ. 9	typ. 40	450
BLS2731-110	SOT423A	2.7 to 3.1	40	100	10	>110	typ. 7.5	typ. 40	454
S-band 50 Ω in/out matched transistor									
BLS3135-10	SOT422A	3.1 to 3.5	40	100	10	>10	typ. 9	typ. 40	459
BLS3135-20	SOT422A	3.1 to 3.5	40	100	10	>20	typ. 8	typ. 40	464
BLS3135-50	SOT422A	3.1 to 3.5	40	100	10	>50	typ. 8	typ. 40	469
BLS3135-65	SOT422A	3.1 to 3.5	40	100	10	65	≥7	typ. 40	473

SSB TRANSMITTERS (1.5 to 30 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (PEP) (W)	SUPPLY VOLTAGE (V)	Stud S Flange F
Bipolar						
30	BLV10(1)	2 × BLW87	–	30	13	F
50	BLV20(1)	2 × BLW83	–	50	28	F
50	BLV11(1)	2 × BLW85	–	50	13	F
100	BLW87(1)	4 × BLW85	–	100	13	F
150	BLW83(1)	2 × BLW76	–	150	28	F
250	2 × BLW83(1)	2 × BLW77	–	250	28	F
220	2 × BLW86(1)	2 × BLW97	–	300	28	F
500	2 × BLW86	4 × BLW77	–	450	28	F
300	2 × BLW83(2)	2 × BLW96	–	350	50	F
40	BLV20(2)	4 × BLW50F	8 × BLW96	1200	50	F
PowerMOS						
15	BLF244(1)	2 × BLF246	–	150	28	–
30	BLF145(1)	2 × BLF147	–	300	28	–
15	BLF244(2)	2 × BLF177	–	300	50	–
60	BLF246(1)	4 × BLF147	–	550	28	–
10	BLF175(1)	4 × BLF177	–	550	50	–
20	2 × BLF175(1)	8 × BLF177	–	1000	50	–

Notes

1. Class-A operation.
2. 28 V supply voltage in class-A operation.

MOBILE TRANSMITTERS (68 to 87.5 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar/PowerMOS				
1	BFG35	BLV10	8	13
1	BFG35	BLF245(1)	12	12.5
1	BFG35	BLV11	15	13
30	BLF244(1)	BLW85	45	13

Note

1. PowerMOS transistor.

BASE STATIONS (68 to 87.5 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)	Stud S Flange F
PowerMOS						
80	BLF242	BLF246	–	80	28	–
150	BLF244	BLF147	–	150	28	–

FM BROADCAST TRANSMITTERS (87.5 to 108 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)	Stud S Flange F
PowerMOS						
240	BLF244	BLF248	–	300	28	–
120	BLF244(1)	BLF278	–	300	50	–
240	BLF244(1)	2 × BLF278	–	550	50	–
320	BLF175	2 × BLF278	–	1000	50	–

Note

1. 28 V supply voltage in class-A operation.

MILITARY COMMUNICATION TRANSMITTERS (25 to 110 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
PowerMOS					
150	BLF242(1)	2 × BLF244	–	12	12.5
150	BLF242(1)	BLF245B	–	12	12.5
500	BLF244(1)	2 × BLF245	–	60	28
100	BLF242(1)	BLF245(1)	2 × BLF246	150	28

Note

1. Class-A operation.

AM AIRCRAFT TRANSMITTERS (108 to 144 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
PowerMOS				
100	BLF242	BLF246	20	28
80	BLF244	BLF147	35	28
120	BLF242(1)	BLF278	75	50

Note

1. 28 V supply voltage in class-A operation.

AM AIRCRAFT TRANSMITTERS (118 to 136 MHz)

INPUT POWER (mW)	1^{st} STAGE	2^{nd} STAGE	3^{rd} STAGE	P_L (W)	SUPPLY VOLTAGE (V)	Stud S Flange F
Bipolar						
240	BLV20	BLW86	–	12	13 or 28	F

AM AIRCRAFT TRANSMITTERS (100 to 400 MHz)

INPUT POWER (mW)	1^{st} STAGE	2^{nd} STAGE	3^{rd} STAGE	P_L (W)	SUPPLY VOLTAGE (V)	Stud S Flange F
PowerMOS						
25	BLF521(1)	BLF543	BLF546	80	28	–
30	BLF521(1)	BLF543	BLF547	100	28	–
100	BLF521(1)	BLF544	BLF548	150	28	–

Note

1. V_{DS} = 12.5 V.

PORTABLE and MOBILE TRANSMITTERS (132 to 174 MHz)

INPUT POWER (mW)	1^{st} STAGE	2^{nd} STAGE	3^{rd} STAGE	P_L (W)	SUPPLY VOLTAGE (V)	Stud S Flange F
PowerMOS						
1	BFG35	BLF245	–	12	12.5	F

BASE STATIONS (132 to 174 MHz)

INPUT POWER (mW)	1^{st} STAGE	2^{nd} STAGE	3^{rd} STAGE	P_L (W)	SUPPLY VOLTAGE (V)	Stud S Flange F
PowerMOS						
220	BLF242	BLF246	–	80	28	–

TV TRANSPOSERS (BAND III: 174 to 230 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	$P_{o(sync)}$ (W)	$P_{o(sat)}$ (W)	SUPPLY VOLTAGE (V)
PowerMOS						
5	BLF242	2 × BLF244	BLF348	40	60	28
5	BLF242	BLF245B	BLF348	40	60	28
12	BLF244	2 × BLF245	2 × BLF348	75	115	28
20	BLF244	2 × BLF346	4 × BLF348	140	220	28

TV TRANSMITTERS (BAND III: 174 to 230 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	$P_{o(sync)}$ (W)	SUPPLY VOLTAGE (V)
PowerMOS					
50	BLF242	2 × BLF244	BLF368	300	32
50	BLF242	BLF245B	BLF368	300	32
100	BLF242	2 × BLF245	2 × BLF368	550	32
160	BLF242	2 × BLF346	4 × BLF368	1000	32
50	BLF242(1)	2 × BLF175	6 × BLF378	1250	50

Note

1. 28 V supply voltage in class-A operation.

BASE STATIONS (400 to 470 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
PowerMOS					
40	BLF521(1)	BLF543	BLF546	80	28
45	BLF521(1)	BLF544	BLF547	100	28
150	BLF521(1)	BLF544	BLF548	150	28

Note

1. V_{DS} = 12.5 V.

TV TRANSPOSERS (BAND IV/V: 470 to 860 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	4th STAGE	$P_{o(sync)}$ (W)	$P_{o(sat)}$ (W)	SUPPLY VOLTAGE (V)
Bipolar							
6	BLW32	BLW33	2 × BLW34	–	4.4	5.7	25
2	BLW32	BLW33	2 × BLW34	2 × BLW98	8	8	25
3	BLW32	BLW33	2 × BLW34	2 × BLV57	13	15	25
3	BFQ68	BLW34	BLW98	2 × BLV58	25(1)	30	25
500	2 × BLW898	2 × BLV859	–	–	40	–	25

Note

1. 25 W sync, –51 dB (–8, –16, or –7 dB).

TV TRANSMITTERS (BAND IV/V: 470 to 860 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	4th STAGE	$P_{o(sync)}$ (W)	SUPPLY VOLTAGE (V)
Bipolar						
12	BFG97	BFQ68	2 × BLW34	2 × BLV59	60	28
15	BFQ34	BLW34	BLV58	BLV862	150	28
30	BFQ34	2 × BLW33	2 × BLV58	4 × BLV862	500	28

BASE STATIONS (860 to 960 MHz) CLASS-AB OPERATION

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	4th STAGE	P_L (W)	SUPPLY VOLTAGE (V)	FREQUENCY (MHz)
Bipolar							
65	BLV99/SL	BLV910	BLV946	–	40	26	960
25	BGY916	BLV958	–	–	75	26	960
75	BLV904	BLV920	BLV958	–	75	26	960
75	BLV904	BLV920	2 × BLV946	–	80	26	960

Note

1. d_{IM} = –30 dB.

BASE STATIONS (860 to 960 MHz) CLASS-AB OPERATION

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	4th STAGE	P_L (W)	SUPPLY VOLTAGE (V)	FREQUENCY (MHz)
LDMOST							
145	BLF1043	BLF1046	–	–	45	26	960
70	BLF1043	BLF1047	–	–	70	26	960
4	BLF1043	BLF1046	BLF1048	–	90	26	960

Note

1. d_{IM} = –30 dB.

BASE STATIONS (1800 to 2000 MHz) CLASS AB OPERATION

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)	FREQUENCY (MHz)
Bipolar						
60	BLV2042	BLV2042	BLV2044	15	26	DSC1800 & PCS1900
45	BLV2042	BLV2042	BLV2045N	30	26	DSC1800 & PCS1900
200	BLV2042	BLV2044	2 x BLV2045N	60	26	DSC1800 & PCS1900
30	BGY1816	BLV2047	–	60	26	DSC1800
30	BGY1916	BLV2047	–	60	26	PCS1900
30	BGY2016	BLV2047	–	60	26	DSC1800 & PCS1900
120	BLV2042	BLV2044	BLV2047	60	26	DSC1800 & PCS1900

BASE STATIONS (1800 to 2000 MHz) CLASS AB OPERATION

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	4th STAGE	P_L (W)	SUPPLY VOLTAGE (V)	FREQUENCY (MHz)
LDMOST							
170	BLF2043	BLF2045	–	–	30	26	2000
30	BLF2043	BLF2047L	–	–	65	26	2000
35	BLF2043	BLF2045	BLF2047L	–	65	26	2000
25	BLF2043	BLF2045	BLF2047L/90	–	90	26	2000
45	BLF2043	BLF2045	BLF2048	–	120	26	2000
65	BLF2043	BLF2045	BLF2047L/90	–	180	25	2000

W-CDMA (2.0 to 2.2 GHz) CLASS AB OPERATION

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
25	BLF2045	BLF2047	6 × BLF2047	360	26
25	BLF2045	BLF2047	3 × BLF2048	360	26

GENERAL

QUALITY

Total Quality Management

Philips Semiconductors is a Quality Company, aiming towards one ultimate standard, that of Business Excellence. The tool we use in striving towards this goal is our Total Quality Management (TQM) system. The TQM is described in our Quality manuals, and is summarized in the following paragraphs. The Philips Business Excellence Programme as part of TQM follows the European Foundation for Quality Management (EFQM) model. The EFQM award is on the level of the Malcolm Baldridge award.

QUALITY ASSURANCE

Quality Assurance (QA) is based on ISO 9000 standards and customer standards such as QS-9000. Our factories are certified to ISO 9000 and QS-9000 by external inspectorates. Sales organizations and headquarters are also certified to ISO 9000. The products of Philips Semiconductors are in conformance with the requirements of international standards.

PARTNERSHIPS WITH CUSTOMERS

Partnerships with customers include Process Quality measurement co-operation (using PPM), design-in agreements, ship-to-stock, just-in-time, sharing technology roadmaps, a change notification programme, self-qualification programmes and application support.

PARTNERSHIPS WITH SUPPLIERS

Our suppliers are certified to ISO 9000 and participate in ship-to-stock programmes. Key-suppliers receive support and feedback through our Supplier Quality System (SQS) audits.

CONTINUOUS IMPROVEMENT PROGRAMME

The continuous improvement programme incorporates continuous process and system improvement, design improvement, complete use of statistical process control, and logistics improvement, driven by key performance indicators. To encourage improvement in teamwork a very popular Quality Improvement Competition is held yearly. With a large number of improvement teams participating, opportunities arise for the sharing of successful improvement ideas.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. By means of failure-mode-and-effect analysis the critical parameters of a process are identified. Procedures are then laid down to ensure the highest level of performance for these parameters. The capability of process steps is also planned in this phase in preparation for production under statistical process control.

Quality network

Product quality is the responsibility of the Business Lines, with their Quality and Reliability (Q&R) departments operating in a supportive and controlling manner. The sales organization has Quality Managers who respond to any quality matters raised by customers. Customer complaints are then handled by direct contact between Sales Quality and the relevant Q&R department. General quality requirements are covered by a divisional Quality department.

Product conformance

The assurance of product conformance is an integral part of our Quality Assurance practice. This is achieved by:

- In-line Quality Assurance to monitor process reproducibility during manufacture. Equipment performance and process steps are under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for Quality feedback and corrective actions. Periodic sample inspections to monitor and measure the conformance of products are increasingly being replaced by continuous in-line monitoring.
- Qualification tests.

The inspection and test requirements are detailed in the General Quality Specifications in the SNW-FQ-611 series.

Product reliability

Highly accelerated tests are implemented to evaluate and monitor product reliability. Rejects from reliability tests are subjected to failure analysis, so that improvements may be made. This analysis also extends to product related customer complaints.

Customer response

Our quality improvement depends on working together with our customer. We need our customer's input, and we therefore invite constructive comments on all aspects of our performance. For all such matters, please contact your local Philips Semiconductors sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM

Basic type number

This type designation code applies to non-microwave discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors. Only code letters relevant to the devices in this data handbook are given here.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

B Silicon or other material with a band gap of 1 to 1.3 eV

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

G Multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter; see under Section "Serial number"

L Transistor; power, high frequency

SERIAL NUMBER

For devices primarily intended for industrial or professional equipment, the serial number comprises one letter (Z, Y, X, etc.) and two to four figures running from 10 to 9999.

Version letter

A letter may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type.

TYPE DESIGNATION CODE FOR MICROWAVE TRANSISTORS

Code structure

The standard structures of type designation code for microwave transistors can be shown as follows, where X represents a letter and 0 represents a numeral:

XXX0000X	for transistors without matching cell
XXX00000X	for transistors with input matching cell and specified for narrowband applications
XXX0000X00X or XXX0000X000X	for transistors specified for wideband applications

Letters

FIRST LETTER

The first letter shows the mode of operation:

L linear

M short pulse

P CW class B

R long pulse.

SECOND LETTER

The second letter shows the encapsulation:

A SOT100

B SOT441A (FO-45)

C SOT442A (FO-46)

E SOT122A

F SOT448A (FO-231)

L SOT437A (FO-229)

P SOT447A (FO-102)

T SOT440A (FO-41B)

V SOT445A (FO-83A and FO-83B)

W SOT446A (FO-93)

X SOT439A (FO-91B)

Z SOT443A (FO-57C).

THIRD LETTER

The third letter indicates the common potential:

E common emitter

B common base

C common collector.

FOURTH LETTER (SUFFIX LETTER)

The fourth letter indicates the supply voltage:

Q 10 to 12 V

R 15 to 16 V

S 18 V

T 20 V or 18 to 21 V

U 28 to 30 V

W 40 to 45 V

X 24 V

Y 50 V

Z 48 V.

Numbers

TRANSISTORS WITHOUT MATCHING CELL (XXX0000X)

1st digit indicates frequency of measurement (GHz).

2nd, 3rd and 4th digits indicate power:

in watts for P, M and R modes of operation

in multiples of 100 mW for L mode of operation.

TRANSISTORS SPECIFIED FOR NARROWBAND APPLICATIONS (XXX00000X)

1st and 2nd digits indicate frequency of measurement (× 0.1 GHz).

3rd, 4th and 5th digits give the power:

in watts for P, M and R modes of operation

in multiples of 100 mW for L mode of operation.

TRANSISTORS SPECIFIED FOR WIDEBAND APPLICATIONS

1st and 2nd digits indicate the lower frequency of use (in 0.1 GHz).

3rd and 4th digits indicate the higher frequency of use (in 0.1 GHz).

Last digit indicates the power:

in watts for P, M and R modes of operation

in multiples of 100 mW for L mode of operation.

MARKING CODES FOR RF POWER TRANSISTORS

For the purposes of matched pair applications, RF power MOS transistors are marked with a code that indicates their gate-source voltage range (see Table 1).

Table 1 Marking codes for RF power transistors

CODE	V_{GS}	CODE	V_{GS}
0	1.00 to 1.10	J	2.80 to 2.90
1	1.10 to 1.20	K	2.90 to 3.00
2	1.20 to 1.30	L	3.00 to 3.10
3	1.30 to 1.40	M	3.10 to 3.20
4	1.40 to 1.50	N	3.20 to 3.30
5	1.50 to 1.60	O	3.30 to 3.40
6	1.60 to 1.70	P	3.40 to 3.50
7	1.70 to 1.80	Q	3.50 to 3.60
8	1.80 to 1.90	R	3.60 to 3.70
9	1.90 to 2.00	S	3.70 to 3.80
A	2.00 to 2.10	T	3.80 to 3.90
B	2.10 to 2.20	U	3.90 to 4.00
C	2.20 to 2.30	V	4.00 to 4.10
D	2.30 to 2.40	W	4.10 to 4.20
E	2.40 to 2.50	X	4.20 to 4.30
F	2.50 to 2.60	Y	4.30 to 4.40
G	2.60 to 2.70	Z	4.40 to 4.50
H	2.70 to 2.80		

MARKING CODES FOR MICROWAVE TRANSISTORS

The microwave transistors in this book are normally marked with manufacturer's name or trademark, type designation and lot identification code. If space on the transistor package is insufficient for full type designation, the following marking codes may be used for identification (see Table 2).

Table 2 Marking codes for microwave transistors

TYPE NUMBER	MARKING CODE
LBE2003S	407
LBE2009S	409
LTE21009R	435
LTE42005S	502
LTE42012R	198
MTB10010U	10010U
PTB32005X	3205X

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its publication number 60134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS

The letter symbols for transistors and signal diodes detailed in this section are based on IEC publication number 60747.

Letter symbols for currents, voltages and powers

BASIC LETTERS

I, i	current
V, v	voltage
P, p	power.

Upper-case letter symbols are used to represent all values except instantaneous values that vary with time, these are represented by lower-case letters.

SUBSCRIPTS

A, a	anode terminal
(AV), (av)	average value
B, b	base terminal
C, c	collector terminal
D, d	drain terminal
E, e	emitter terminal
F, f	forward
G, g	gate terminal
K, k	cathode terminal
M, m	peak value
O, o	as third subscript: the terminal not mentioned is open-circuit
R, r	as first subscript: reverse. As second subscript: repetitive. As third subscript: with a specified resistance between the terminal not mentioned and the reference terminal
(RMS), (rms)	root-mean-square value
S, s	as first or second subscript: source terminal (FETs only). As second subscript: non-repetitive (not FETs). As third subscript: short circuit between the terminal not mentioned and the reference terminal
X, x	specified circuit
Z, z	replaces R to indicate the actual working voltage, current or power of voltage reference and voltage reference diodes.

No additional subscript is used for DC values.

Upper-case subscripts are used for the indication of:

- Continuous (DC) values (without signal), e.g. I_B
- Instantaneous total values, e.g. i_B
- Average total values, e.g. $I_{B(AV)}$
- Peak total values, e.g. I_{BM}
- Root-mean-square total values, e.g. $I_{B(RMS)}$.

Lower-case subscripts are used for the indication of values applying to the varying component alone:

- Instantaneous values, e.g. i_b
- Root-mean-square values, e.g. $I_{b(rms)}$
- Peak values, e.g. I_{bm}
- Average values, e.g. $I_{b(av)}$.

If more than one subscript is used, the subscript for which both styles exist are either all upper-case or all lower-case.

ADDITIONAL RULES FOR SUBSCRIPTS

Transistor currents

If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples: I_B, i_B, i_b, I_{bm}.

Diode currents

To indicate a forward current (conventional current flow into the anode terminal), the subscript F or f should be used. For a reverse current (conventional current flow out of the anode terminal), the subscript R or r should be used.

Examples: I_F, I_R, i_F, $I_{f(rms)}$.

Transistor voltages

If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples: V_{BE}, v_{BE}, v_{be}, V_{bem}.

Diode voltages

To indicate a forward voltage (anode positive with respect to cathode), the subscript F or f should be used. For a reverse voltage (anode negative with respect to cathode), the subscript R or r should be used.

Examples: V_F, V_R, v_F, V_{rm}.

Supply voltages or currents

Supply voltages or supply currents are indicated by repeating the appropriate terminal subscript.

Examples: V_{CC}, I_{EE}.

If it is necessary to indicate a reference terminal, this should be done by a third subscript.

Example: V_{CCE}.

Subscripts for devices with more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal, followed by a number. In the case of multiple subscripts, hyphens may be necessary to avoid confusion.

Examples:

I_{B2} continuous (DC) current flowing into the second base terminal

V_{B2-E} continuous (DC) voltage between the terminals of second base and emitter terminals.

Subscripts for multiple devices

For multiple unit devices, the subscripts are modified by a number preceding the letter subscript. In the case of multiple subscripts, hyphens may be necessary to avoid confusion.

Examples:

I_{2C} continuous (DC) current flowing into the collector terminal of the second unit

V_{1C-2C} continuous (DC) voltage between the collector terminals of the first and second units.

Application of the rules

Figure 1 represents a transistor collector current as a function of time. It comprises a continuous (DC) current and a varying component.

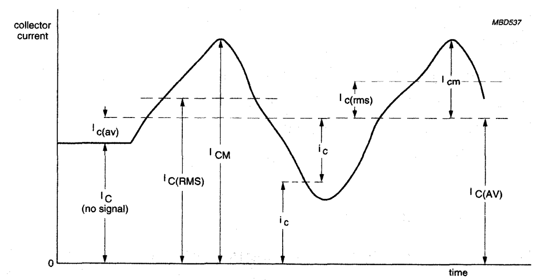


Fig.1 Collector current as a function of time.

Letter symbols for electrical parameters

DEFINITION

For the purpose of this publication, the term 'electrical parameter' applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

BASIC LETTERS

The following list comprises the most important basic letters used for electrical parameters of semiconductor devices.

B, b	susceptance (imaginary part of an admittance)
C	capacitance
G, g	conductance (real part of an admittance)
H, h	hybrid parameter
L	inductance
R, r	resistance (real part of an impedance)
X, x	reactance (imaginary part of an impedance)
Y, y	admittance
Z, z	impedance.

Upper-case letters are used for the representation of:

- Electrical parameters of external circuits and of circuits in which the device forms only a part.
- All inductances and capacitances.

Lower-case letters are used for the representation of electrical parameters inherent in the device, with the exception of inductances and capacitances.

SUBSCRIPTS

General subscripts

The following list comprises the most important general subscripts used for electrical parameters of semiconductor devices.

F, f	forward (forward transfer)
I, i (or 1)	input
L, l	load
O, o (or 2)	output
R, r	reverse (reverse transfer)
S, s	source.

Examples: Z_s, h_f, h_F.

The upper-case variant of a subscript is used for the designation of static (DC) values.

Examples:

h_{FE}static value of forward current transfer ratio in common-emitter configuration (DC current gain)

R_EDC value of the external emitter resistance.

The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript is used for the designation of small-signal values.

Examples:

h_{fe}small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration

$Z_e = R_e + jX_e$ small-signal value of the external impedance.

If more than one subscript is used, subscripts for which both styles exist are either all upper-case or all lower-case.

Examples: h_{FE}, y_{RE}, h_{fe}.

Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer.

Examples: h_i (or h_{11}), h_o (or h_{22}), h_f (or h_{21}), h_r (or h_{12}).

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E}).

DISTINCTION BETWEEN REAL AND IMAGINARY PARTS

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

Examples: $Z_i = R_i + jX_i$, $y_{fe} = g_{fe} + jb_{fe}$.

If such symbols do not exist, or if they are not suitable, the following notation is used:

Examples:

Re (h_{ib}) etc. for the real part of h_{ib}

Im (h_{ib}) etc. for the imaginary part of h_{ib}.

Scattering parameters

In distinction to the conventional h-, y- and z-parameters, scattering parameters (s-parameters) relate to travelling wave conditions. Fig.2 shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.

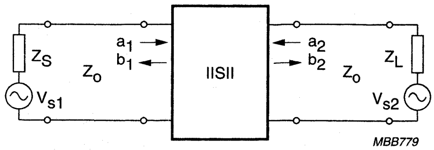


Fig.2 Two-port network.

From Fig.2: $a_1 = \frac{V_{i1}}{\sqrt{Z_0}}$; $a_2 = \frac{V_{i2}}{\sqrt{Z_0}}$; $b_1 = \frac{V_{r1}}{\sqrt{Z_0}}$; $b_2 = \frac{V_{r2}}{\sqrt{Z_0}}$

The squares of these quantities have the dimension of power.

Z_0 = characteristic impedance of the transmission line in which the two-port is connected

V_i = incident voltage

V_r = reflected (generated) voltage.

The four-pole equations for s-parameters are:

$b_1 = s_{11}a_1 + s_{12}a_2$

$b_2 = s_{21}a_1 + s_{22}a_2$.

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \frac{b_1}{a_1} \mid a_2 = 0$$

$$s_r = s_{12} = \frac{b_1}{a_2} \mid a_1 = 0$$

$$s_f = s_{21} = \frac{b_2}{a_1} \mid a_2 = 0$$

$$s_o = s_{22} = \frac{b_2}{a_2} \mid a_1 = 0$$

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ input reflection coefficient: the complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_L = Z_0 = 50\ \Omega$ and $V_{s2} = 0$

$s_r = s_{12}$ reverse transmission coefficient: the complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_S = Z_0 = 50\ \Omega$ and $V_{s1} = 0$

$s_f = s_{21}$ forward transmission coefficient: the complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_L = Z_0 = 50\ \Omega$ and $V_{s2} = 0$

$s_o = s_{22}$ output reflection coefficient: the complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_S = Z_0 = 50\ \Omega$ and $V_{s1} = 0$.

SOLDERING SMD TRANSISTORS

Introduction

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting (SMD). Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly. Surface mounting techniques are complex and this chapter gives only a simplified overview of the subject. For a more detailed description of soldering techniques, refer to the current edition of Data Handbook SC18 *"Discrete Semiconductor Packages"*.

Although many electronic components are available as surface mounting types, some are not and this often leads to the use of through-hole as well as surface mounting components on one substrate (a mixed print). The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

Reflow soldering process

There are three basic process steps for single-sided PCB reflow soldering, these are:

1. Applying solder paste to the PCB
2. Component placement
3. Reflow soldering.

Applying solder paste to the PCB

Solder paste can be applied to the PCB's solder lands by one of either three methods: dispensing, screen or stencil printing.

Dispensing is flexible but is slow, and only suitable for pitches of 0.65 mm and above.

With screen printing, a fine-mesh screen is placed over the PCB and the solder paste is forced through the mesh onto the solder lands of the PCB. However, because of mesh aperture limitations (emulsion resolution), this method is only suitable for solder paste deposits of 300 μm and wider.

Stencil printing is similar to screen printing, except that a metal stencil is used instead of a fine-mesh screen. The stencil is usually made of stainless steel or bronze and should be 150 to 200 μm thick. A squeegee is passed across the stencil to force solder paste through the apertures in the stencil and onto the solder lands on the PCB. It does not suffer from the same limitations as the other two printing methods and so is the preferred method currently available.

Component placement

The position of the component with respect to the solder lands is an important factor in the final result of the assembly process. A misaligned component can lead to unreliable joints, open circuits and/or bridges between leads.

The placement accuracy is defined as the maximum permissible deviation of the component outline or component leads, with respect to the actual position of the solder land pattern belonging to that component or component leads on the circuit board.

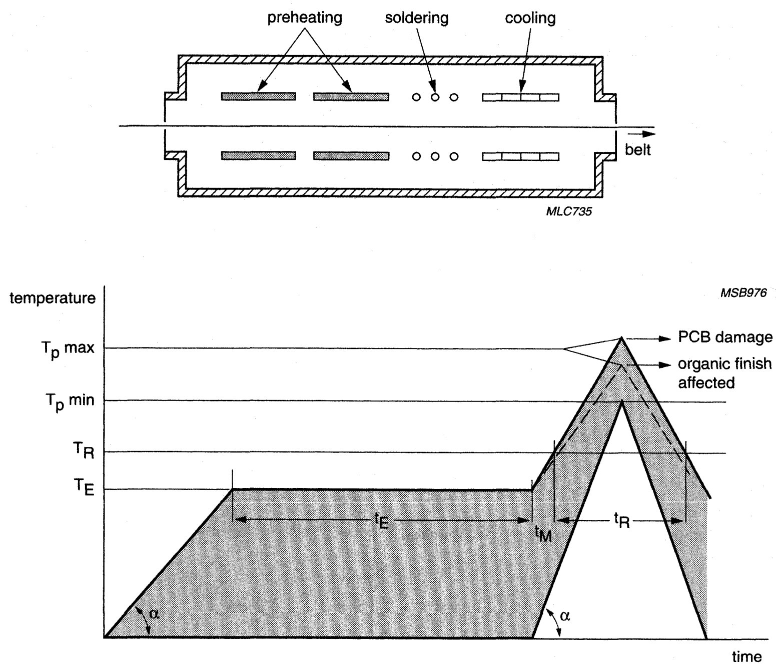
Reflow soldering

There are several methods available to provide the heat to reflow the solder paste, such as convection, hot belt, hot gas, vapour phase and resistance soldering. The preferred method is, however, convection reflow.

Convection reflow

With this method, the PCB passes through an oven where it is preheated, reflow soldered and cooled (see Fig.3). If the heating rate of the board and components are similar, however, preheating is not necessary.

During the reflow soldering process, all parts of the board must be subjected to an accurate temperature/ time profile. Figure 3 shows a suitable profile framework for single-sided reflow soldering and the first side of double-sided print boards. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.



α	≤ 10 °C/s.	t_E	≤ 1 min, if possible (else ≤ 5 min).
T_E	≤ 160 °C.	t_M	= 2 to 30 s.
T_R	= 180 °C.	t_R	≤ 70 s.
$T_p$min	= 205 °C.		
$T_p$max	= 240 °C		for soldering the first side of a double-sided board with organic finish.
$T_p$max	= 280 °C		for all other cases.

Fig.3 Convection reflow soldering method (top), process requirements for reflow soldering (bottom).

Double-wave soldering process

There are four basic process steps for double-wave soldering, these are:

1. Applying adhesive
2. Component placement
3. Curing adhesive
4. Wave soldering process.

APPLYING ADHESIVE

To hold SMDs on the board during wave soldering, it is necessary to bond the component to the PCB with one or more adhesive dots. This is done either by dispensing, stencilling or pin transfer. Dispensing is currently the most popular technique. It is flexible and allows a controlled amount of adhesive to be applied at each position. Stencil printing and pin transfer are less flexible and are mainly used for mass production.

COMPONENT PLACEMENT

Positioning components on the PCB is similar in practice to that of reflow soldering.To prevent component shift and smearing of the adhesive, board support is important while placing components.

CURING THE ADHESIVE

To provide sufficient bonding strength between component and board, the adhesive must be properly cured. The adhesive can be cured either by infrared or hot-air convection.

WAVE SOLDERING PROCESS

After applying adhesive, placing the component on the PCB and curing, the PCB can be wave soldered. The wave soldering process is basically built up from three sub-processes. These are:

1. Fluxing
2. Preheating
3. (Double) wave soldering.

Although listed here as sub-process they are in practice combined in one machine. All are served by one transport mechanism, which guides the PCBs at an incline through the soldering machine. It's important to note that the PCB must be loaded into the machine so that the SMDs on the board come into direct contact with the solder wave (see Fig.4).

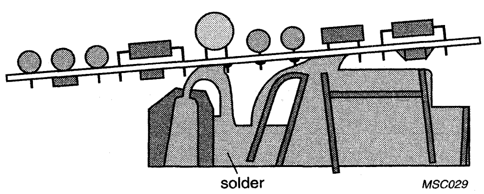


Fig.4 Double-wave soldering.

Fluxing

Fluxing is necessary to promote wetting both of the PCB and the mounted components. This ensures a good and even solder joint. During the fluxing process, the solder side of the PCB (including the components) are covered with a thin layer of solder flux, which can be applied to the PCB either by spraying or as a foam.

Preheating

After the flux is applied, the PCB needs to be preheated. This serves several purposes: it evaporates the flux solvents, it accelerates the activity of the flux and it heats the PCB and components to reduce thermal shock.

The required pre-heat temperature depends on the type of flux used. For example, the more common low-residue fluxes require a pre-heat temperature of 120 °C (measured on the wave solder side of the PCB).

(Double) wave soldering

The PCB first passes over a highly intensive (jet) solder wave with a carefully controlled constant height. This ensures good contact with the PCB, the edges of SMDs and the leads of components near to high non-wetted bodies. The greater the board's immersion depth into this first wave, the fewer joints will be missed.

The second, smoother laminar solder wave completes formation of the solder fillet, giving an optimal soldered connection between component and PCB. It also reduces the possibility of solder bridging by taking up excessive solder.

To reduce lead/tin oxides and possibly other solder imperfection forming during soldering, the complete wave configuration can be encapsulated by an inert atmosphere such as nitrogen.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

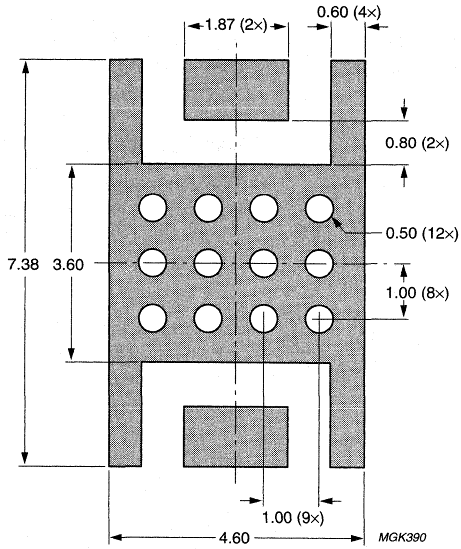
- Hand-soldering is time-consuming and therefore expensive
- The component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- There is a risk of breaking the substrate and internal connections in the component could be damaged
- The component package could be damaged by the iron.

Specific recommendations for SOT409

Both the metallized ground plate and leads contribute to the heatflow. For the best results it is recommended to mount the transistor on a grounded metallized area on the printed-circuit board equipped with a large number of metallized through-holes filled with solder. A thermal resistance ($R_{th\ mb\text{-}h}$) of 0.9 K/W can be achieved if a heatsink compound is used when the printed-circuit board is mounted on the heatsink.

Recommended footprints

The recommended footprints for the discrete semiconductor packages contained in this book are given in Fig.5.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

Fig.5 Reflow soldering footprint for SOT409 (not suitable for wave soldering); typical dimensions.

SOLDERING SMD MODULES

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens. Two reflow steps are permitted.

Hand soldering must be avoided because the soldering iron tip can exceed the maximum permitted temperature of 250 °C and damage the module.

The maximum allowed temperature is (see Fig.6):

t = 5 s at 250 °C.

The maximum ramp-up is 10 °C per second.

The maximum cool-down is 5 °C per second.

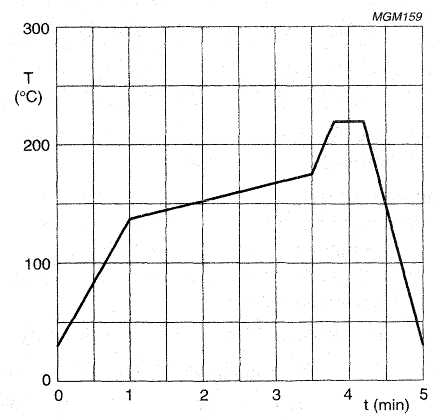


Fig.6 Recommended reflow temperature profile.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.

MOUNTING FLANGED TRANSISTORS AND MODULES

Mounting recommendations for transistors

- Ensure holes in heatsinks are free from burrs.
- Minimum depth of tapped holes in heatsinks is 6 mm.
- Use 4-40 UNC-2A cheese-head screws with a flat washer to spread the joint pressure.
- For transistors dissipating up to 80 W, the heatsink thickness should be at least 3 mm copper (> 99.9% ETP-Cu) or 5 mm aluminium (99% Al). The thickness of the heatsink should be increased proportionally for transistors dissipating more power.
- The minimum flatness of the mounting area is 0.01 mm.
- Mounting area roughness should be less than 0.5 μm.
- Avoid, as much as possible, use of flux or flux solutions because flux can penetrate even hermetically sealed ceramic-capped transistors. Tin and wash the printed-circuit boards **before** mounting the transistors, then solder the transistors into place without using flux.
- Transistor leads may be tinned by dipping them full-length into a solder bath at a temperature of about 230 °C. No flux should be used during tinning.
- Recommended heatsink compounds: WPS II (silicone-free) from Austerlitz-Electronics; Comp. Trans. from KF; 340 from Dow Corning; Trans-Heat from E. Friis-Mikkelsen.
- When a transistor is removed from a heatsink, the flange, almost certainly, will have been distorted by the joint pressure. Grinding or lapping of the flange to the required flatness and smoothness is necessary before the transistor is remounted.

MOUNTING SEQUENCE

- Apply a thin layer of evenly-distributed heatsink compound to the flange.
- Position the device with flat washers in place.
- Tighten the screws until finger-tight (0.05 Nm).
- Further tighten the screws until the specified torque is reached (do not lubricate). Refer to Table 3 for torques.
- To lock mounting screws, allow about 30 minutes for them to bed-down after the specified torque has been applied, re-tighten to the specified torque and apply locking paint.

Table 3 Specified torque for flange mounted transistors

PACKAGE	TORQUE (Nm)	
	min	max
SOT119	0.6	0.75
SOT121	0.6	0.75
SOT123	0.6	0.75
SOT161	0.6	0.75
SOT171	0.6	0.75
SOT262	0.6	0.75
SOT268	0.6	0.75
SOT273	0.6	0.75
SOT279	0.6	0.75
SOT289	0.6	0.75
SOT324B	0.6	0.75
SOT390	–	0.5
SOT391A	0.6	0.75
SOT391B	0.6	0.75
SOT422	–	0.5
SOT423	–	0.4
SOT437	–	0.5
SOT439	–	0.4
SOT440	–	0.4
SOT443	–	0.5
SOT445	–	0.4
SOT448	–	0.5
SOT468	–	0.4

Mounting recommendations for flanged modules

Modules (such as the SOT365) are manufactured using a ceramic substrate soldered to a copper or iron flange or mounting base; this causes a small thermal mismatch between these two components. A further thermal mismatch will exist between the mounting base and the heatsink to which it is mounted. Because of these mismatches, precautions must be taken to avoid unnecessary mechanical stresses being applied to the ceramic substrate and other components within the module resulting from variations in temperature during operating cycles.

DESIGN OF HEATSINK

To ensure that the maximum specified mounting base temperature will not be exceeded under maximum fault conditions, the module should always be mounted on a heatsink of suitable thermal resistance.

The mounting area of the heatsink should be flat and free from burrs and loose particles. Particular attention should be paid to the mounting hole areas. The maximum amount of bowing along the plane of the module should not exceed 0.1 mm. Where anodizing is used, the area under the module should be milled clean as the presence of anodizing under the module can result in high resistance earth paths, leading to oscillation and early failure, in addition to poor thermal contact.

The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should not be less than 5 mm, to ensure a rigid assembly. On finned heatsinks, the module should be mounted along a plane parallel to the fins.

MOUNTING OF MODULES

To ensure a good thermal contact and to prevent mechanical stresses when bolted down, the flatness of the mounting base is designed to be typically better than 100 μm.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to "finger tight" and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

A thin, even layer of thermal compound should be used between the mounting base and the heatsink to achieve the best possible contact thermal resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting base; too little will also result in poor thermal resistance.

When mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap. ESD precautions must be taken to protect the device from electro-static damage.

ELECTRICAL CONNECTIONS

The main earth return path of all modules is via the mounting base; it is therefore important that the heatsink is well earthed and that return paths are kept as short as possible. Failure to ensure this may result in loss of output power or oscillation, which in turn will have a detrimental effect on the module life.

The RF output connection should be to correctly-designed 50 Ω terminations. Failure to do this will result in a mismatch being presented to the module, with a resulting reduction in module life.

THERMAL BEHAVIOUR OF TRANSISTORS

The thermal behaviour of packages is dependent on the materials used to construct the package. Table 4 gives an overview of the materials used in packages, while Table 5 shows the coefficients of linear thermal expansion for each material. The thermal expansion of the different parts can be calculated from this data.

Table 4 Overview of materials used in packages

PACKAGE	FLANGE			LEADFRAME				BACK-PAD	CERAMIC INSULATOR		
	Cu	W-Cu	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	Ni	KOVAR (Fe54/Ni29)	Cu	Cu	BeO	AlN	Al_2O_3
SOT119	√	–	–	√	–	–	–	–	√	–	–
SOT120	√(1)	–	–	√	–	–	–	–	√	–	–
SOT121	√	–	–	√	–	–	–	–	√	–	–
SOT122	√(1)	–	–	√	–	–	–	–	√	–	–
SOT123	√	–	–	√	–	–	–	–	√	–	–
SOT147	√(1)	–	–	√	–	–	–	–	√	–	–
SOT161	√	–	–	√	–	–	–	–	√	–	–
SOT171	√	–	–	√	–	–	–	–	√	–	–
SOT172	–	–	–	√	–	–	–	–	√	–	–
SOT262	–	√	–	√	–	–	–	–	√	–	–
SOT268	–	√	–	√	–	–	–	–	√	–	–
SOT273	√	–	–	√	–	–	–	–	√	–	–
SOT279	√	–	–	√	–	–	–	–	√	–	–
SOT289	–	√	–	–	–	√	–	–	√	–	–
SOT324	–	√	–	√	–	–	–	–	√	–	–
SOT390	–	√	–	√	–	–	–	–	√	–	–
SOT391	–	√	–	√	–	–	–	–	√	–	–
SOT391B	–	–	–	√	–	–	–	√	√	–	–
SOT409B	–	–	–	–	–	–	√	√	–	√	–
SOT422	√	–	–	–	√	–	–	–	√	–	–
SOT423	√	–	–	–	√	–	–	–	√	–	–
SOT437	–	√	–	√	–	–	–	–	√	–	–
SOT439	√	–	–	–	√	–	–	–	√	–	–
SOT440	√	–	–	–	–	√	–	–	√	–	–
SOT441	–	–	–	√	–	–	–	–	√	–	–
SOT443	–	√	–	–	–	√	–	–	√	–	–
SOT445	√	–	–	–	–	√	–	–	√	–	–
SOT448	–	√	–	–	√	–	–	–	√	–	–
SOT467	–	√	–	√	–	–	–	–	–	–	√
SOT468	–	–	√	√	–	–	–	–	–	√	–
SOT502	–	√	–	√	–	–	–	–	–	–	√
SOT504	–	√	–	√	–	–	–	–	√	–	–
SOT538	√	–	–	–	–	–	–	–	–	–	√
SOT539	–	√	–	√	–	–	–	–	–	–	√
SOT540	–	√	–	√	–	–	–	–	–	–	√
SOT541	–	√	–	√	–	–	–	–	–	–	√

Note

1. Not flange, but stud.

Table 5 Coefficients of linear thermal expansion of package materials between 25 and 150 °C

SYMBOL	Cu	W-Cu	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	Ni	KOVAR (Fe54/Ni29)	BeO	AlN	UNIT
α	17.9	6.6	9.5 to 6.0	4.5	11.6	4.4	6.7	4.0	ppm/K

CAPSTAN HEADERS

Table 6 Mounting data for capstan headers

ITEM	MOUNTING STUD DIAMETER			TOLERANCE	UNIT
	1/4″	3/8″	1/2″		
Thread	8-32 UNC-2A(B)	10-32 UNF-2A(B)	1/4″ × 28 UNF-2A(B)	–	–
Maximum diameter of threaded stud	4.14	4.80	6.33	–	mm
Diameter of heatsink mounting hole	4.15	4.85	6.35	+0.05/–0	mm
Mounting nut thickness	3.5 and 5	5	5.5	–	mm
Mounting nut torque:					
minimum	0.75	1.5	2.3	–	Nm
maximum	0.85	1.7	2.7	–	Nm
Distance from heatsink to printed-circuit board	2.9	3.8	4.8	+0/–0.2	mm

Mounting recommendations

- Avoid, as much as possible, use of flux or flux solutions because flux can penetrate even hermetically sealed ceramic-capped transistors. Tin and wash the printed-circuit boards **before** mounting the power transistors, then solder the transistors into place without using flux.
- Transistor leads may be tinned by dipping them full-length into a solder bath at a temperature of about 230 °C. No flux should be used during tinning.
- Heatsink surfaces at the mounting hole are to be flat, parallel and free of burrs or oxidation.
- Do not use locking washers, their locking action can deteriorate in time due to the comparative softness of most heatsink materials. A flat washer can be used to spread the joint pressure.
- Ensure a positive clearance exists between leads and printed circuit board, this prevents upward lead-bending and consequent damage to the encapsulation
- Recommended heatsink compounds: WPS II (silicone-free) from Austerlitz-Electronics; Comp. Trans. from KF; 340 from Dow Corning; Trans-Heat from E. Friis-Mikkelsen.
- The full mounting nut torque should be applied only once in the life of a transistor. For pre-assembly testing, apply no more than two-thirds of the specified torque.

Mounting sequence

- Apply a thin layer of evenly-distributed heatsink compound to the heatsink.
- Position the device with a flat washer in place.
- Tighten the screws until finger-tight (0.05 Nm).
- Further tighten the screws until the specified torque is reached (do not lubricate); for torques, refer to the package outline section of this data handbook.
- To lock mounting screws, allow about 30 minutes for them to bed-down after the specified torque has been applied, re-tighten to the specified torque and apply locking paint.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. Our RF Power MOS transistors are sensitive to electrostatic discharge and, to avoid damage, the following precautions must be taken.

Work station

Figure 7 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material.

The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

Our devices are packed for dispatch in antistatic conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

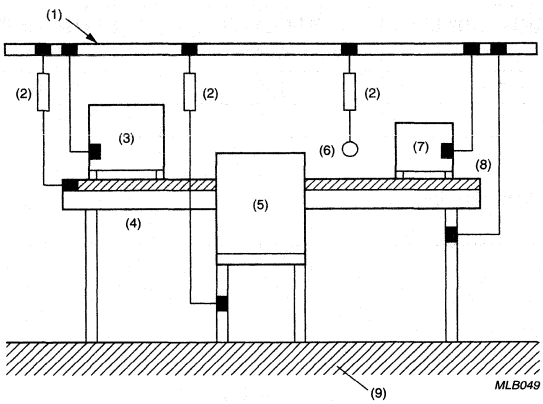
Assembly

The devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards should be handled in the same way as unmounted devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ±10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.7 Protected work station.

TAPE AND REEL PACKING

Packing types

Table 7 Packing quantities per reel

PACKAGE	TAPE WIDTH (mm)	REEL SIZE (mm)	QUANTITY PER REEL	12NC[(1)] ends with:
SOT409A/B	16	180	500	...115
SOT502	44	360	300	...135

Note

1. 12NC is the Philips twelve-digit ordering code.

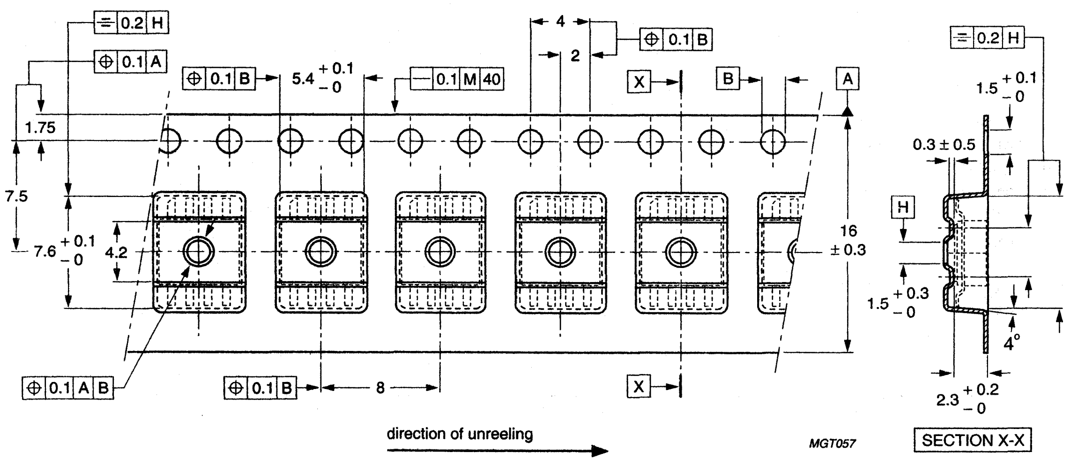
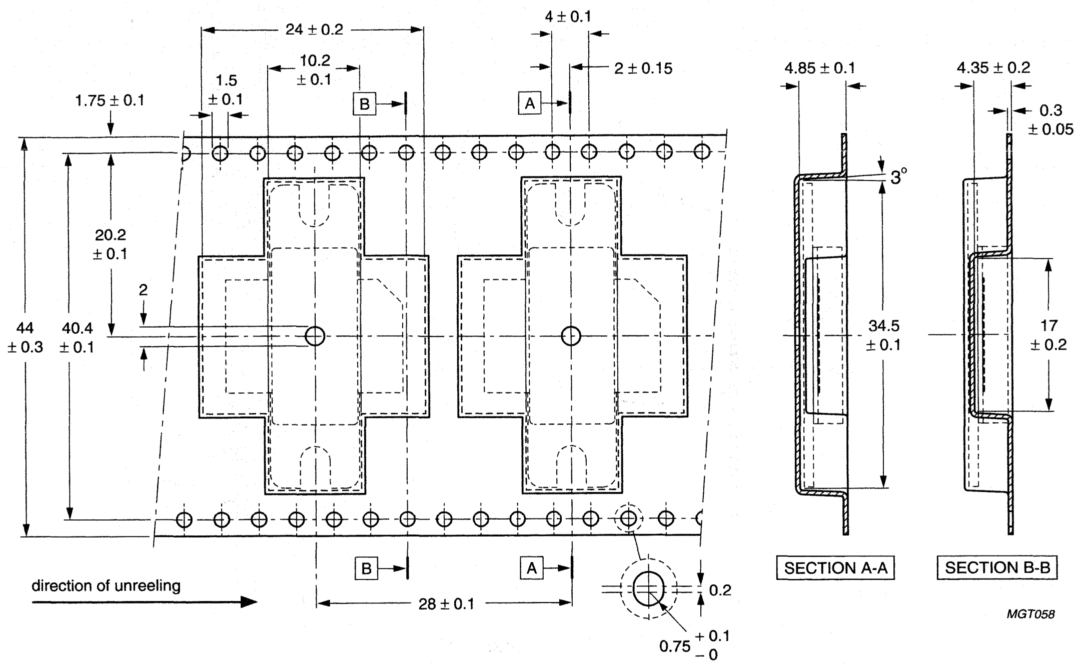
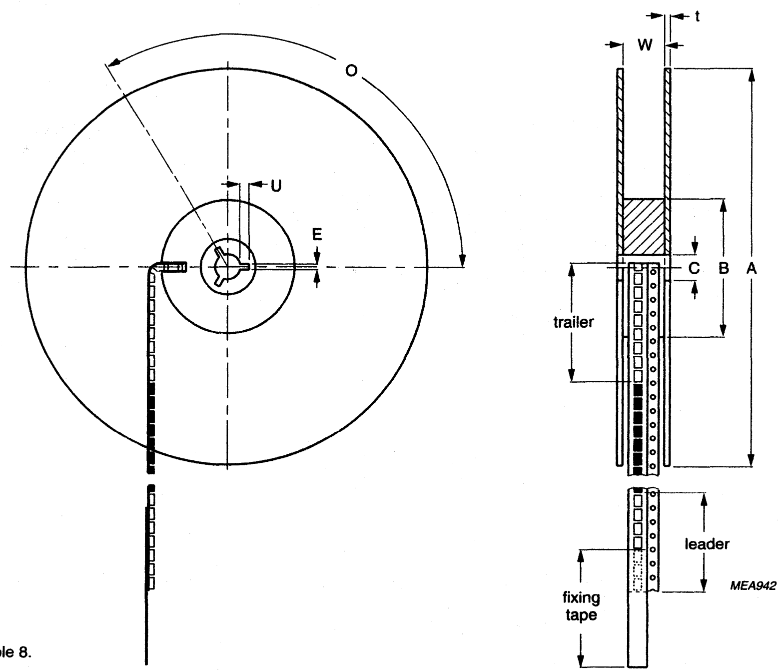


Fig.8 Specification of tape for SOT409.



(1) Tolerance over any 10 pitches: ±0.2 mm.

Fig.9 Specification of tape for SOT502.



For dimensions see Table 8.

Fig.10 Reel specification.

Table 8 Reel dimensions (in mm)

DIMENSION (see Fig.10)	**16 mm CARRIER TAPE**	**TOLERANCE**	**40 mm CARRIER TAPE**	**TOLERANCE**
Flange				
A	180	±0.5	330	–
t	1.5	+0.5/–0.1	3	–
W	16.4	±0.2	44.4	+2/–0
Hub				
B	62	±1.5	101	±1.5
C	12.75	+0.15/–0.2	13	±1.5
Key slot				
E	2	±0.2	1.5	–
U	4	±0.5	3.6	–
O	120°	–	120°	–

THERMAL CONSIDERATIONS

Introduction

This chapter only gives a brief overview of the thermal characteristics of discrete semiconductors. For a more in-depth explanation, refer to the current edition of Data Handbook SC18 *"Discrete Semiconductor Packages"*.

Thermal resistance

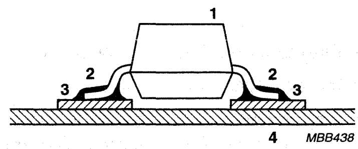
Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a a printed board, a substrate or heatsink. Referring to Fig.11 (for surface mounted devices mounted on a substrate), heat conducts from its source (the junction) via the package leads and soldered connections to the substrate. Some heat radiates from the package into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The elements of thermal resistance shown in Fig.12 are defined as follows:

$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base
$R_{th\ j\text{-}c}$	thermal resistance from junction to case
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point
$R_{th\ c\text{-}a}$	thermal resistance from case to ambient
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient.



Heat radiates from the package '1' to ambient.
Heat conducts via leads '2', solder joints '3' to the substrate '4'.

Fig.11 Heat losses.

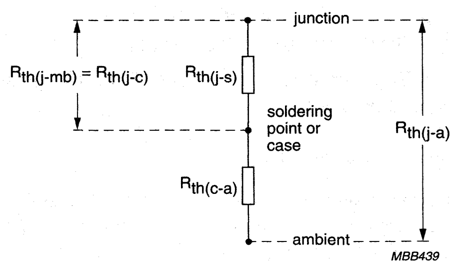


Fig.12 Representation of thermal resistance paths of a device mounted on a substrate or printed board.

The temperature at the junction depends on the ability of the package and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$$T_{j\,max} = T_{amb} + P_{tot\,max}(R_{th\,j\text{-}s} + R_{th\,s\text{-}a})$$
$$= T_{amb} + P_{tot\,max}(R_{th\,j\text{-}a})$$

where:

$T_{j\,max}$ is the maximum junction temperature

T_{amb} is the ambient temperature

$P_{tot\,max}$ is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\,max}$, only T_{amb} and $R_{th\,s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\,s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\,j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the package construction, the die bonding method and the die area, all of which are fixed.

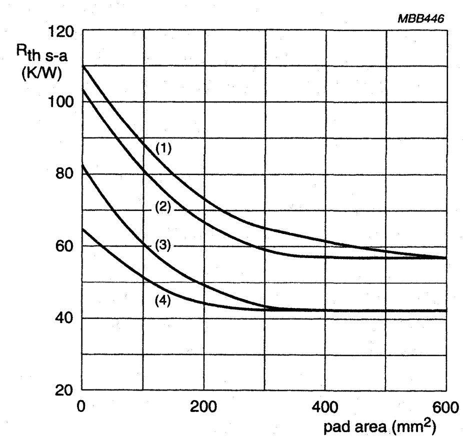
For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from

$T_j = T_{case} + P_{tot} \times R_{th\,j\text{-}c}$ or, using the soldering point definition, from $T_j = T_{solder} + P_{tot} \times R_{th\,j\text{-}s}$.

Values of $T_{j\,max}$ and $R_{th\,j\text{-}s}$, or $R_{th\,j\text{-}c}$ or $R_{th\,j\text{-}a}$ are given in the device data sheets.

Thermal resistance ($R_{th\,s\text{-}a}$)

The thermal resistance from soldering point to ambient, and that from case to ambient depends on the shape and material of the tracks and substrate as illustrated in Figure 13.



(1) Single-sided, unplated.
(2) Single-sided, plated.
(3) Double-sided, unplated.
(4) Double-sided, plated.

Fig.13 Thermal resistance ($R_{th\,s\text{-}a}$) as a function of pad area on different configurations of FR4 epoxy fibre-glass circuit board.

RELIABILITY GRADES

Microwave transistors are available from different quality levels which are listed as follows:

- **Standard grade**

  This applies to devices following the designation rules as listed in the chapters “Type Designation Code For Microwave Transistors”and “Pro Electron Type Numbering System”.

- **Grade “X” and “Y”**

  These grades correspond respectively to the equivalent MIL-STD 19500 grades JANTX and JANTXV.

  They have been subject to additional screening tests than those normally applied to the standard grade. The local sales organization can confirm whether they are available for the type you have selected.

  The majority of the devices included in this book may also be available in accordance with a space screening file similar to JANS or ESA/SCC5010.

Reliability grades (only for brazed cap devices and orders in excess of 50 parts)

OPERATION	MIL STD 750 METHOD	CONDITIONS	REQUIREMENTS (%)		
			STD GRADE	GRADE “X”(1)	GRADE “Y”(2)
Assembly			100	100	100
Internal visual inspection		note 3	100	100	100
Capping			100	100	100
Stabilization bake	1032	T = 200 °C; duration 48 hours	100	100	100
Temperature cycling	1051	condition C; 20 cycles; no dwell at 25 °C	–	100	100
Constant acceleration	2006	20000 g axis Y1; P_{tot} ≤5 W	–	–	100
		10000 g axis Y1; P_{tot} >5 W	–	–	100
Hermetic seal (brazed cap)	1071	condition H - FC43			
fine			100	100	100
gross			100	100	100
Serialisation			–	–	100
Initial electrical parameters		note 4	–	100 GO/NOGO	100 GO/NOGO

OPERATION	MIL STD 750 METHOD	CONDITIONS	REQUIREMENTS (%)		
			STD GRADE	GRADE "X"(1)	GRADE "Y"(2)
High temperature reverse bias (HTRB)	1039	T_{amb} = 150 °C; V_{CBmin} = 80% of published V_{CB}; duration 48 hours	–	100	100
Interim electrical parameters		note 5	–	–	100 read and record
Power burn-in	1039	T_{amb} = 125 °C; V_{CB} = 10 V; I_C reached when T_j average = 175 °C; duration 160 hours	–	–	100
Delta calculation		note 6	–	–	100
Other electrical parameters		note 4	100	100 GO/NOGO	read and record
Marking		as specified	100	100	100
External visual inspection	2071		100	100	100
Packing			100	100	100
Check for delivery		note 3			

Notes

1. Grade "X" is equivalent to JANTX.
2. Grade "Y" is equivalent to JANTXV.
3. As per Philips component specification.
4. Published DC, R_{th} and RF parameters.
5. Interim electrical parameters are published.
6. Published collector cut off current and forward current ratio. Delta limits are: Delta h_{FE} max = ±20% of initial value; Delta cut off current max = ±100% of initial value or ±10% of published parameter limit (whichever is greater).

BATCH RELEASE TESTS FOR GRADE "X" AND "Y" EQUIVALENTS

Group B; note 1.

INSPECTIONS	MIL STD 750 METHOD	CONDITIONS	SAMPLING PLAN LTPD(2)	SMALL LOT QUALITY CONFORMANCE INSPECTION	
				NO. OF DEVICES	NO. OF FAILURES
Subgroup 1					
Solderability	2026	the sampling plan applies to the number of leads inspected. A minimum of 3 devices shall be tested.	15	4	0
Resistance to solvents	1022				
Subgroup 2					
Temperature cycling (air to air)	1051	no dwell at 25 °C; test condition C, except step 3 at 175 °C; 45 cycles including screening	10	6	0
Thermal shock	1056	10 cycles; condition A			
Hermetic seal	1071				
fine leak		test condition H; max. leak rate = 5×10^{-7} atm cc/s			
gross leak		test condition C			
Electrical measurements		DC parameters of the relevant data sheet			
Subgroup 3					
Steady-state operation life	1027	as power burn-in except T_{mb} = 150 °C; duration 340 hours	10	12	0
Electrical measurements		DC parameters of the relevant data sheet			
Bond strength	2037	the sample shall include a minimum of 3 devices and shall include all wire sizes	20 (wires)	20 (wires)	0
Subgroup 4					
Decap internal visual (design criteria)	2075	visual criteria in accordance with qualified design		1	0
Subgroup 5 (not applicable)					
Subgroup 6					
High temperature life (non operating)	1032	340 hours at T_{amb} = 200 °C (brazed cap)	10	12	0
Electrical measurements		DC parameters of the relevant data sheet			

Notes

1. Optional for grades "X" and "Y" (minimum order quantity = 50 devices).
2. Sampling according to MIL-STD 19500. Small lot sampling applies for batches up to 500 devices.

SUMMARY OF SYMBOLS FOR MICROWAVE TRANSISTORS

C_{cb}	collector-base capacitance
C_{ce}	collector-emitter capacitance
C_{eb}	emitter-base capacitance
d_{im}	intermodulation distortion
δ	duty factor
F_{min}	noise factor
f	signal frequency
G_a	associated gain (for a low-noise transistor)
G_{ma}	maximum available gain
G_{ms}	maximum stable gain
G_p	power gain under specified conditions
G_{po}	low level power gain associated with P_{L1}
h_{FE}	DC current gain
I_C	DC collector current
I_{CBO}	collector cut-off current, open emitter
I_{CER}	collector cut-off current, with specified R_{BE}
I_{CES}	collector cut-off current, base connected to emitter
I_{CQ}	quiescent current
I_{EBO}	emitter cut-off current, open collector
η_C	collector efficiency $P_L / (I_C \times V_{CC})$
η_{add}	power added efficiency $(P_{out} - P_{in}) / (I_C \times V_{CC})$
P_{in}	input power
P_L	load power under specified conditions
P_{L1}	load power for 1 dB compressed power gain
P_{out}	output power
P_{tot}	total power dissipation
$R_{th\ j\text{-}c}$	thermal resistance from junction to case
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base
$R_{th\ mb\text{-}j}$	thermal resistance from mounting base to heatsink
T_j	junction temperature
t_p	pulse width
T_{sld}	lead soldering temperature
T_{stg}	storage temperature
V_{CBO}	collector-base voltage, open emitter
V_{CC}	collector supply voltage
V_{CE}	collector-emitter voltage
V_{CEO}	collector-emitter voltage, open base
V_{CER}	collector-emitter voltage with specified R_{BE}
V_{CES}	collector-emitter voltage, base connected to emitter
V_{EBO}	emitter-base voltage, open collector
VSWR	voltage standing wave ratio
z_i	complex transistor impedance as seen by the generator
Z_L	complex transistor load impedance as seen by the transistor
Z_{th}	thermal impedance from junction to heatsink.

OPERATING RECOMMENDATIONS

These recommendations are included for the avoidance of damage or destruction of silicon bipolar transistors operating at high frequencies and high power during testing, setting-up procedures and final operation.

Polarization

A current-limiting power supply should be used when testing transistors in a new circuit.

Initial testing at reduced supply voltage is discouraged because the resulting change in output impedance could cause oscillation due to mismatch.

The RF blocking choke in the supply line, together with the DC blocking capacitor of the internal output prematching circuit of the transistor, could sometimes cause oscillations at very low frequencies. The oscillations can often be removed by bypassing the choke with a low value resistor.

Operation

INPUT POWER

When the circuit has not been optimized, the average power input should be kept a lower level than specified. Initial testing of CW amplifiers is best performed in pulsed operation at 50% duty factor. For pulsed amplifiers, the duty factor should be reduced.

OUTPUT WAVEFORM

The output waveform should be checked with a spectrum analyser or similar equipment to ensure that no parasitic effects causing unwanted modulation are present.

FREQUENCY

Microwave performance is published in the data sheet at a single frequency or for a range of frequencies. Devices whose data is published for narrow band application can normally be used at frequencies other than that specified. However, for high power types in particular, broadband operation may be difficult to obtain and the gain of transistors with an internal input prematching network may decrease sharply at higher frequencies.

Broadband transistors (generally those with type numbers starting with two letters followed by four digits) also have an output prematching network. This is essentially a high-pass filter with a resonance frequency below the lowest operating frequency. The transistor could be damaged if operated at this resonance frequency, therefore the manufacturer should be consulted if extended frequency operation is required.

Thermal considerations

The junction temperature is of paramount importance in the reliability of transistors and every effort should be made to keep this temperature as low as possible. This is affected by mechanical aspects of the fitting, therefore mounting recommendations given by the manufacturer should be followed.

Values of thermal resistance given in the data sheets are for a specific junction temperature. Note that thermal resistance from junction to mounting base increases with junction temperature at approximately 0.3%/K.

For transistors required for pulsed operation, an equivalent thermal impedance is given for a specified pulse format (pulse width and duty factor). This allows for calculation of peak junction temperature (at the end of a pulse). For widely differing pulse formats the manufacturer should be consulted.

The maximum power dissipation is defined as $P_{tot} = V_{CE} \times I_C - P_o + P_i$ at $T_j = 200$ °C.

APPLICATION INFORMATION

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	TYPE NUMBER
A	amplifier			1/4 MC3403 or equivalent
D.U.T.	microwave transistor			
TR	transistor			2N2219 or equivalent
D	diode			1N4148 or equivalent
C1, C2	tantalum capacitor	22 μF, 50 V		
R1	resistor	2.2 kΩ ±5%		
R2, R3, R5, R6	resistor	10 kΩ ±5%		
R4	resistor	4.7 kΩ ±5%		
R_p	resistor	10 kΩ ±5%	10 turns	
R_b, R_c, R_e, R_x	resistor	note 1		

Note

1. Values to be adapted to I_c of the D.U.T.

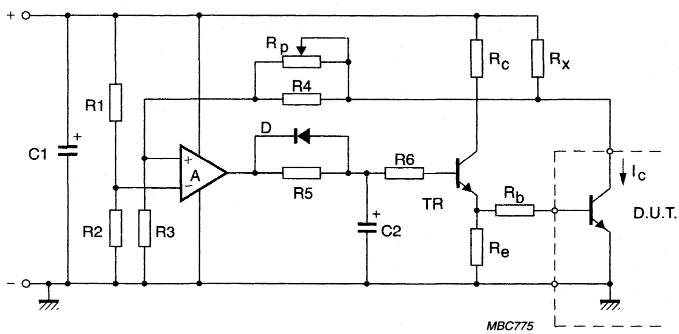


Fig.14 Bias circuit for a class-A linear microwave transistor.

DEVICE DATA

(in alphanumeric sequence)

FEATURES

- 26 V nominal supply voltage
- 16 W output power into a load of 50 Ω with an RF drive power of 25 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 920 to 960 MHz frequency range.

DESCRIPTION

The BGY916 is a three-stage UHF amplifier module in a SOT365A package. It consists of one NPN silicon planar transistor die and two silicon MOS-FET dies mounted on a metallized ceramic AlN substrate, together with matching and bias circuitry.

PINNING - SOT365A

PIN	DESCRIPTION
1	RF input
2	V_{S1}
3	V_{S2}
4	RF output
flange	ground

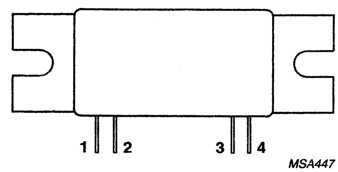


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_{S1}; V_{S2} (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
CW	920 to 960	26	16	≥28	≥35	50

LIMITING VALUES

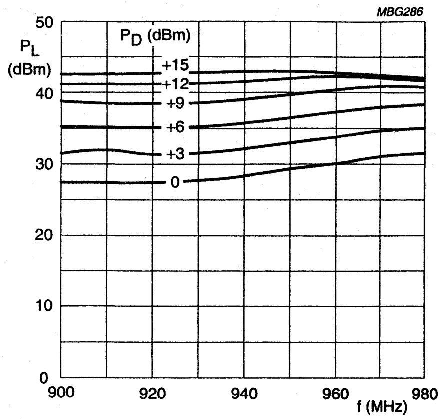
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage	–	28	V
V_{S2}	DC supply voltage	–	28	V
P_D	input drive power	–	80	mW
P_L	load power	–	25	W
T_{stg}	storage temperature	–30	+100	°C
T_{mb}	operating mounting base temperature	–10	+90	°C

CHARACTERISTICS

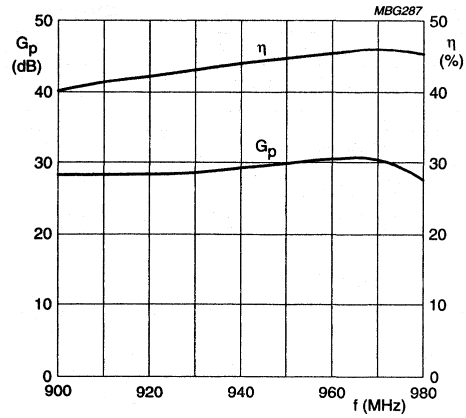
T_{mb} = 25 °C; V_{S1} = V_{S2} = 26 V; P_L = 16 W; Z_S = Z_L = 50 Ω unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency		920	–	960	MHz
I_{S1}	supply current		–	50	–	mA
I_{S2}	supply current	$P_D < -60$ dBm	–	150	–	mA
P_L	load power		16	19	–	W
G_p	power gain		28	30	32	dB
ΔG_p	gain ripple	40 dB dynamic range at f = 920 to 960 MHz	–	1	4	dB
η	efficiency		35	40	–	%
H_2	second harmonic		–	–47	–35	dBc
H_3	third harmonic		–	–55	–45	dBc
$VSWR_{in}$	input VSWR		–	1 : 1.5	2 : 1	
	isolation	V_{S1} = 0	–	–	–40	dBm
	stability	VSWR ≤ 3 : 1 through all phases; V_{S2} = 24 to 28 V	–	–	–60	dBc
	reverse intermodulation	$P_{carrier}$ = 16 W; $P_{interference}$ = 16 μW; $f_i = f_c$ ±600 kHz	–	–68	–65	dBc
F	noise figure		–	5	8	dBc
B	AM bandwidth		2	–	–	MHz
	ruggedness	VSWR ≤ 5 : 1 through all phases	no degradation			



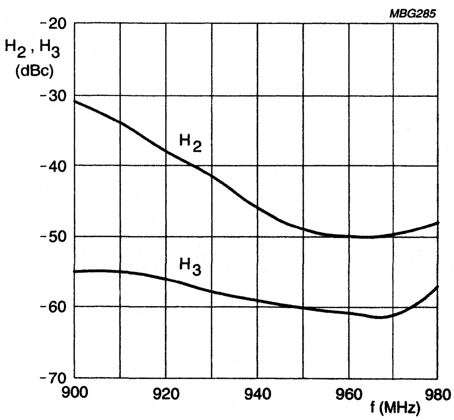
$V_{S1} = V_{S2} = 26$ V; $Z_S = Z_L = 50\ \Omega$; $T_{mb} = 25$ °C.

Fig.2 Load power as a function of frequency; typical values.



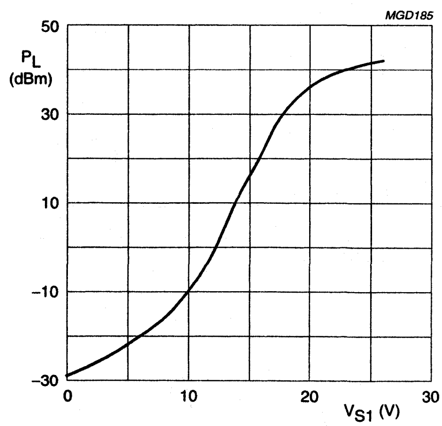
$V_{S1} = V_{S2} = 26$ V; $P_L = 16$ W; $Z_S = Z_L = 50\ \Omega$; $T_{mb} = 25$ °C.

Fig.3 Power gain and efficiency as functions of frequency; typical values.



$V_{S1} = V_{S2} = 26$ V; $P_L = 16$ W; $Z_S = Z_L = 50\ \Omega$; $T_{mb} = 25$ °C.

Fig.4 Harmonics as a function of frequency; typical values.



f = 940 MHz; $V_{S2} = 26$ V; $Z_S = Z_L = 50\ \Omega$; $T_{mb} = 25$ °C.

Fig.5 Load power as a function of supply voltage; typical values.

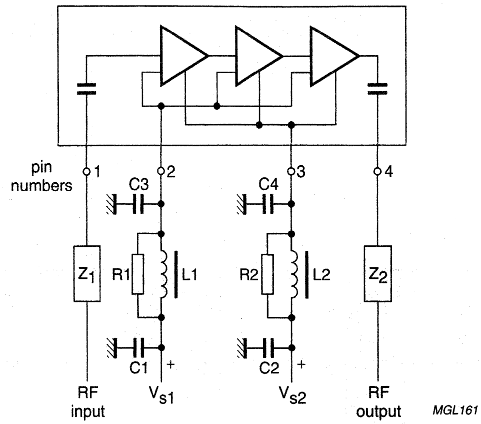


Fig.6 Test circuit.

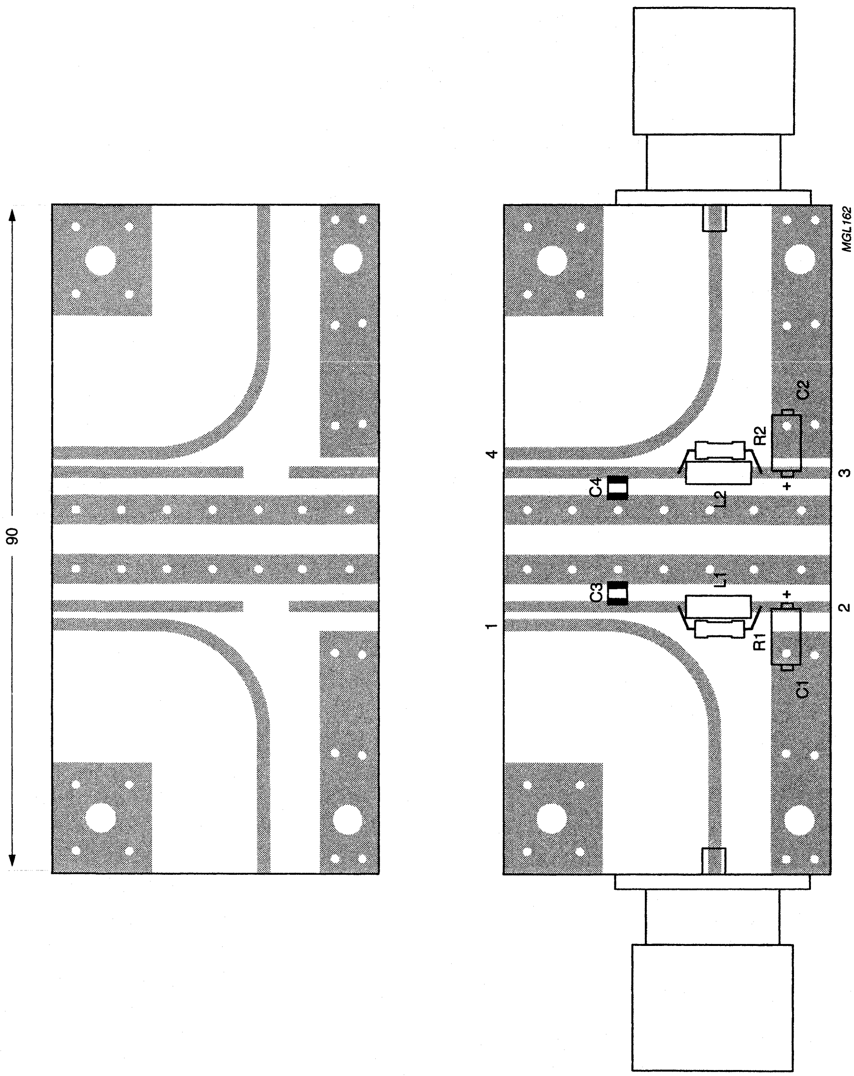


Fig.7 Printed-circuit board component layout.

Dimensions in mm.

List of components (see Figs 6 and 7)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 μF; 35 V	
C3, C4	multilayer ceramic chip capacitor	100 nF; 50 V	
L1, L2	Grade 4S2 Ferroxcube bead		4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline; note 1	50 Ω	–

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stresses when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be used between the mounting base and the heatsink to achieve the best possible contact thermal resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to "finger tight" and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

ESD precautions must be taken to protect the device from electrostatic damage.

UHF amplifier module BGY916/5

FEATURES

- 26 V nominal supply voltage
- 5 V nominal bias voltage
- 16 W output power into a load of 50 Ω with an RF drive power of 25 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 920 to 960 MHz frequency range.

DESCRIPTION

The BGY916/5 is a three-stage UHF amplifier module in a SOT365A package. It consists of one NPN silicon planar transistor die and two silicon MOS-FET dies mounted on a metallized ceramic AlN substrate, together with matching and bias circuitry.

PINNING SOT365A

PIN	DESCRIPTION
1	RF input
2	V_{S1} (bias)
3	V_{S2}
4	RF output
flange	ground

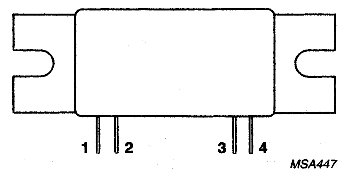


Fig.1 Simplified outline

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_{S1} (V)	V_{S2} (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
CW	920 to 960	5	26	16	≥28	≥35	50

LIMITING VALUES

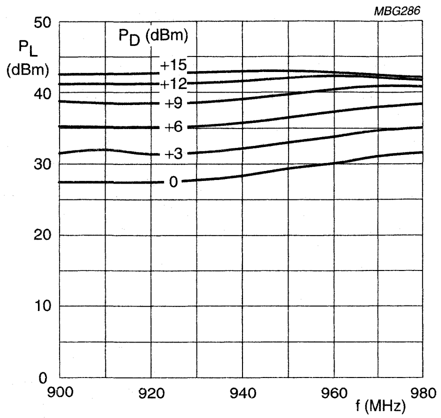
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage	–	5.5	V
V_{S2}	DC supply voltage	–	28	V
P_D	input drive power	–	80	mW
P_L	load power	–	25	W
T_{stg}	storage temperature	–30	+100	°C
T_{mb}	operating mounting base temperature	–10	+90	°C

CHARACTERISTICS

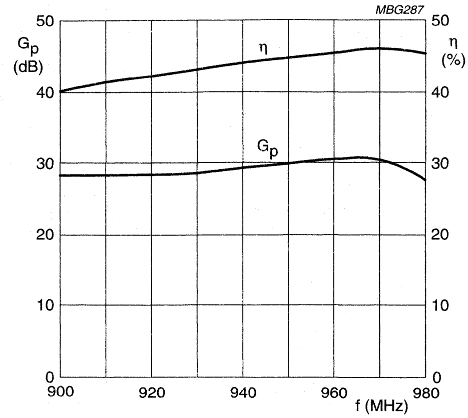
T_{mb} = 25 °C; V_{S1} = 5 V; V_{S2} = 26 V; P_L = 16 W; $Z_S = Z_L$ = 50 Ω unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency		920	–	960	MHz
I_{S1}	supply current		–	50	–	mA
I_{S2}	supply current	P_D < –60 dBm	–	150	–	mA
P_L	load power	P_D = 25 mW (14 dBm)	16	19	–	W
G_p	power gain		28	30	32	dB
ΔG_p	gain ripple	40 dB dynamic range at f = 920 to 960 MHz	–	1	4	dB
η	efficiency		35	40	–	%
H_2	second harmonic		–	–47	–35	dBc
H_3	third harmonic		–	–55	–45	dBc
$VSWR_{in}$	input VSWR		–	1.5 : 1	2 : 1	
	isolation	V_{S1} = 0	–	–	–40	dBm
	stability	VSWR ≤ 3 : 1 through all phases; V_{S2} = 24 to 26 V	–	–	–60	dBc
	reverse intermodulation	$P_{carrier}$ = 16 W; $P_{interference}$ = 16 μW; $f_i = f_c$ ±600 kHz	–	–68	–65	dBc
F	noise figure		–	5	8	dBc
B	AM bandwidth	At 3 dB corner frequency; $P_{carrier}$ = 16 W; modulation = 20 %	2	–	–	MHz
	ruggedness	VSWR ≤ 5 : 1 through all phases	no degradation			



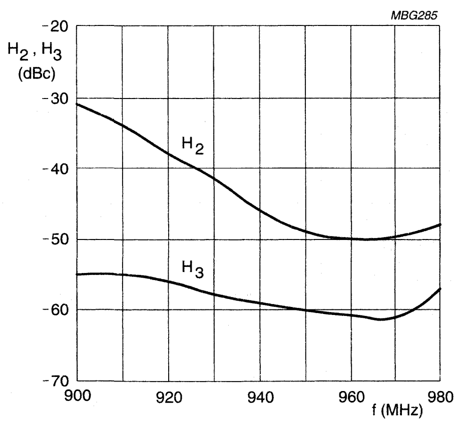
V_{S1} = 5 V; V_{S2} = 26 V; Z_S = Z_L = 50 Ω; T_{mb} = 25 °C.

Fig.2 Load power as a function of frequency; typical values.



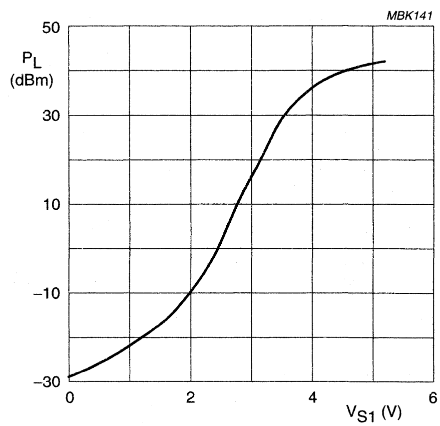
V_{S1} = 5 V; V_{S2} = 26 V; P_L = 16 W; Z_S = Z_L = 50 Ω; T_{mb} = 25 °C.

Fig.3 Power gain and efficiency as functions of frequency; typical values.



V_{S1} = 5 V; V_{S2} = 26 V; P_L = 16 W; Z_S = Z_L = 50 Ω; T_{mb} = 25 °C.

Fig.4 Harmonics as a function of frequency; typical values.



f = 940 MHz; V_{S2} = 26 V; Z_S = Z_L = 50 Ω; T_{mb} = 25 °C.

Fig.5 Load power as a function of supply voltage; typical values.

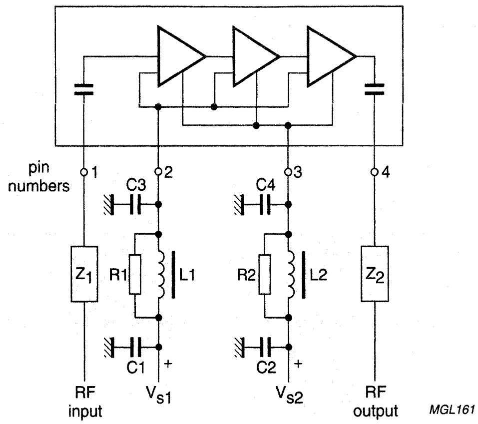
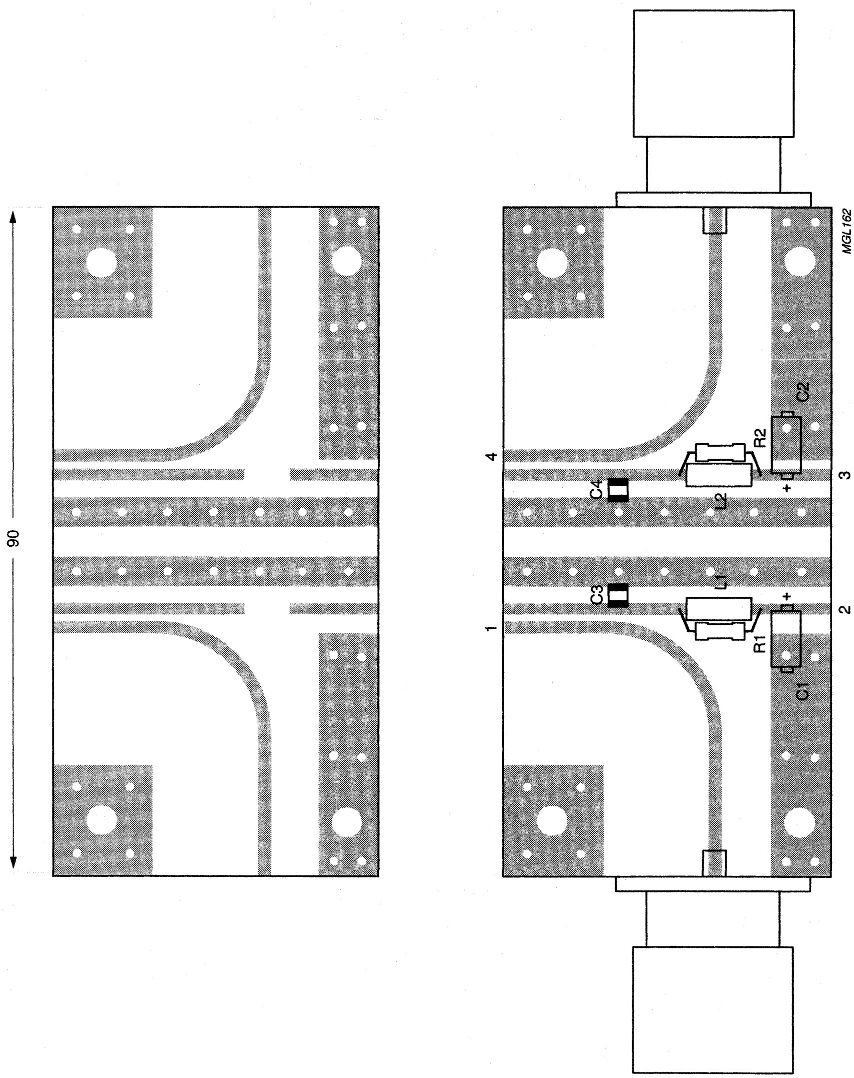


Fig.6 Test circuit.



Dimensions in mm.

Fig.7 Printed-circuit board component layout.

List of components (see Figs 6 and 7)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 μF; 35 V	
C3, C4	multilayer ceramic chip capacitor	100 nF; 50 V	
L1, L2	Grade 4S2 Ferroxcube bead		4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline; note 1	50 Ω	–

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stresses when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be used between the mounting base and the heatsink to achieve the best possible contact thermal resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to “finger tight” and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

ESD precautions must be taken to protect the device from electrostatic damage.

UHF amplifier module BGY925

FEATURES

- 26 V nominal supply voltage
- 23 W output power into a load of 50 Ω with an RF drive power of 36 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 920 to 960 MHz frequency range.

DESCRIPTION

The BGY925 is a three-stage UHF amplifier module in a SOT365A package. It consists of one NPN silicon planar transistor die and two silicon MOSFET dies mounted on a metallized ceramic AlN substrate, together with matching and bias circuitry.

PINNING - SOT365A

PIN	DESCRIPTION
1	RF input
2	V_{S1}
3	V_{S2}
4	RF output
Flange	ground

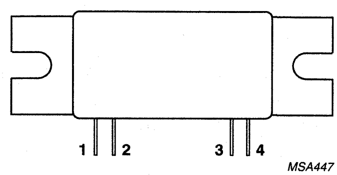


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_{S1}, V_{S2} (V)	P_L (W)	G_p (dB)	η (%) (note 1)	Z_S, Z_L (Ω)
CW	920 to 960	26	23	≥28	≥30	50

Note

1. At P_L = 16 W.

LIMITING VALUES

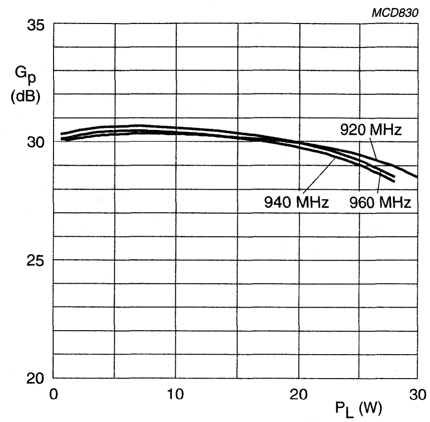
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage	–	28	V
V_{S2}	DC supply voltage	–	28	V
P_D	input drive power	–	80	mW
P_L	load power	–	32	W
T_{stg}	storage temperature	–30	+100	°C
T_{mb}	operating mounting-base temperature	–10	+90	°C

CHARACTERISTICS

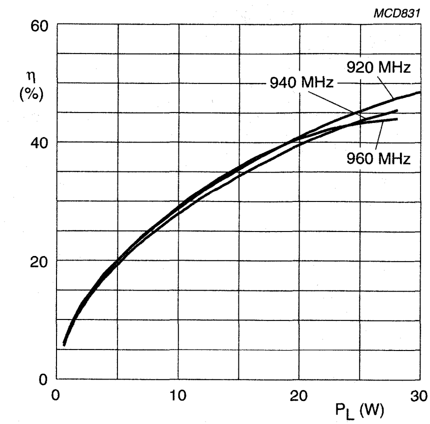
$Z_S = Z_L = 50\ \Omega$; $P_L = 23$ W; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency range		920	–	960	MHz
I_{S1}	supply current		–	50	–	mA
I_{S2}	supply current	$P_D < -60$ dBm	–	500	–	mA
P_L	load power		23	–	–	W
G_p	power gain	160 mW $\leq P_L <$ 2 W	28	30	34	dB
		2 W $\leq P_L \leq$ 23 W	28	30	32	dB
η	efficiency	$P_L = 16$ W	30	–	–	%
H_2	second harmonic	$P_L = 16$ W	–	–	–35	dBc
H_3	third harmonic	$P_L = 16$ W	–	–	–40	dBc
$VSWR_{in}$	input VSWR		–	–	2:1	
	stability	VSWR $\leq$ 3 : 1 through all phases; $V_{S2} = 26$ to 27 V; $P_L = 23$ W	–	–	–60	dBc
	reverse intermodulation	$P_{carrier} = 16$ W; $P_{interference} = 1.6\ \mu$W; $f_i = f_c \pm 600$ kHz	–	–80	–	dBc
	direct intermodulation	$P_{carrier} = 16$ W; $P_{interference} = 1.6$ mW; $f_i = f_c + 270$ kHz	–	–55	–	dBc
NF	noise figure				8	dBc
B	AM bandwidth	corner frequency = 3 dB; $P_{carrier} = 16$ W; modulation = 20%	2	–	–	MHz
	ruggedness	VSWR $\leq$ 5 : 1 through all phases; $V_{S2} = 26$ V; $P_L = 23$ W	no degradation			



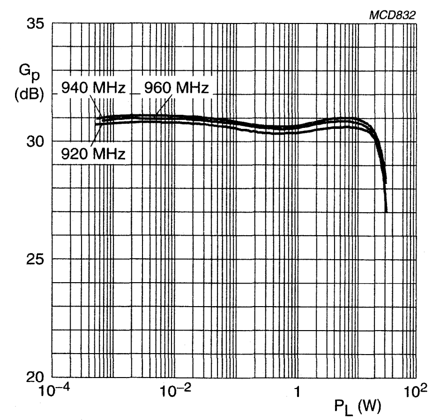
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.2 Power gain as a function of load power; typical values.



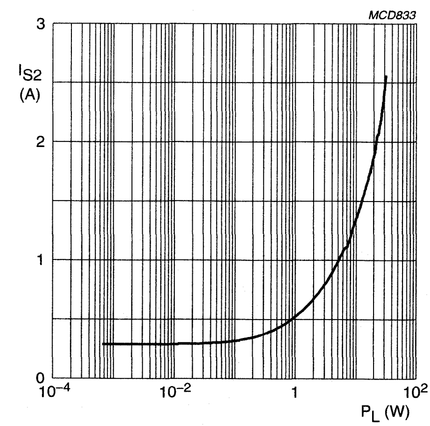
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.3 Efficiency as a function of load power; typical values.



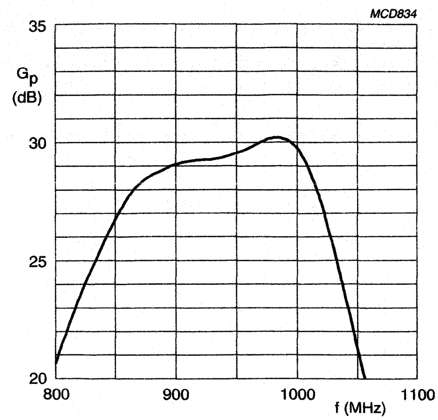
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.4 Power gain as a function of load power; typical values.



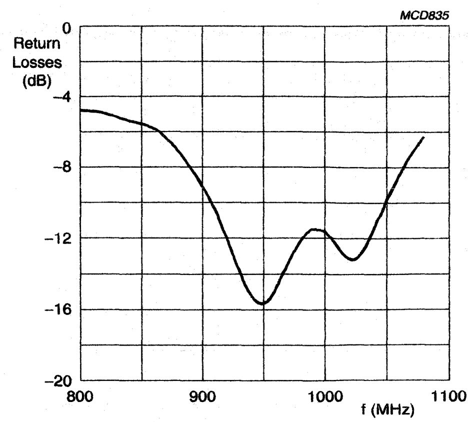
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C;
f = 920 to 960 MHz.

Fig.5 Supply current as a function of load power; typical values.



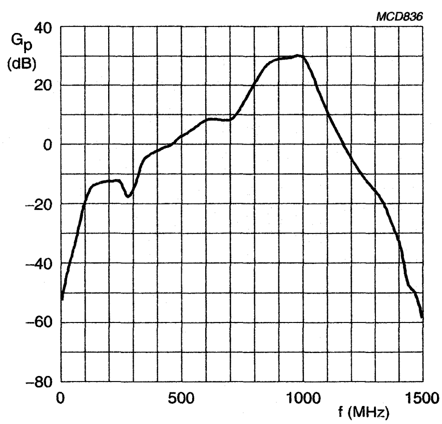
$Z_S = Z_L = 50\ \Omega$; $P_D = -30$ dBm; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.6 Small signal in band power gain as a function of frequency; typical values.



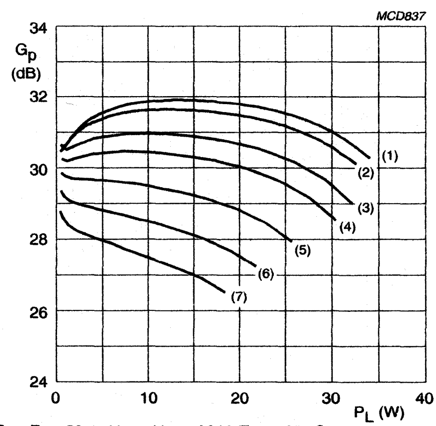
$Z_S = Z_L = 50\ \Omega$; $P_D = -30$ dBm; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.7 Small signal in band input return losses as a function of frequency; typical values.



$Z_S = Z_L = 50\ \Omega$; $V_{S1} = V_{S2} = 26$ V; $P_D = -30$ dBm; $T_{mb} = 25$ °C.

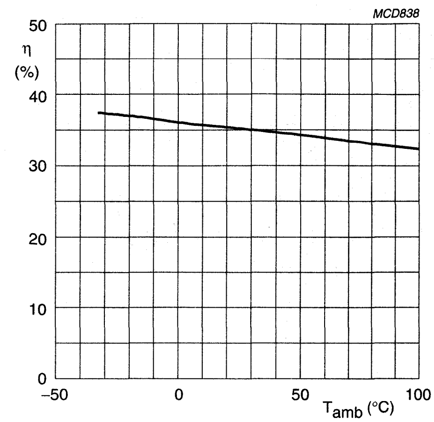
Fig.8 Small signal out band power gain as a function of frequency; typical values.



$Z_S = Z_L = 50\ \Omega$; $V_{S1} = V_{S2} = 26$ V; $T_{mb} = 25$ °C.

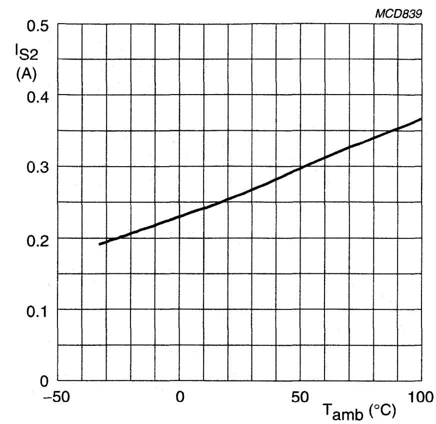
(1) $T_{amb} = -33$°C.
(2) $T_{amb} = -20$°C.
(3) $T_{amb} = 3$°C.
(4) $T_{amb} = 25$°C.
(5) $T_{amb} = 50$°C.
(6) $T_{amb} = 75$°C.
(7) $T_{amb} = 100$°C.

Fig.9 Power gain as a function of load power; typical values



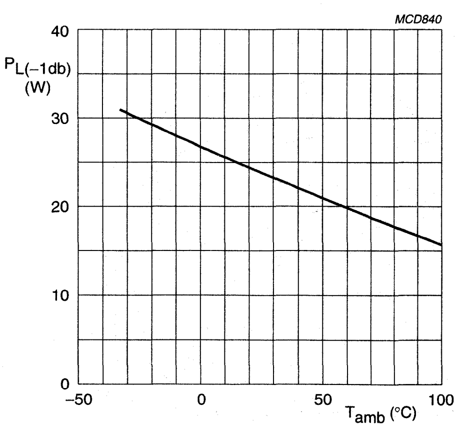
$Z_S = Z_L = 50\ \Omega$; $P_L = 16$ W; $V_{S1} = V_{S2} = 26$ V.

Fig.10 Efficiency as a function of ambient temperature; typical values.



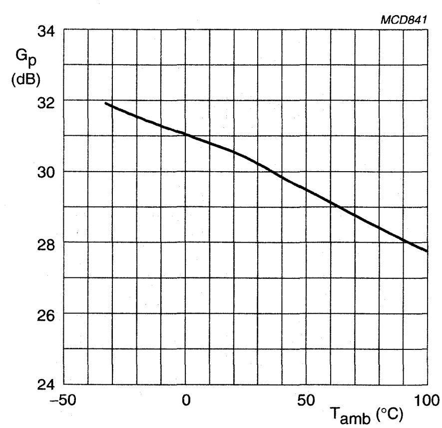
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = V_{S2} = 26$ V; $P_D = 0$.

Fig.11 Quiescent current as a function of ambient temperature; typical values.



$Z_S = Z_L = 50\ \Omega$; $P_{ref} = 5$ W; $V_{S1} = V_{S2} = 26$ V.

Fig.12 Load power at −1 dB gain as a function of ambient temperature; typical values.



$Z_S = Z_L = 50\ \Omega$; $P_L = 5$ W; $V_{S1} = V_{S2} = 26$ V.

Fig.13 Power gain as a function of ambient temperature; typical values.

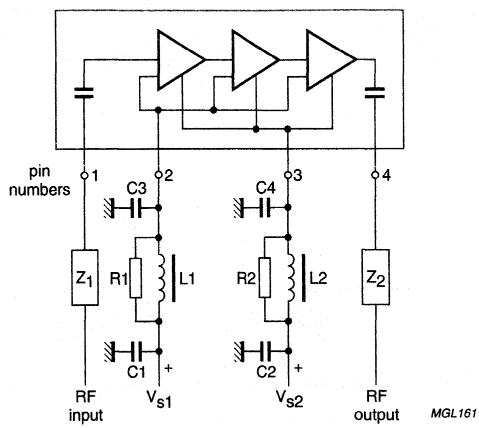
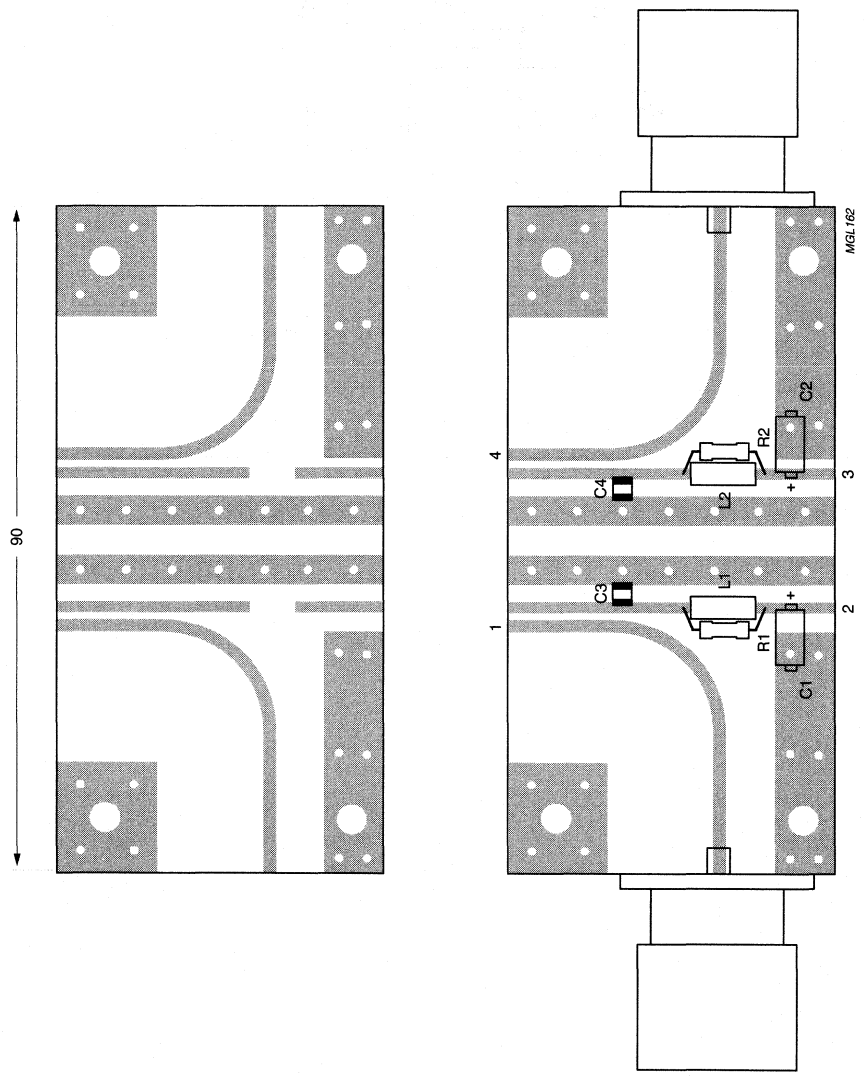


Fig.14 Test circuit.



Dimensions in mm.

Fig.15 Printed-circuit board component layout.

List of components (See Figs 14 and 15)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 μF; 35 V	
C3, C4	multilayer ceramic chip capacitor	100 nF; 50 V	
L1, L2	Grade 4S2 Ferroxcube bead		4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline; note 1	50 Ω	

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stress when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be applied between the mounting base and the heatsink to achieve the best possible thermal contact resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting-base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to “finger tight” and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

ESD precautions must be taken to protect the device from electrostatic damage.

UHF amplifier module — BGY925/5

FEATURES

- 26 V nominal supply voltage
- 23 W output power into a load of 50 Ω with an RF drive power of 36 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 920 to 960 MHz frequency range.

DESCRIPTION

The BGY925/5 is a three-stage UHF amplifier module in a SOT365A package. The module consists of one NPN silicon planar transistor die and two silicon MOSFET dies mounted together with matching and bias circuitry on a metallized ceramic AlN substrate.

PINNING - SOT365A

PIN	DESCRIPTION
1	RF input
2	V_{S1}
3	V_{S2}
4	RF output
Flange	ground

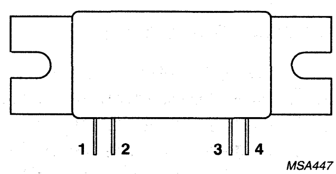


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C, 100 % tested during manufacture.

MODE OF OPERATION	f (MHz)	V_{S1} (V)	V_{S2} (V)	P_L (W)	G_p (dB)	η (%) (note 1)	Z_S, Z_L (Ω)
CW	920 to 960	5	26	23	≥28	≥30	50

Note

1. At P_L = 16 W.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

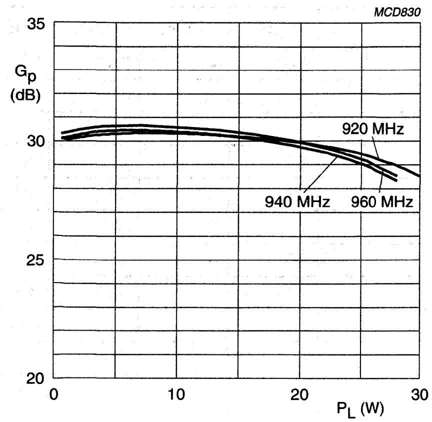
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage	–	5.5	V
V_{S2}	DC supply voltage	–	28	V
P_D	input drive power	–	80	mW
P_L	load power	–	32	W
T_{stg}	storage temperature	–30	+100	°C
T_{mb}	operating mounting-base temperature	–10	+90	°C

UHF amplifier module BGY925/5

CHARACTERISTICS

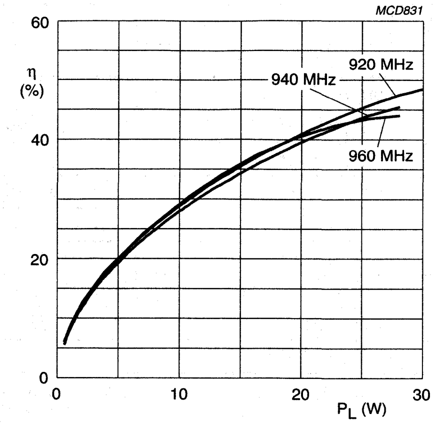
$Z_S = Z_L = 50\ \Omega$; $P_L = 23$ W; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency range		920	–	960	MHz
I_{S1}	supply current		–	50	–	mA
I_{S2}	supply current	$P_D < -60$ dBm	–	500	–	mA
P_L	load power		23	–	–	W
G_p	power gain	160 mW $\leq P_L \leq$ 23 W	28	30	34	dB
		2 W $\leq P_L \leq$ 23 W	28	30	32	dB
η	efficiency	$P_L = 16$ W	30	–	–	%
H_2	second harmonic	$P_L = 16$ W	–	–	−35	dBc
H_3	third harmonic	$P_L = 16$ W	–	–	−40	dBc
$VSWR_{in}$	input VSWR		–	–	2:1	
	stability	VSWR ≤ 3 : 1 through all phases; $V_{S2} = 26$ to 27 V; $P_L = 23$ W	–	–	−60	dBc
	reverse intermodulation	$P_{carrier} = 16$ W; $P_{interference} = 1.6\ \mu$W; $f_i = f_c \pm 600$ kHz	–	−80	–	dBc
	direct intermodulation	$P_{carrier} = 16$ W; $P_{interference} = 1.6$ mW; $f_i = f_c + 270$ kHz	–	−55	–	dBc
NF	noise figure		–	–	8	dBc
B	AM bandwidth	corner frequency = 3 dB; $P_{carrier} = 16$ W; modulation = 20%	2	–	–	MHz
	ruggedness	VSWR ≤ 5 : 1 through all phases; $V_{S2} = 26$ V; $P_L = 23$ W	no degradation			



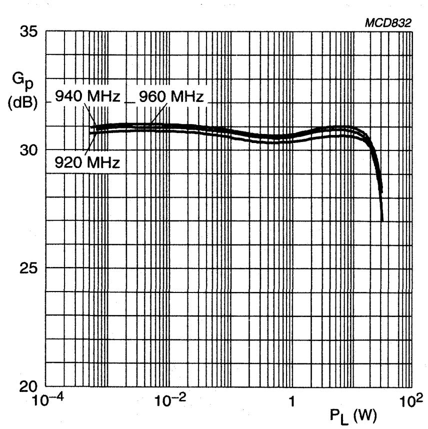
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.2 Power gain as a function of load power; typical values.



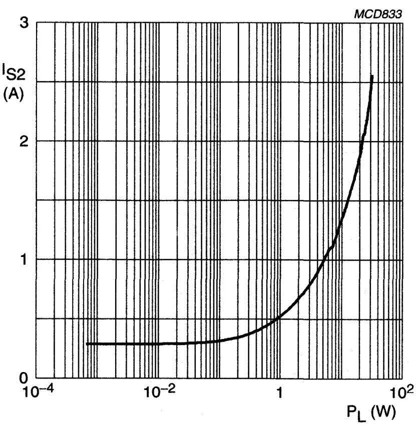
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.3 Efficiency as a function of load power; typical values.



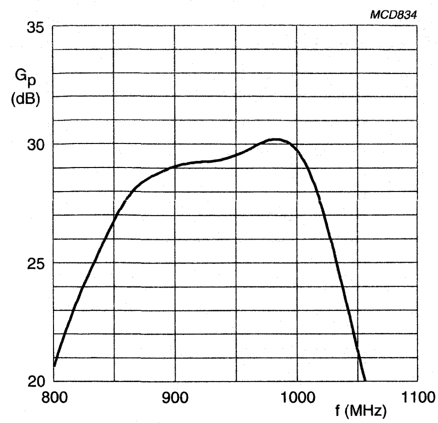
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.4 Power gain as a function of load power; typical values.



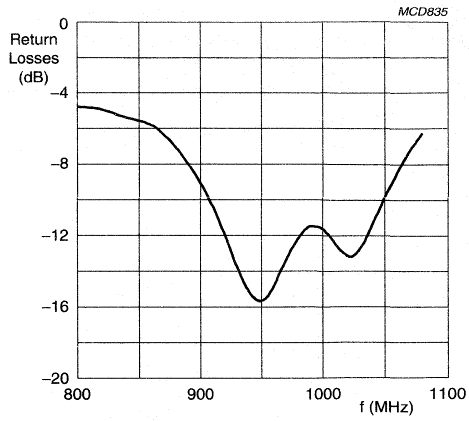
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C;
f = 920 to 960 MHz.

Fig.5 Supply current as a function of load power; typical values.



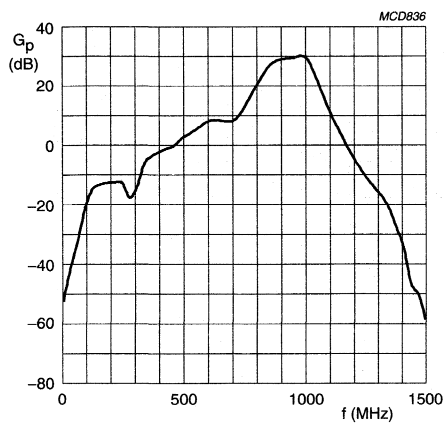
$Z_S = Z_L = 50\ \Omega$; $P_D = -30$ dBm; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.6 Small signal in band power gain as a function of frequency; typical values.



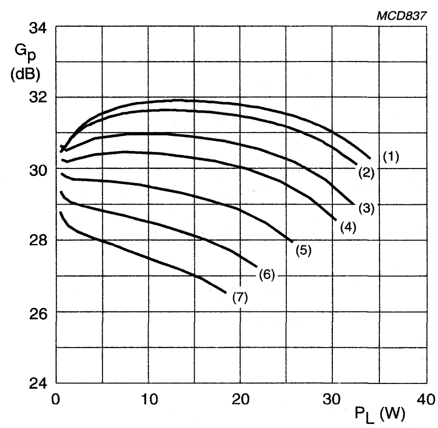
$Z_S = Z_L = 50\ \Omega$; $P_D = -30$ dBm; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C.

Fig.7 Small signal in band input return losses as a function of frequency; typical values.



$Z_S = Z_L = 50\ \Omega$; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $P_D = -30$ dBm; $T_{mb} = 25$ °C.

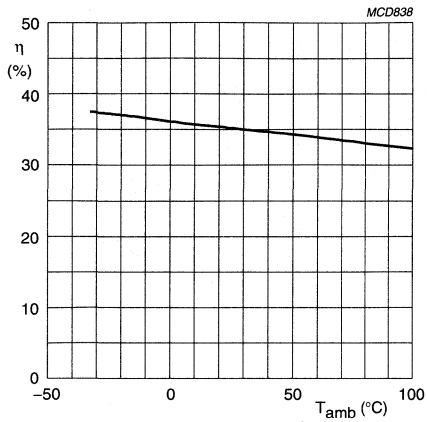
Fig.8 Small signal out band power gain as a function frequency; typical values.



$Z_S = Z_L = 50\ \Omega$; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $T_{mb} = 25$ °C.

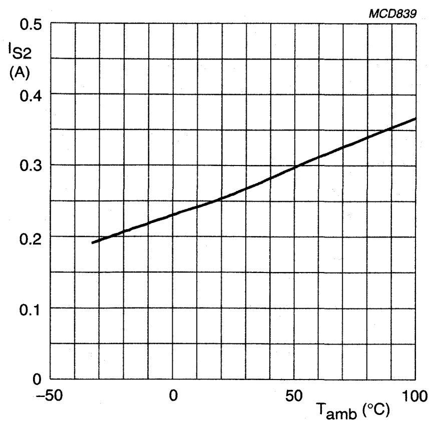
(1) $T_{amb} = -33$°C.
(2) $T_{amb} = -20$°C.
(3) $T_{amb} = 3$°C.
(4) $T_{amb} = 25$°C.
(5) $T_{amb} = 50$°C.
(6) $T_{amb} = 75$°C.
(7) $T_{amb} = 100$°C.

Fig.9 Power gain as a function of load power; typical values



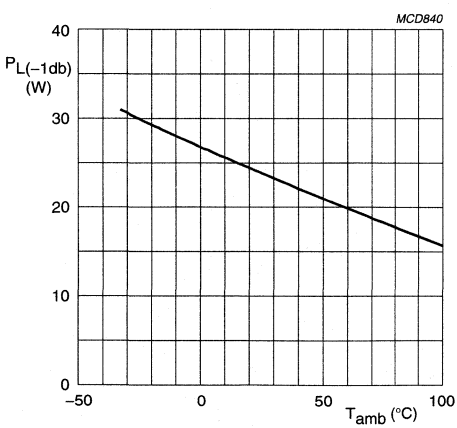
$Z_S = Z_L = 50\ \Omega$; $P_L = 16$ W; $V_{S1} = 5$ V; $V_{S2} = 26$ V.

Fig.10 Efficiency as a function of ambient temperature; typical values.



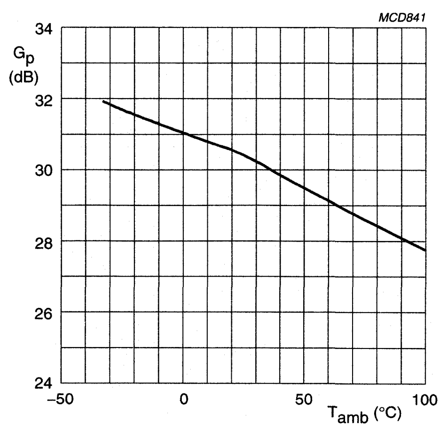
$Z_S = Z_L = 50\ \Omega$; $V_{S1} = 5$ V; $V_{S2} = 26$ V; $P_D = 0$.

Fig.11 Quiescent current as a function of ambient temperature; typical values.



$Z_S = Z_L = 50\ \Omega$; $P_{ref} = 5$ W; $V_{S1} = 5$ V; $V_{S2} = 26$ V.

Fig.12 Load power at −1 dB gain as a function of ambient temperature; typical values.



$Z_S = Z_L = 50\ \Omega$; $P_L = 5$ W; $V_{S1} = 5$ V; $V_{S2} = 26$ V.

Fig.13 Power gain as a function of ambient temperature; typical values.

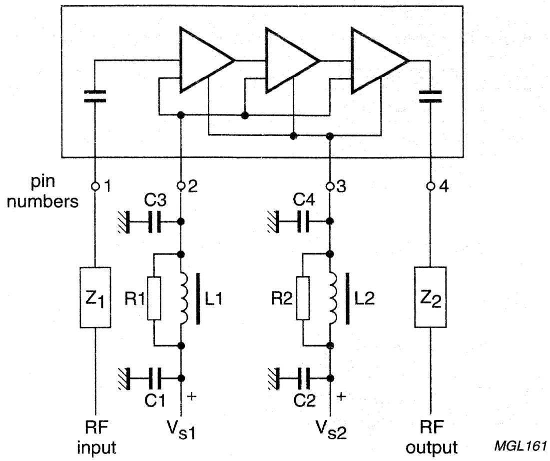
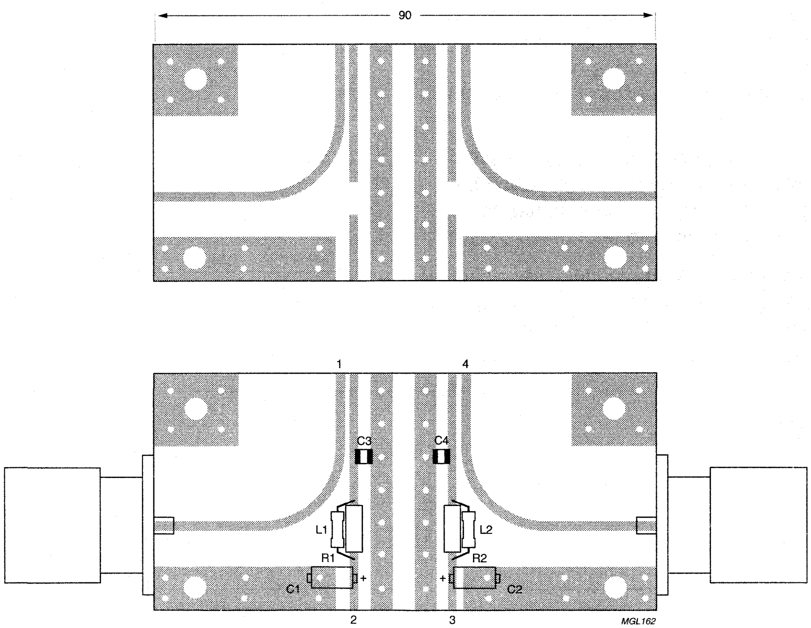


Fig.14 Test circuit.



Dimensions in mm.

Fig.15 Printed-circuit board component layout.

List of components (See Figs 14 and 15)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 μF; 35 V	
C3, C4	multilayer ceramic chip capacitor	100 nF; 50 V	
L1, L2	Grade 4S2 Ferroxcube bead		4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline; note 1	50 Ω	

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stress when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be applied between the mounting base and the heatsink to achieve the best possible thermal contact resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting-base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to “finger tight” and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

ESD precautions must be taken to protect the device from electrostatic damage.

UHF amplifier module BGY1816

FEATURES

- 26 V nominal supply voltage
- 16 W output power into a load of 50 Ω with an RF drive power of ≤63 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 1805 to 1880 MHz frequency band.

DESCRIPTION

The BGY1816 is a three-stage UHF amplifier module in a SOT365A package with a plastic cap. It consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic AlN substrate.

PINNING - SOT365A

PIN	DESCRIPTION
1	RF input
2	V_{S1}
3	V_{S2}
4	RF output
Flange	ground

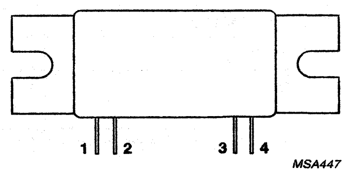


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_{S1} (V)	V_{S2} (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
CW	1805 to 1880	5	26	≥16	≥24	≥30	50

LIMITING VALUES

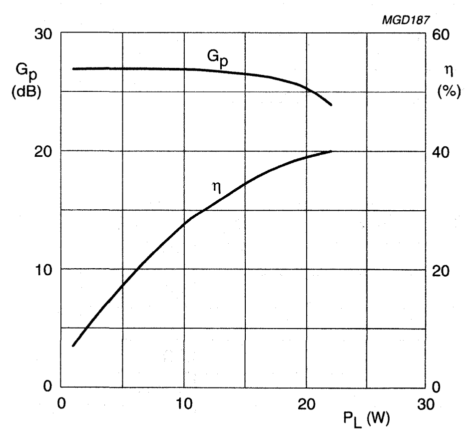
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage		4.5	5.5	V
V_{S2}	DC supply voltage		–	28	V
P_D	input drive power		–	120	mW
P_L	load power	T_{mb} = 25 °C	–	20	W
T_{stg}	storage temperature		–30	+100	°C
T_{mb}	operating mounting base temperature		–10	+90	°C

CHARACTERISTICS

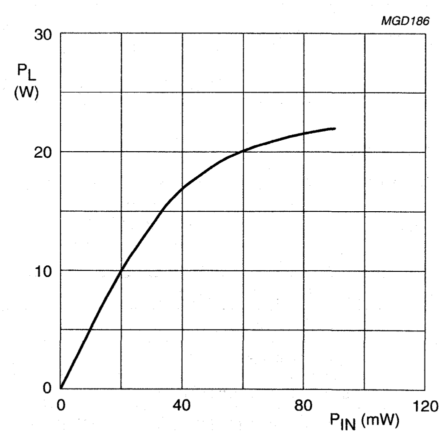
T_{mb} = 25 °C; V_{S1} = 5 V; V_{S2} = 26 V; P_L = 16 W; Z_S = Z_L = 50 Ω unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency		1805	–	1880	MHz
I_{S1}	supply current		–	80	–	mA
I_{S2}	supply current	P_D < −60 dBm	–	430	–	mA
P_L	load power	P_D < 63 mW	16	–	–	W
G_p	power gain		24	–	28	dB
η	efficiency		30	–	–	%
H_2	second harmonic		–	–	−35	dBc
H_3	third harmonic		–	–	−40	dBc
$VSWR_{in}$	input VSWR		–	–	1.6 : 1	
	stability	VSWR ≤ 2 : 1 through all phases; P_L ≤ 16 W; V_{S2} = 25 to 27 V	–	–	−60	dBc
	reverse intermodulation	$P_{carrier}$ = 16 W; $P_{reverse}$ = −40 dBc; f_i = f_c ±200 kHz	–	–	−53	dBc
B	AM bandwidth	corner frequency = 3 dB; $P_{carrier}$ = 16 W; modulation = 20%	2	–	–	MHz
	ruggedness	VSWR ≤ 5 : 1 through all phases	no degradation			



f = 1850 MHz; V_{S1} = 5 V; V_{S2} = 26 V; Z_S = Z_L = 50 Ω; T_{mb} = 25 °C.

Fig.2 Power gain and efficiency as functions of load power; typical values.



f = 1850 MHz; V_{S1} = 5 V; V_{S2} = 26 V; Z_S = Z_L = 50 Ω; T_{mb} = 25 °C.

Fig.3 Load power as a function of input power; typical values.

APPLICATION INFORMATION

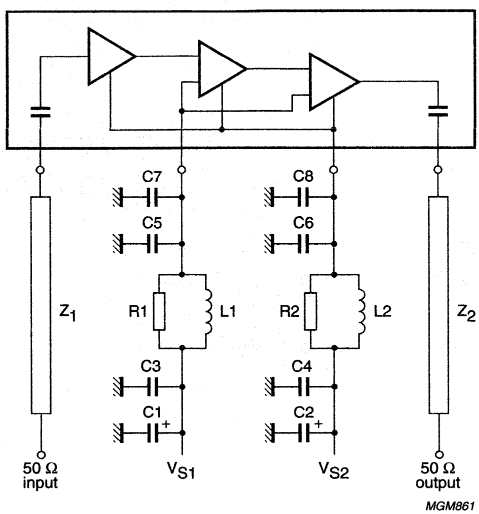


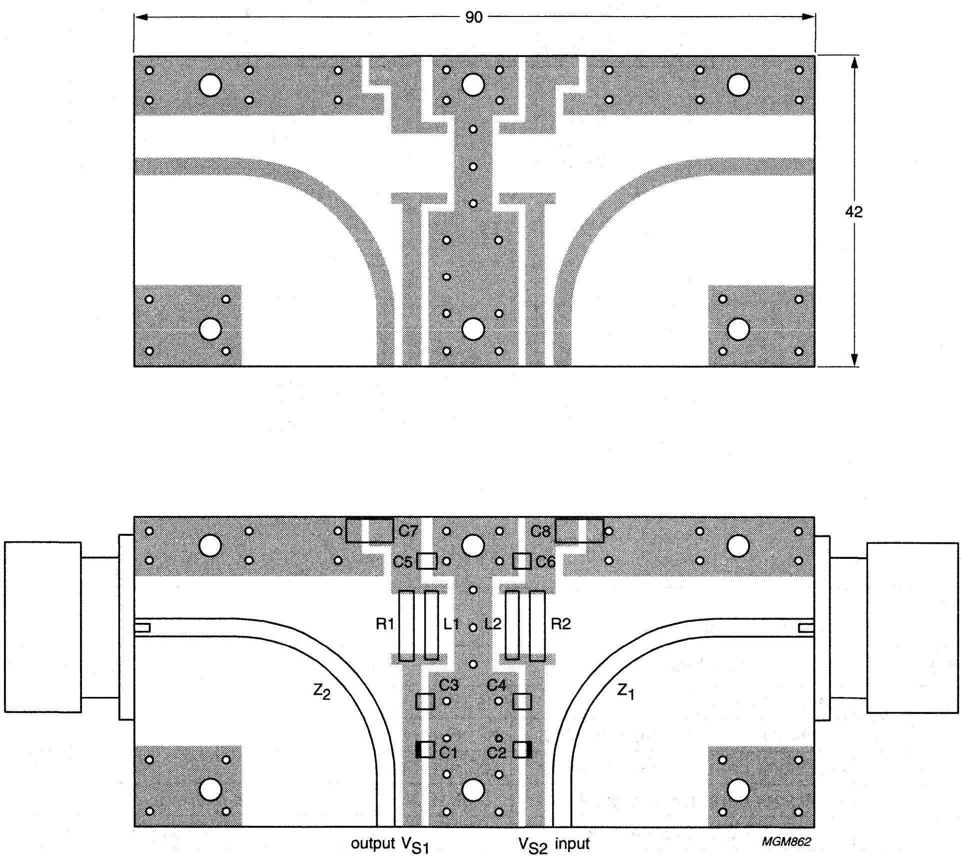
Fig.4 Test circuit.

List of components (see Figs 4 and 5)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 μF; 35 V	
C3, C4	multilayer ceramic chip capacitor	10 nF; 50 V	
C5, C6	multilayer ceramic chip capacitor	100 pF; 50 V	
C7, C8	multilayer ceramic chip capacitor	10 pF; 50 V	
L1, L2	Grade 4S2 Ferroxcube bead		4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline: note 1	50 Ω	

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.



Dimensions in mm.

Fig.5 Printed-circuit board component layout.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stress when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be applied between the mounting base and the heatsink to achieve the best possible thermal contact resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to “finger tight” and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

ESD precautions must be taken to protect the device from electrostatic damage.

UHF amplifier module BGY1816S

FEATURES

- 26 V nominal supply voltage
- 16 W output power into a load of 50 Ω with an RF drive power of ≤20 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 1805 to 1880 MHz frequency band.

DESCRIPTION

The BGY1816S is a three-stage UHF amplifier module in a SOT501A package with a plastic cap. It consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic AlN substrate.

PINNING - SOT501A

PIN	DESCRIPTION
1	RF input
2	V_{S1}
3	V_{S2}
4	RF output
Flange	ground

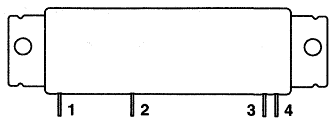


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_{S1} (V)	V_{S2} (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
CW	1805 to 1880	5	26	≥16	≥29	≥30	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage		4.5	5.5	V
V_{S2}	DC supply voltage		–	28	V
P_D	input drive power		–	120	mW
P_L	load power	T_{mb} = 25 °C	–	20	W
T_{stg}	storage temperature		–30	+100	°C
T_{mb}	operating mounting base temperature		–10	+90	°C

CHARACTERISTICS

T_{mb} = 25 °C; V_{S1} = 5 V; V_{S2} = 26 V; P_L = 16 W; Z_S = Z_L = 50 Ω unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency		1805	–	1880	MHz
I_{S1}	supply current		–	80	–	mA
I_{S2}	supply current	P_D < −60 dBm	–	430	–	mA
P_L	load power	P_D < 20 mW	16	–	–	W
G_p	power gain		29	–	–	dB
η	efficiency		30	–	–	%
H_2	second harmonic		–	–	−35	dBc
H_3	third harmonic		–	–	−40	dBc
$VSWR_{in}$	input VSWR		–	–	2 : 1	
	stability	VSWR ≤ 2 : 1 through all phases; P_L ≤ 16 W; V_{S2} = 25 to 27 V	–	–	−60	dBc
	reverse intermodulation	$P_{carrier}$ = 16 W; $P_{reverse}$ = −40 dBc; $f_i = f_c$ ±200 kHz	–	–	−53	dBc
B	AM bandwidth	corner frequency = 3 dB; $P_{carrier}$ = 16 W; modulation = 20%	2	–	–	MHz
	ruggedness	VSWR ≤ 5 : 1 through all phases	no degradation			

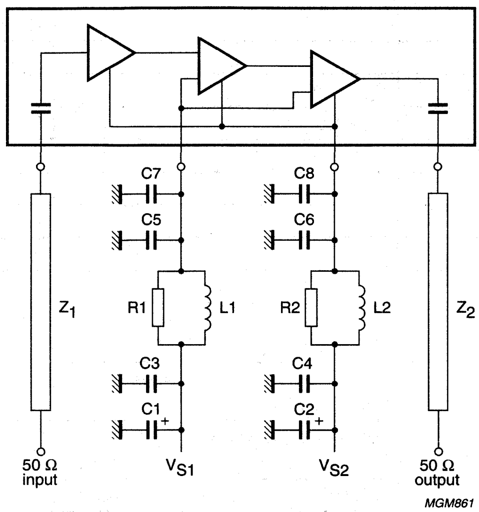


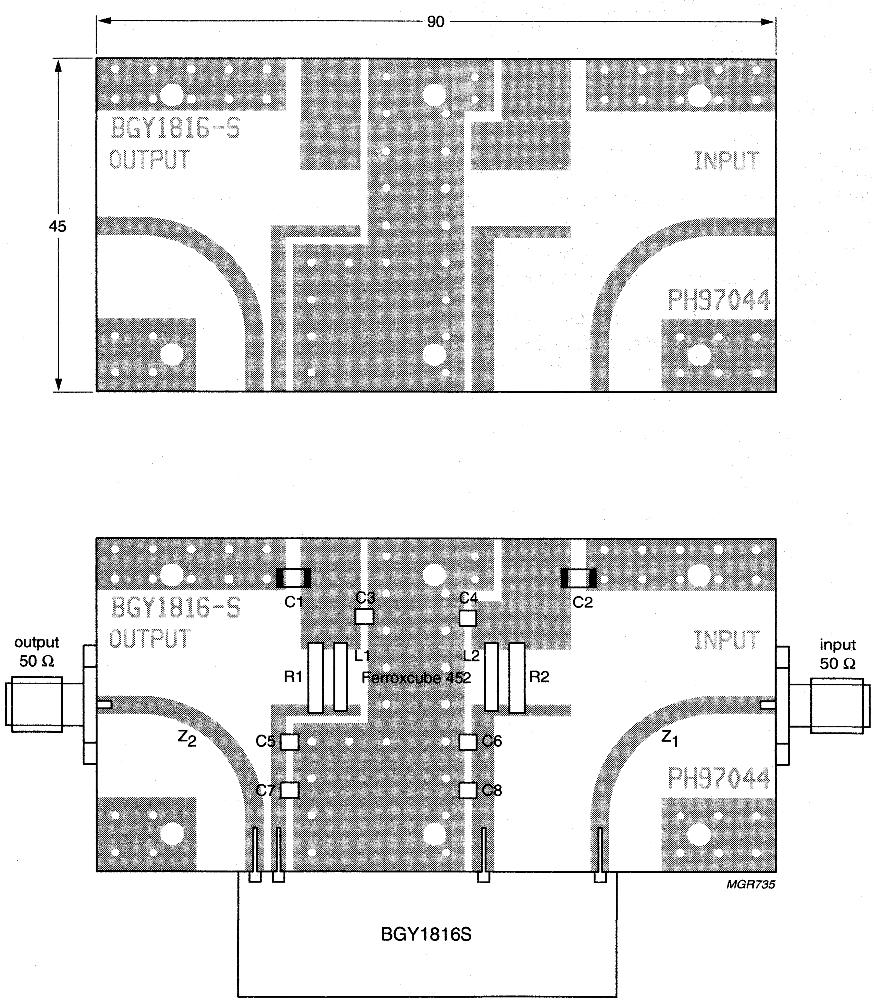
Fig.2 Test circuit.

List of components (see Figs 2 and 3)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 μF; 35 V	
C3, C4	multilayer ceramic chip capacitor	10 nF; 50 V	
C5, C6	multilayer ceramic chip capacitor	100 pF; 50 V	
C7, C8	multilayer ceramic chip capacitor	10 pF; 50 V	
L1, L2	Grade 4S2 Ferroxcube bead		4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline; note 1	50 Ω	–

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.



Dimensions in mm.

Fig.3 Printed-circuit board component layout.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stress when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be applied between the mounting base and the heatsink to achieve the best possible thermal contact resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to "finger tight" and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

ESD precautions must be taken to protect the device from electrostatic damage.

FEATURES

- 26 V nominal supply voltage
- 16 W output power into a load of 50 Ω with an RF drive power of ≤63 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 1930 to 1990 MHz frequency band.

DESCRIPTION

The BGY1916 is a three-stage UHF amplifier module in a SOT365A package with a plastic cap. It consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic AlN substrate.

PINNING - SOT365A

PIN	DESCRIPTION
1	RF input
2	V_{S1}
3	V_{S2}
4	RF output
Flange	ground

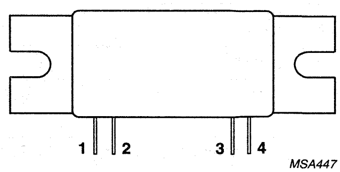


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_{S1} (V)	V_{S2} (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
CW	1930 to 1990	5	26	≥16	≥24	≥30	50

LIMITING VALUES

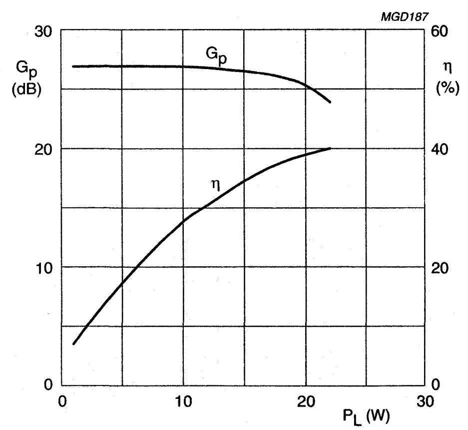
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage		4.5	5.5	V
V_{S2}	DC supply voltage		–	28	V
P_D	input drive power		–	120	mW
P_L	load power	T_{mb} = 25 °C	–	20	W
T_{stg}	storage temperature		–30	+100	°C
T_{mb}	operating mounting base temperature		–10	+90	°C

CHARACTERISTICS

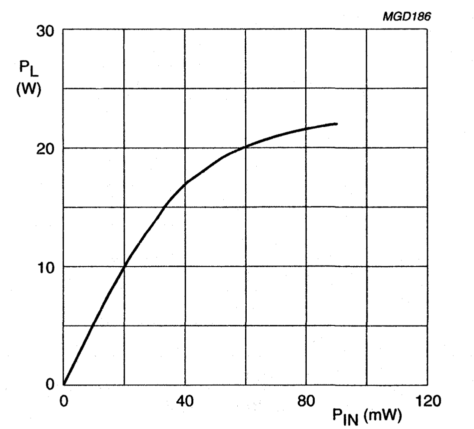
T_{mb} = 25 °C; V_{S1} = 5 V; V_{S2} = 26 V; P_L = 16 W; $Z_S = Z_L$ = 50 Ω unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency		1930	–	1990	MHz
I_{S1}	supply current		–	80	–	mA
I_{S2}	supply current	$P_D < -60$ dBm	–	430	–	mA
P_L	load power	$P_D < 63$ mW	16	–	–	W
G_p	power gain		24	–	28	dB
η	efficiency		30	–	–	%
H_2	second harmonic		–	–	–35	dBc
H_3	third harmonic		–	–	–45	dBc
$VSWR_{in}$	input VSWR		–	–	1.6 : 1	
	stability	VSWR ≤ 2 : 1 through all phases; $P_L \leq 16$ W; V_{S2} = 25 to 27 V	–	–	–60	dBc
	reverse intermodulation	$P_{carrier}$ = 16 W; $P_{reverse}$ = –40 dBc; $f_i = f_c$ ±200 kHz	–	–	–53	dBc
B	AM bandwidth	corner frequency = 3 dB; $P_{carrier}$ = 16 W; modulation = 20%	2	–	–	MHz
	ruggedness	VSWR ≤ 5 : 1 through all phases	no degradation			



f = 1960 MHz; V_{S1} = 5 V; V_{S2} = 26 V; $Z_S = Z_L$ = 50 Ω; T_{mb} = 25 °C.

Fig.2 Power gain and efficiency as functions of load power; typical values.



f = 1960 MHz; V_{S1} = 5 V; V_{S2} = 26 V; $Z_S = Z_L$ = 50 Ω; T_{mb} = 25 °C.

Fig.3 Load power as a function of input power; typical values.

APPLICATION INFORMATION

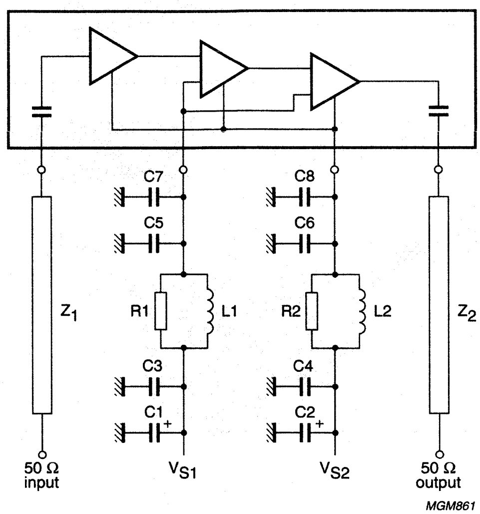


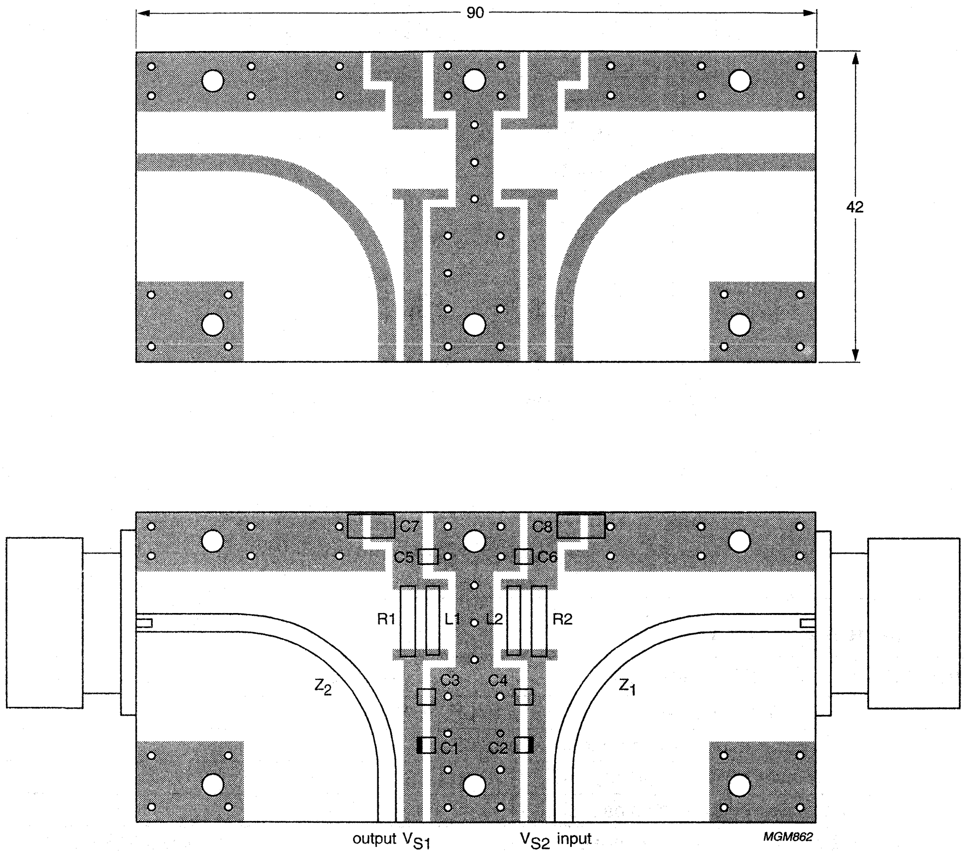
Fig.4 Test circuit.

List of components (see Figs 4 and 5)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 µF; 35 V	
C3, C4	multilayer ceramic chip capacitor	10 nF; 50 V	
C5, C6	multilayer ceramic chip capacitor	100 pF; 50 V	
C7, C8	multilayer ceramic chip capacitor	10 pF; 50 V	
L1, L2	Grade 4S2 Ferroxcube bead		4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline: note 1	50 Ω	

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.



Dimensions in mm.

Fig.5 Printed-circuit board component layout.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stress when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be applied between the mounting base and the heatsink to achieve the best possible thermal contact resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to "finger tight" and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once the module is mounted on the heatsink, the leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

Precautions must be taken to protect the device from electrostatic damage (ESD).

UHF amplifier module BGY2016

FEATURES

- 26 V nominal supply voltage
- 16 W output power into a load of 50 Ω with an RF drive power of ≤20 mW.

APPLICATIONS

- Base station transmitting equipment operating in the 1805 to 1990 MHz frequency band.

DESCRIPTION

The BGY2016 is a three-stage UHF amplifier module in a SOT365A package with a plastic cap. It consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic AlN substrate.

PINNING - SOT365A

PIN	DESCRIPTION
1	RF input
2	V_{S1}
3	V_{S2}
4	RF output
Flange	ground

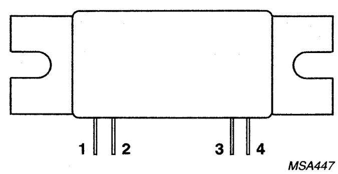


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_{S1} (V)	V_{S2} (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
CW	1805 to 1990	5	26	≥16	≥28	≥30	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{S1}	DC supply voltage		4.5	5.5	V
V_{S2}	DC supply voltage		–	28	V
P_D	input drive power		–	120	mW
P_L	load power	T_{mb} = 25 °C	–	20	W
T_{stg}	storage temperature		–30	+100	°C
T_{mb}	operating mounting base temperature		–10	+90	°C

CHARACTERISTICS

T_{mb} = 25 °C; V_{S1} = 5 V; V_{S2} = 26 V; P_L = 16 W; $Z_S = Z_L$ = 50 Ω unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency		1805	–	1990	MHz
I_{S1}	supply current		–	80	–	mA
I_{S2}	supply current	$P_D < -60$ dBm	–	430	–	mA
P_L	load power	$P_D < 20$ mW	16	–	–	W
G_p	power gain		28	–	35	dB
ΔG_p	in band gain variation	f = 1805 to 1880 MHz; P_L = 5 W	–	–	2	dB
		f = 1930 to 1990 MHz; P_L = 5 W	–	–	2	dB
$\lvert G_{p1} - G_{p2} \rvert$	gain expansion	G_{p1} at P_L = 160 mW; G_{p2} at P_L = 5 mW	–	–	±1	dB
η	efficiency	P_L = 16 W	30	–	–	%
H_2	second harmonic	P_L = 16 W	–	–	–35	dBc
H_3	third harmonic	P_L = 16 W	–	–	–40	dBc
$VSWR_{in}$	input VSWR		–	–	2 : 1	
	stability	VSWR ≤ 2 : 1 through all phases; $P_L \leq 16$ W; V_{S2} = 25 to 27 V	–	–	–60	dBc
	reverse intermodulation	$P_{carrier}$ = 16 W; $P_{reverse}$ = –40 dBc; $f_i = f_c$ ±200 kHz	–	–	–53	dBc
B	AM bandwidth	corner frequency = 3 dB; $P_{carrier}$ = 16 W; modulation = 20%	2	–	–	MHz
	ruggedness	VSWR ≤ 5 : 1 through all phases	no degradation			

APPLICATION INFORMATION

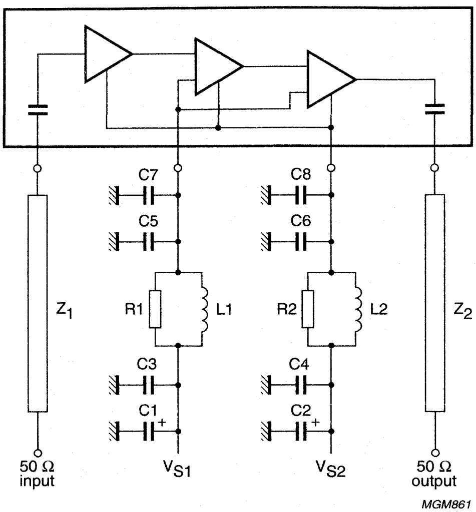


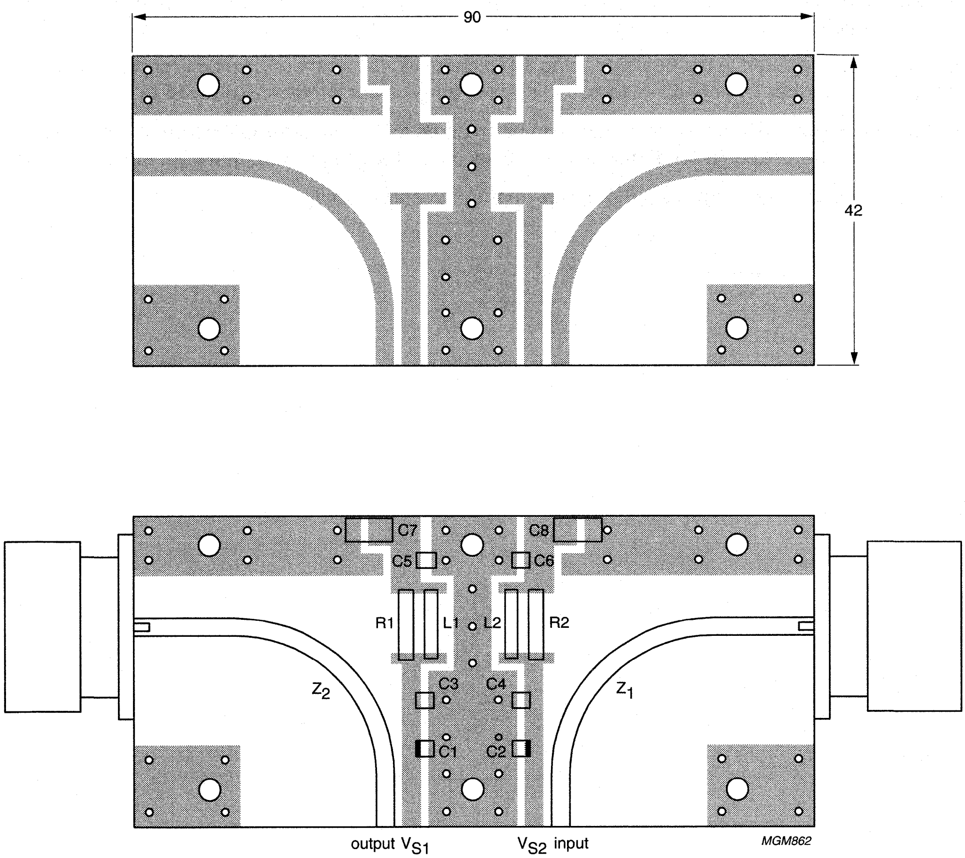
Fig.2 Test circuit.

List of components (See Figs 2 and 3)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	electrolytic capacitor	10 μF; 35 V	–
C3, C4	multilayer ceramic chip capacitor	10 nF; 50 V	–
C5, C6	multilayer ceramic chip capacitor	100 pF; 50 V	–
C7, C8	multilayer ceramic chip capacitor	10 pF; 50 V	–
L1, L2	Grade 4S2 Ferroxcube bead	–	4330 030 36300
R1, R2	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline; note 1	50 Ω	–

Note

1. The striplines are on a double copper-clad printed-circuit board with epoxy dielectric (ε_r = 4.5); thickness = 1 mm.



Dimensions in mm.

Fig.3 Printed-circuit board component layout.

MOUNTING RECOMMENDATIONS

To ensure a good thermal contact and to prevent mechanical stress when bolted down, the flatness of the mounting base is designed to be typically better than 0.1 mm. The mounting area of the heatsink should be flat and free from burrs and loose particles. The heatsink should be rigid and not prone to bowing under thermal cycling conditions. The thickness of a solid heatsink should be not less than 5 mm to ensure a rigid assembly.

A thin, even layer of thermal compound should be applied between the mounting base and the heatsink to achieve the best possible thermal contact resistance. Excessive use of thermal compound will result in an increase in thermal resistance and possible bowing of the mounting base; too little will also result in poor thermal conduction.

The module should be mounted to the heatsink using 3 mm bolts with flat washers. The bolts should first be tightened to “finger tight” and then further tightened in alternating steps to a maximum torque of 0.4 to 0.6 Nm.

Once mounted on the heatsink, the module leads can be soldered to the printed-circuit board. A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds at a distance of 2 mm from the plastic cap.

ESD precautions must be taken to protect the device from electrostatic damage.

HF power MOS transistor BLF145

FEATURES

- High power gain
- Low noise figure
- Good thermal stability
- Withstands full load mismatch.

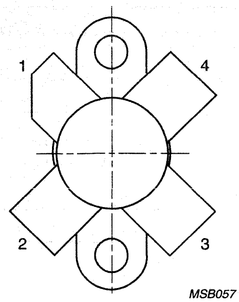
DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for SSB transmitter applications in the HF frequency range. The transistor is encapsulated in a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange. Matched gate-source voltage (V_{GS}) groups are available on request.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION



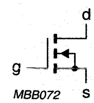


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	P_L (W)	G_p (dB)	η_D (%) (note 1)	d_3 (dB)
SSB, class-A	28	28	1.3	8 (PEP)	> 24	–	< –40
SSB, class-AB	28	28	–	30 (PEP)	typ. 20	typ. 40	typ. –35

Note

1. 2-tone efficiency.

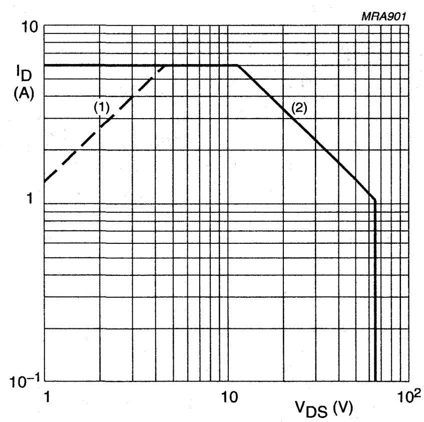
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	6	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

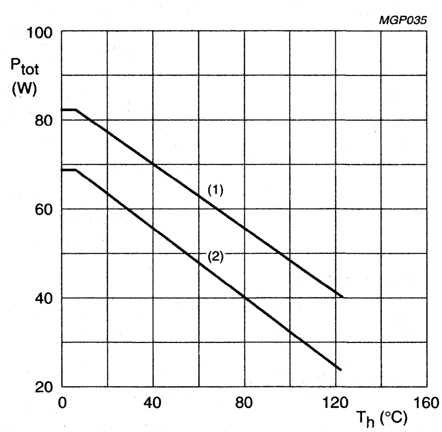
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



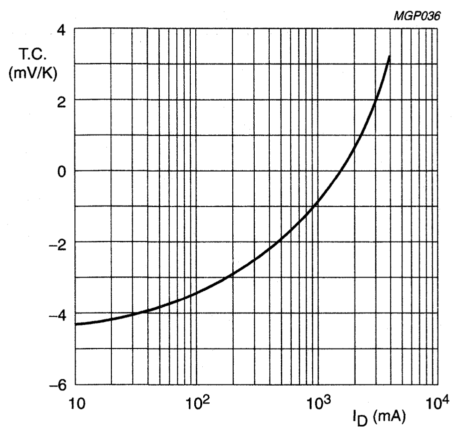
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

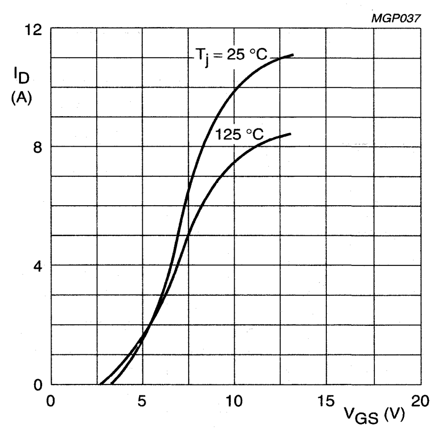
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	–	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	7	–	pF



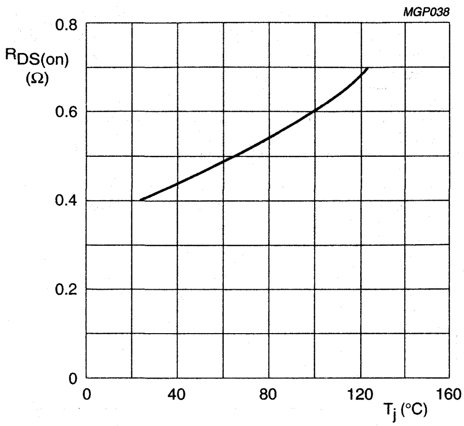
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



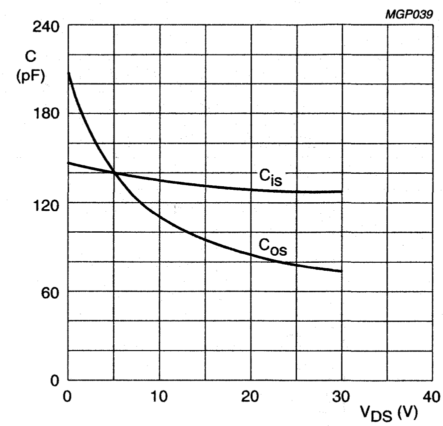
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



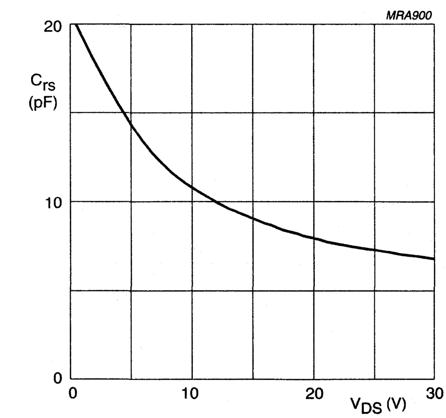
I_D = 1.5 A;
V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

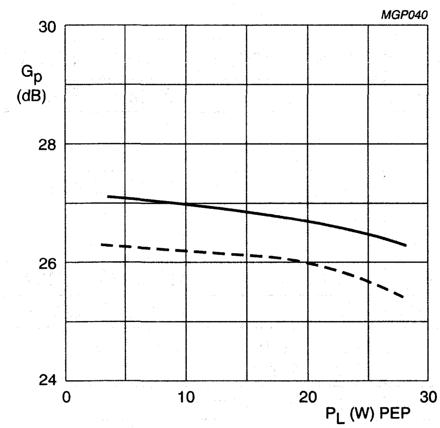
APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; R1 = 26 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-A circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	P_L (W)	G_P (dB)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	Z_L (Ω)
SSB, class-A	28	28	1.3	8 (PEP)	> 24 typ. 27	> −40 typ. −43	< −40 typ. −70	18.4 + j5.2

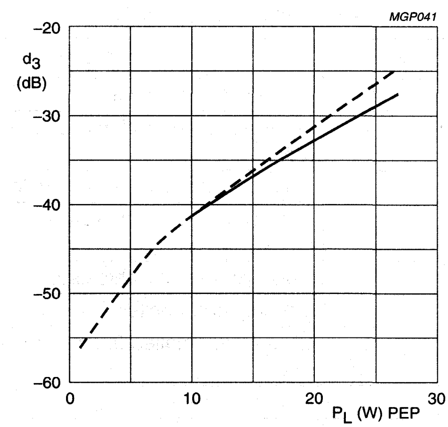
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.



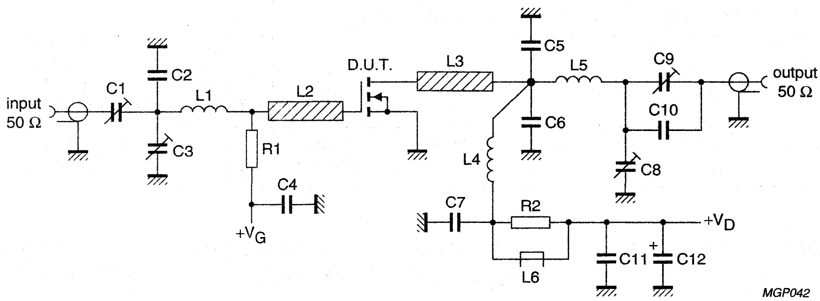
Class-A operation; V_{DS} = 28 V; I_D = 1.3 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



Class-A operation; V_{DS} = 28 V; I_D = 1.3 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Third order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

Fig.11 Test circuit for class-A operation.

List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C8, C9	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2, C10	multilayer ceramic chip capacitor (note 1)	39 pF		
C4, C7	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5, C6	multilayer ceramic chip capacitor (note 1)	27 pF		
C11	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C12	electrolytic capacitor	2.2 μF, 63 V		2222 030 38228
L1	12 turns enamelled 0.5 mm copper wire	307 nH	length 8 mm; int. dia. 4 mm	
L2, L3	stripline (note 2)	30 Ω	length 15 × 6 mm	
L4	14 turns enamelled 1 mm copper wire	1039 nH	length 14 mm; int. dia. 9 mm	
L5	9 turns enamelled 1 mm copper wire	305 nH	length 10 mm; int. dia. 6 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36640
R1	0.25 W metal film resistor	26 Ω		
R2	0.25 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness 1/16 mm.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; R1 = 34 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	Z_L (Ω)
SSB, class-AB	28	28	0.25	30 (PEP)	typ. 20	typ. 40	typ. −35	typ. −40	8.9 + j1.0

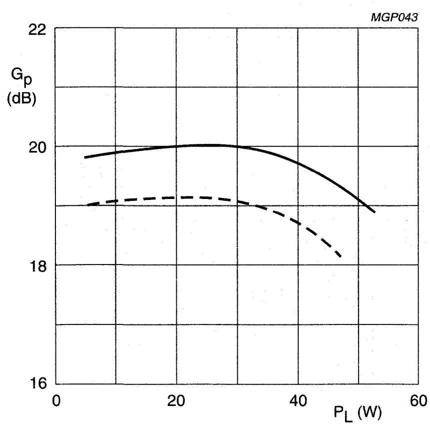
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

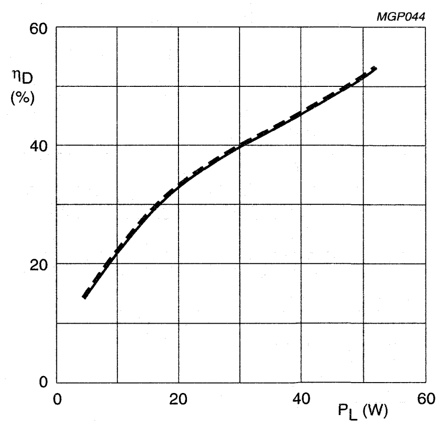
The BLF145 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases at P_L = 30 W single tone under the following conditions:

V_{DS} = 28 V; f = 28 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W at rated load power.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.12 Power gain as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.13 Two tone efficiency as a function of load power, typical values.

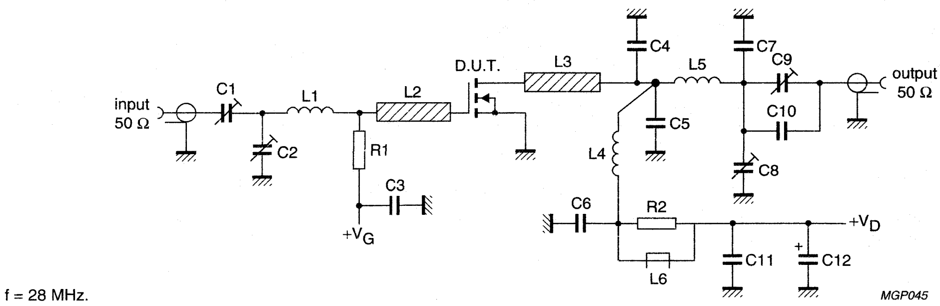


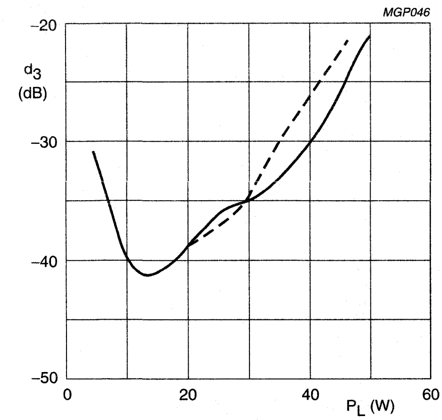
Fig.14 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C4, C5	multilayer ceramic chip capacitor (note 1)	27 pF		
C7, C10	multilayer ceramic chip capacitor (note 1)	39 pF		
C8, C9	film dielectric trimmer	7 to 100 pF		2222 809 07015
C11	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C12	electrolytic capacitor	2.2 μF, 63 V		2222 030 38228
L1	13 turns enamelled 0.5 mm copper wire	415 nH	length 10 mm; int. dia. 5 mm	
L2, L3	stripline (note 2)	30 Ω	length 15 × 6 mm	
L4	10 turns enamelled 1 mm copper wire	390 nH	length 13 mm; int. dia. 7 mm	
L5	9 turns enamelled 1 mm copper wire	245 nH	length 10 mm; int. dia. 5 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36640
R1	0.5 W metal film resistor	34 Ω		
R2	0.25 W metal film resistor	10 Ω		

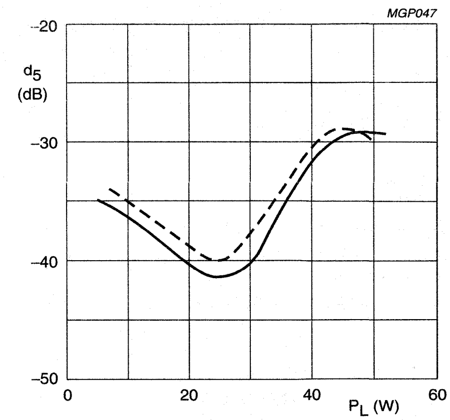
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 4.5$), thickness $^1\!/_{16}$ mm.



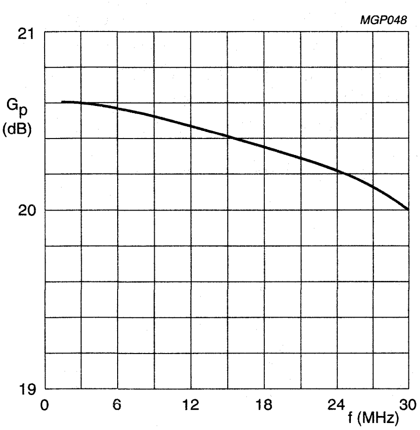
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.15 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.16 Fifth order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W;
R_1 = 34 Ω; Z_L = 8.9 + j1 Ω.

Fig.17 Power gain as a function of frequency, typical values.

Table 1
Input impedance as a function of frequency
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
P_L = 30 W; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; R1 = 34 Ω; Z_L = 8.9 + j1 Ω.

f (MHz)	Z_i (Ω)
1.5	32.9 – j2.2
3.0	32.4 – j4.3
6.0	30.7 – j8.1
10	27.4 – j11.9
15	32.9 – j14.6
20	18.5 – j15.4
25	15.1 – j15.3
30	12.5 – j14.6

VHF power MOS transistor BLF147

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for industrial and military applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to 'General' section for further information.

PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

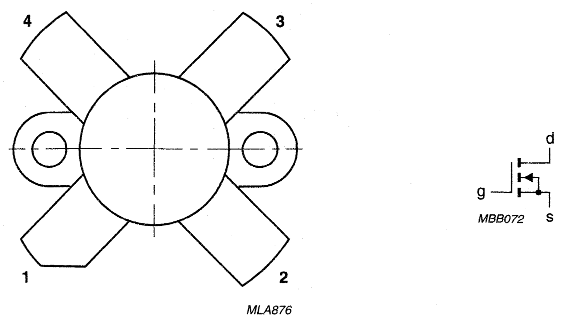


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)	d_5 (dB)
SSB, class-AB	28	28	150 (PEP)	> 17	> 35	< −30	< −30
CW, class-B	108	28	150	typ. 70	typ. 70	−	−

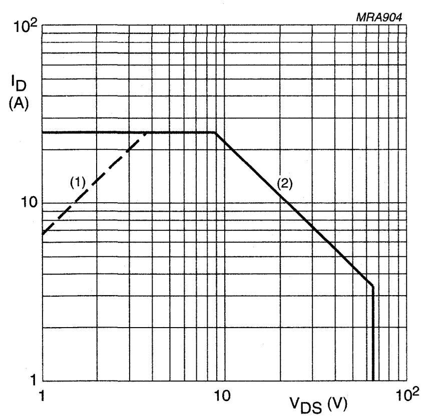
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

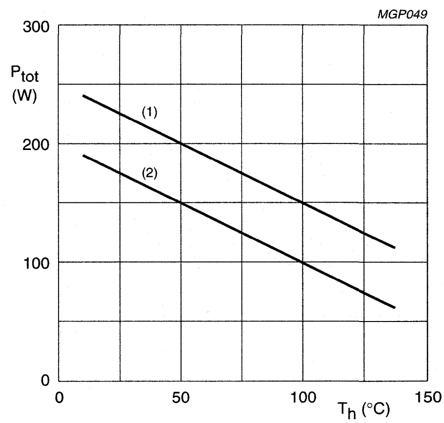
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	0.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



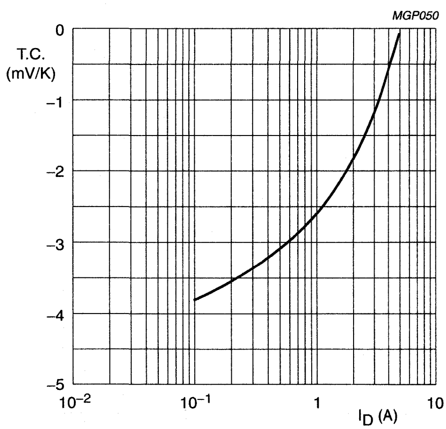
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

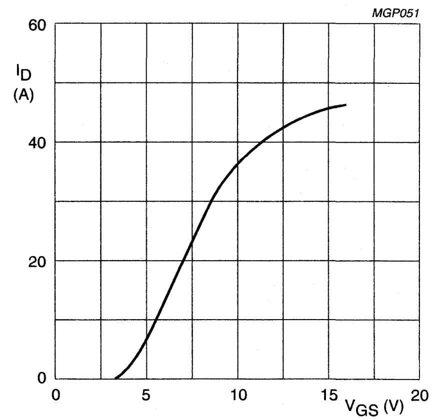
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 100 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 200 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 100 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	450	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	360	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	55	–	pF



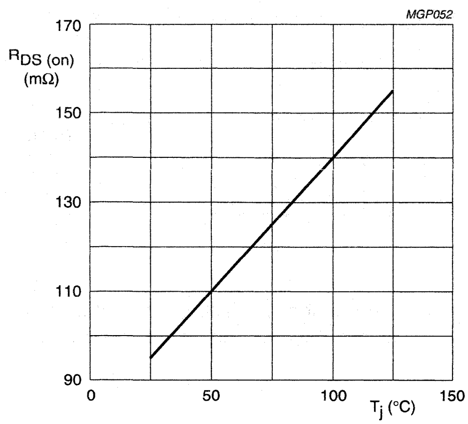
V_{DS} = 28 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



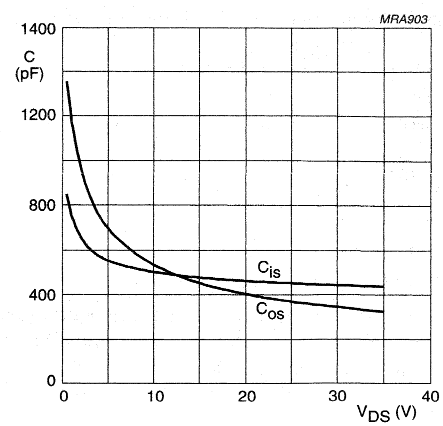
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



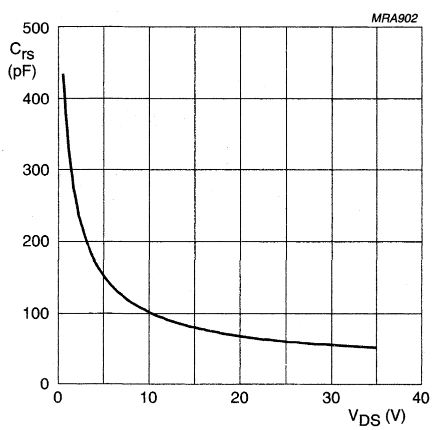
I_D = 8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; R_{GS} = 9.8 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (A)	G_p (dB)	η_D (%)	d_3 (dB) (note 2)	d_5 (dB) (note 2)
20 to 150 (PEP)	28	28	1	> 17 typ. 19	> 35 typ. 40	< −30 typ. −34	< −30 typ. −40

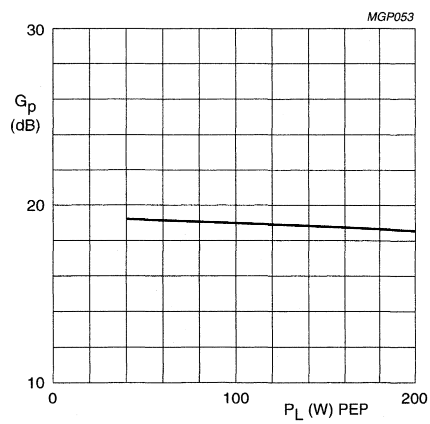
Notes

1. Optimum load impedance: 2.1 + j0 Ω.
2. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

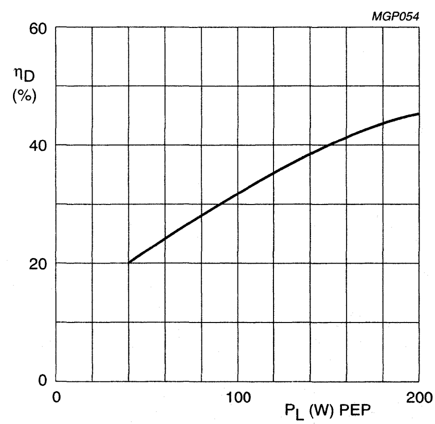
The BLF147 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 28 MHz at rated load power.



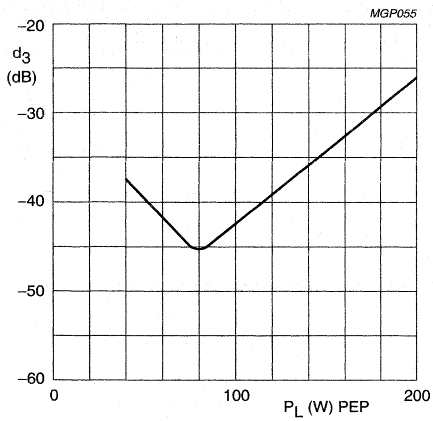
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.9 Gain as a function of load power, typical values.



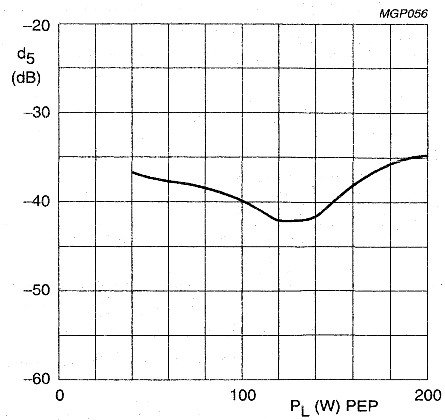
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.10 Efficiency as a function of load power, typical values.



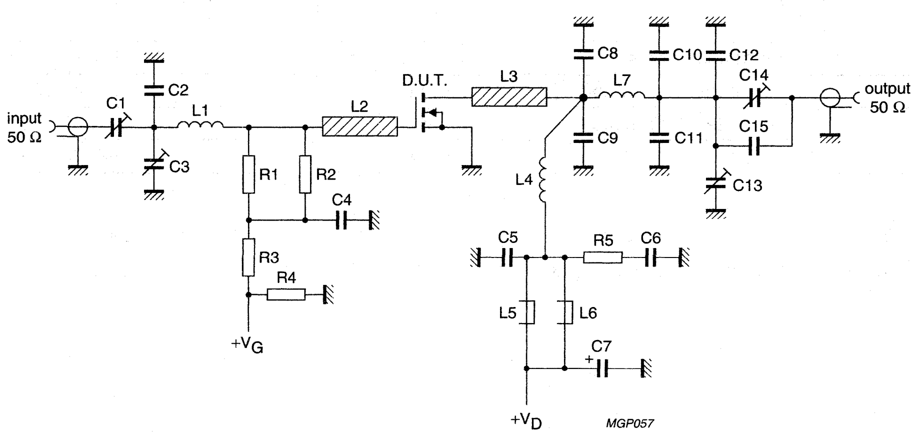
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.11 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.12 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

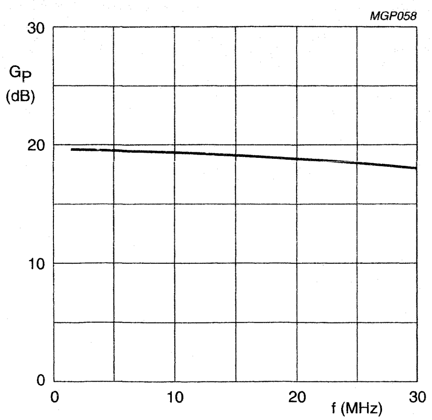
Fig.13 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2, C8, C9	multilayer ceramic chip capacitor (note 1)	75 pF		
C4, C5	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C6	multilayer ceramic chip capacitors in parallel	3 × 100 nF		2222 852 47104
C7	electrolytic capacitor	2.2 µF, 63 V		
C10	multilayer ceramic chip capacitor (note 1)	100 pF		
C11, C12	multilayer ceramic chip capacitor (note 1)	150 nF		
C15	multilayer ceramic chip capacitor (note 1)	240 pF		
L1	6 turns enamelled 0.7 mm copper wire	145 nH	length 5 mm; int. dia. 6 mm; leads 2 × 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 × 6 mm	
L4	4 turns enamelled 1.5 mm copper wire	148 nH	length 8 mm; int. dia. 10 mm; leads 2 × 5 mm	
L5, L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	3 turns enamelled 2.2 mm copper wire	79 nH	length 8 mm; int. dia. 8 mm; leads 2 × 5 mm	
R1, R2	1 W metal film resistor	19.6 Ω		2322 153 51969
R3	0.4 W metal film resistor	10 kΩ		2322 151 71003
R4	0.4 W metal film resistor	1 MΩ		2322 151 71005
R5	1 W metal film resistor	10 Ω		2322 153 51009

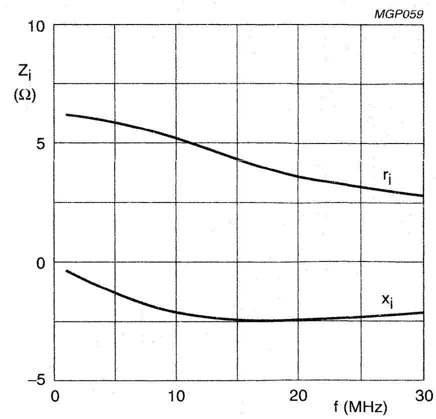
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm.



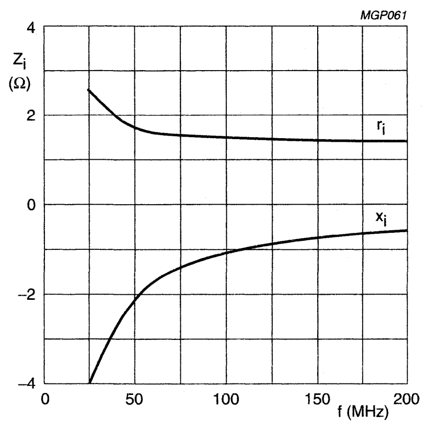
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 6.25 Ω; P_L = 150 W (PEP); R_L = 2.1 Ω.

Fig.14 Gain as a function of frequency, typical values.



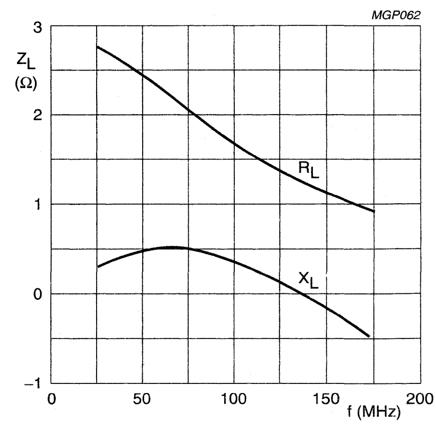
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 6.25 Ω; P_L = 150 W (PEP); R_L = 2.1 Ω.

Fig.15 Input impedance as a function of frequency (series components), typical values.



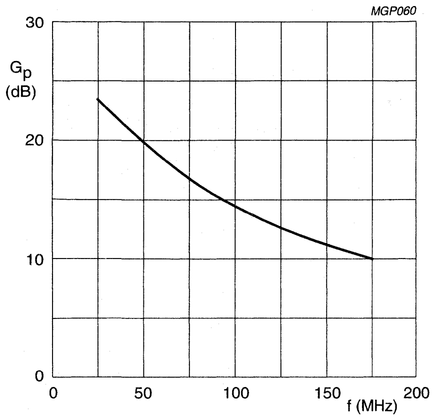
Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.16 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.17 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.18 Power gain as a function of frequency, typical values.

HF/VHF power MOS transistor — BLF175

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the HF/VHF frequency range.

The transistor has a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

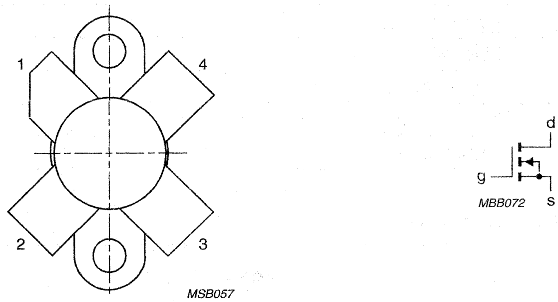


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	d_3 (dB)
class-A	28	50	800	8 (PEP)	> 24	–	< –40
class-AB	28	50	150	30 (PEP)	typ. 24	typ. 40 (note 1)	typ. –35
CW, class-B	108	50	30	30	typ. 20	typ. 65	–

Note

1. 2-tone efficiency.

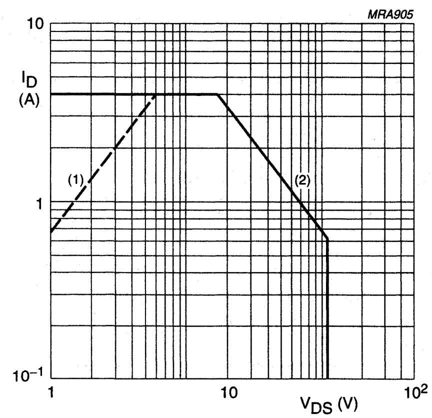
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

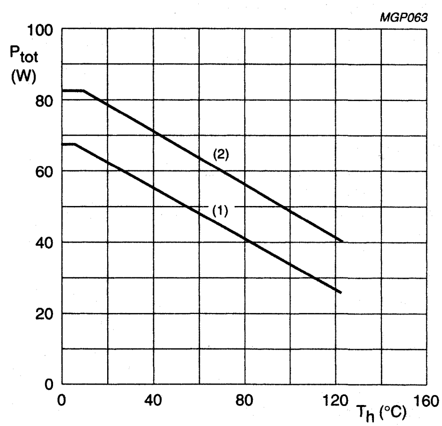
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 68 W	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 68 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



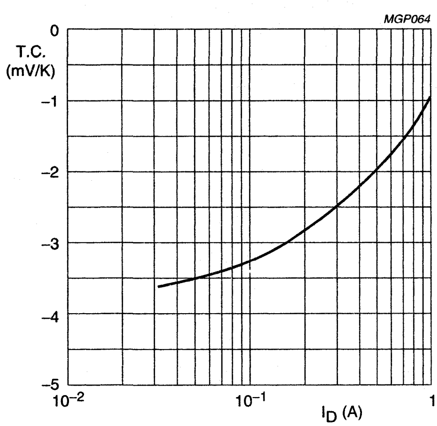
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

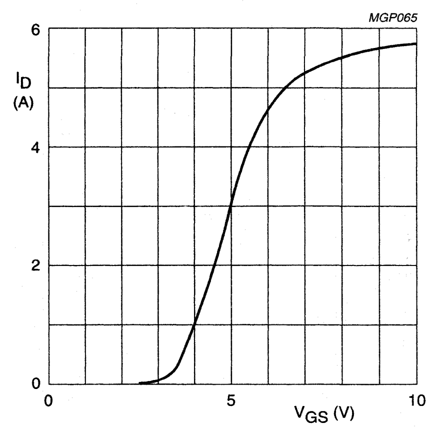
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	100	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1 A; V_{DS} = 10 V	1.1	1.6	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1 A; V_{GS} = 10 V	–	0.75	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5.5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	130	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	36	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	3.7	–	pF



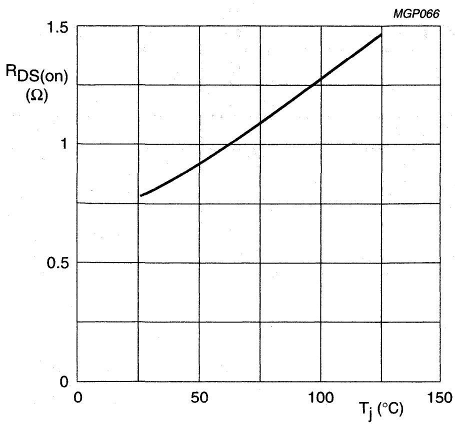
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



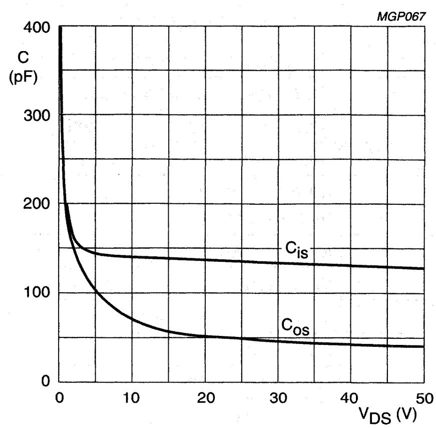
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



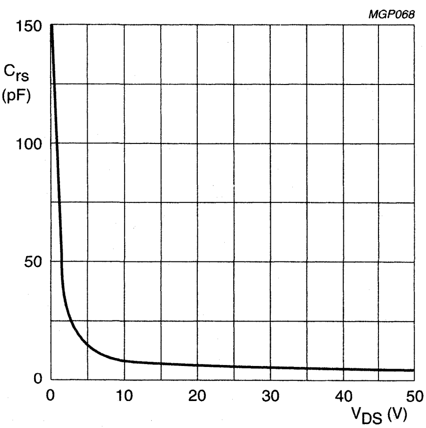
I_D = 1 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

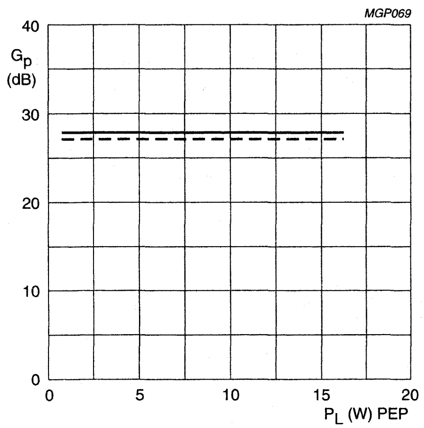
APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_P (dB)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	R_{GS} (Ω)
0 to 8 (PEP)	28	50	800	> 24 typ. 28	> −40 typ. −44	< −40 typ. −64	24 24

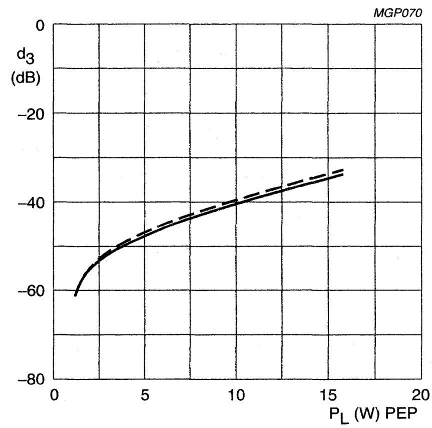
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.



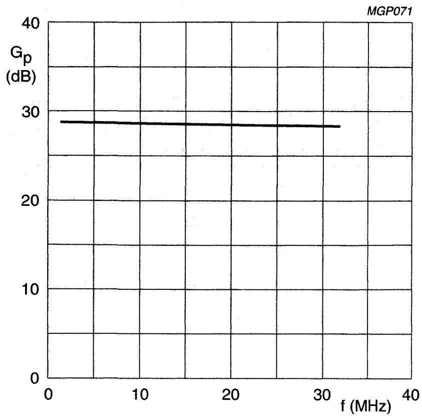
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



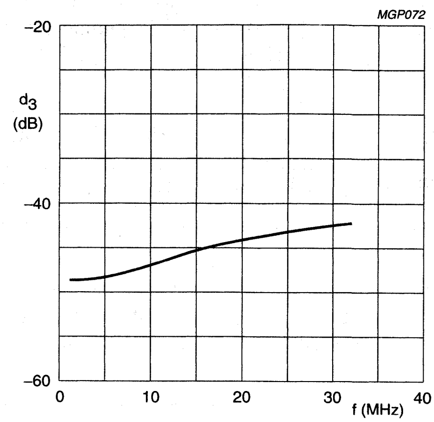
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Third order intermodulation distortion as a function of load power, typical values.



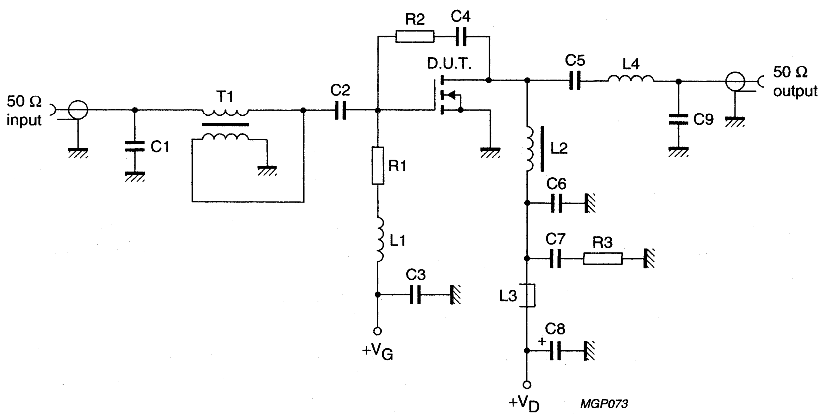
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.11 Power gain as a function of frequency, typical values.



Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.12 Third order intermodulation distortion as a function of frequency, typical values.



f = 28 MHz.

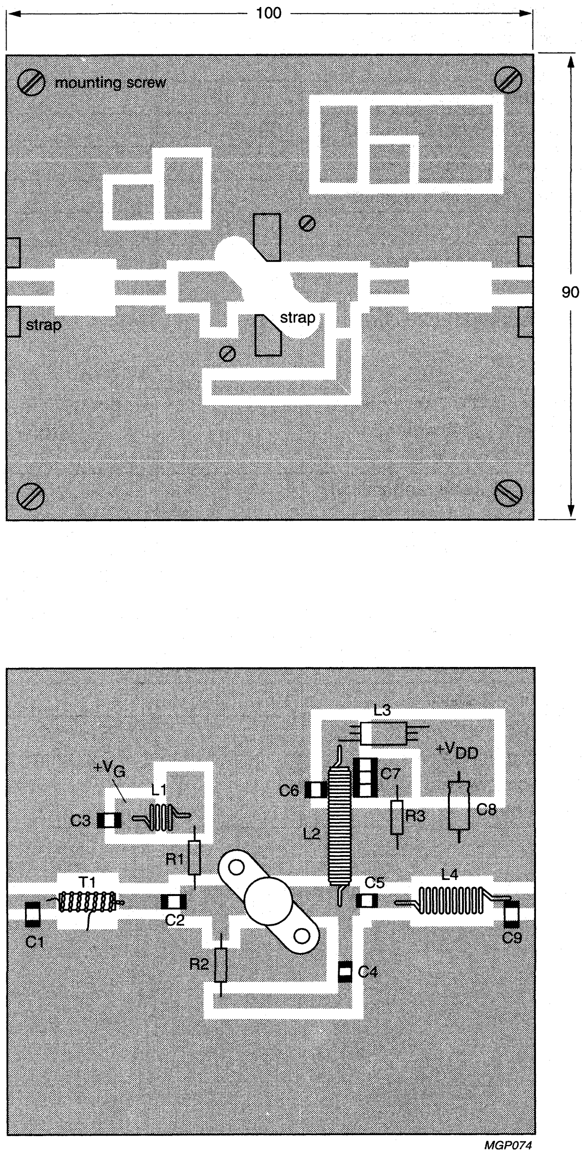
Fig.13 Test circuit for class-A operation.

List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor (note 1)	39 pF		
C2	multilayer ceramic chip capacitor	3 × 10 nF		2222 852 47103
C3, C4, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C8	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
C9	multilayer ceramic chip capacitor (note 1)	24 pF		
L1	4 turns enamelled 0.6 mm copper wire	86 nH	length 3.3 mm; int. dia. 5 mm; leads 2 x 2 mm	
L2	36 turns enamelled 0.7 mm copper wire wound on a rod grade 4B1 Ferroxcube drain choke	20 μH	length 30 mm; int. dia. 5 mm	4330 030 30031
L3	grade 3B Ferroxcube wideband RF choke			4312 020 36640
L4	8 turns enamelled 1 mm copper wire	189 nH	length 9.5 mm; int. dia. 5 mm; leads 2 x 3 mm	
R1	0.4 W metal film resistor	24 Ω		
R2	0.4 W metal film resistor	1500 Ω		
R3	0.4 W metal film resistor	10 Ω		
T1	4 : 1 transformer; 18 turns twisted pair of 0.25 mm copper wire with 10 twists per cm, wound on a grade 4C6 toroidal core		dimensions 9 x 6 x 3 mm	4322 020 97171

Note

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.



Note: The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

Fig.14 Component layout for 28 MHz class-A test circuit.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

$T_h = 25$ °C; $R_{th\ mb\text{-}h} = 0.3$ K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.
$f_1 = 28.000$ MHz; $f_2 = 28.001$ MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_P (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	R_{GS} (Ω)
30 (PEP)	28	50	150	typ. 24	typ. 40 (note 2)	typ. −35	typ. −40	22

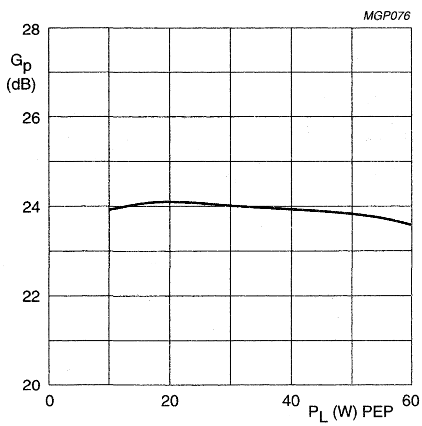
Notes

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.
2. 2-tone efficiency.

Ruggedness in class-AB operation

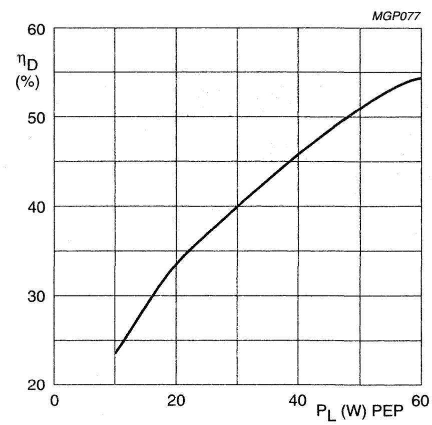
The BLF175 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases at $P_L = 30$ W single tone under the following conditions:

$V_{DS} = 50$ V; f = 28 MHz.



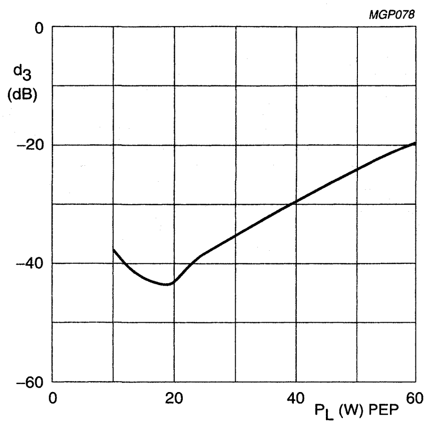
Class-AB operation; $V_{DS} = 50$ V; $I_{DQ} = 0.15$ A;
$R_{GS} = 22$ Ω; $f_1 = 28.000$ MHz; $f_2 = 28.001$ MHz.

Fig.15 Power gain as a function of load power, typical values.



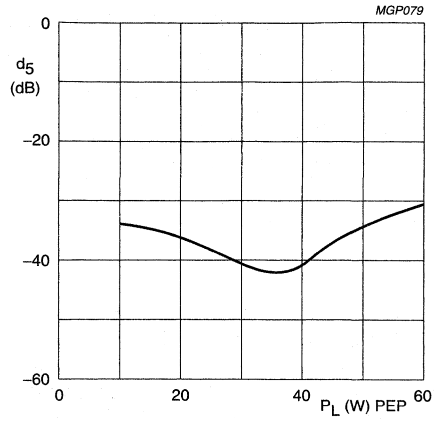
Class-AB operation; $V_{DS} = 50$ V; $I_{DQ} = 0.15$ A;
$R_{GS} = 22$ Ω; $f_1 = 28.000$ MHz; $f_2 = 28.001$ MHz.

Fig.16 Two tone efficiency as a function of load power, typical values.



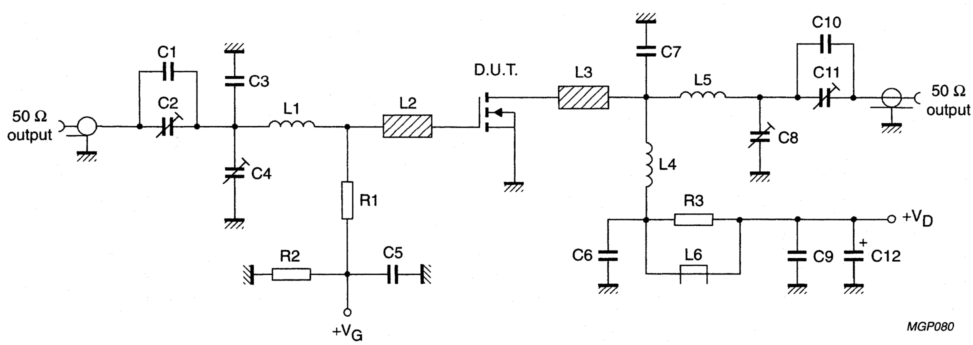
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.17 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.18 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

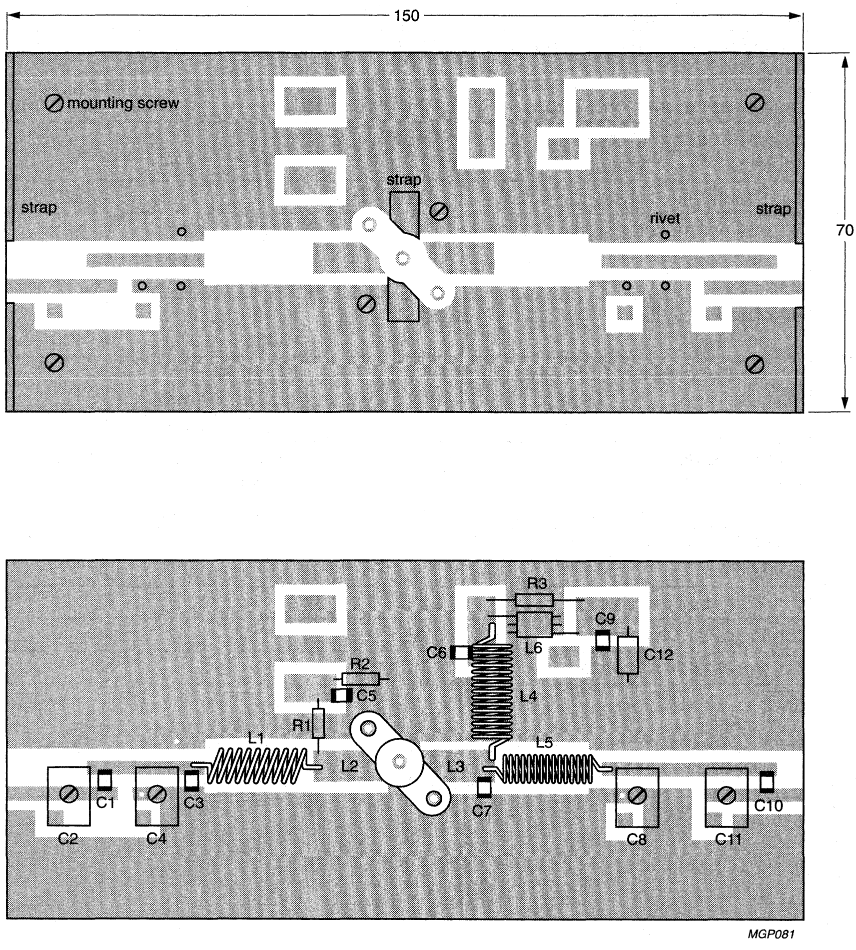
Fig.19 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C10	multilayer ceramic chip capacitor (note 1)	62 pF		
C2, C4, C8, C11	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3	multilayer ceramic chip capacitor (note 1)	51 pF		
C5, C6, C9	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor (note 1)	10 pF		
C12	aluminium electrolytic capacitor	10 µF, 63 V		2222 030 28109
L1	9 turns enamelled 1 mm copper wire	280 nH	length 11 mm; int. dia. 6 mm; leads 2 x 4 mm	
L2, L3	stripline (note 2)	30 Ω	length 10 mm; width 6 mm	
L4	14 turns enamelled 1 mm copper wire	1650 nH	length 20 mm; int. dia. 12 mm; leads 2 x 2 mm	
L5	10 turns enamelled 1 mm copper wire	380 nH	length 13 mm; int. dia. 7 mm; leads 2 x 3 mm	
L6	grade 3B Ferroxcube wideband RF choke			4312 020 36640
R1	0.4 W metal film resistor	22 Ω		
R2	0.4 W metal film resistor	1 MΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

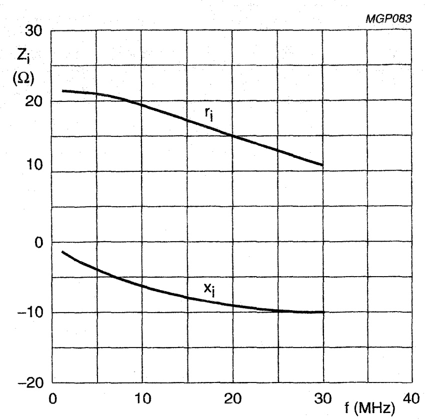
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness 1.6 mm.



Note: The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

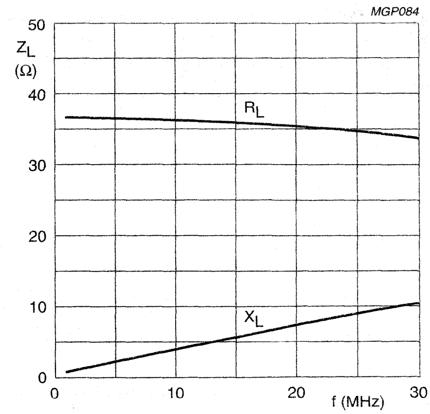
Dimensions in mm.

Fig.20 Component layout for 28 MHz class-AB test circuit.



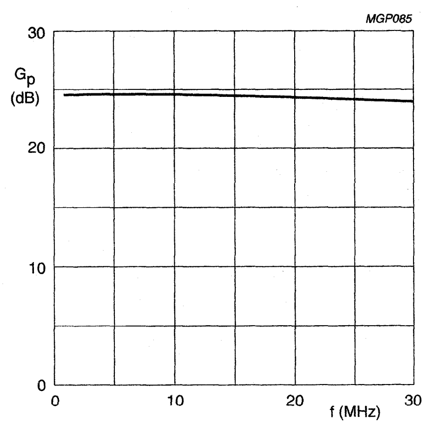
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.21 Input impedance as a function of frequency (series components), typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.22 Load impedance as a function of frequency (series components), typical values.



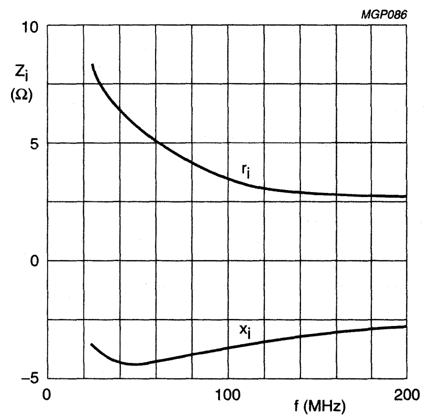
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.23 Power gain as a function of frequency, typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

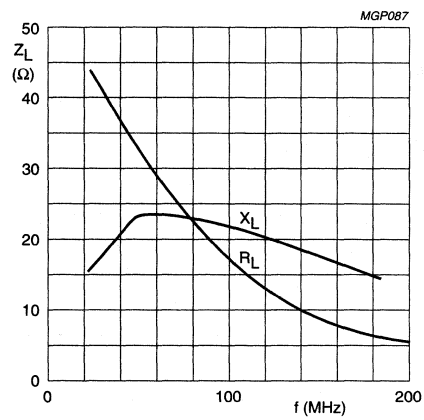
RF performance in SSB operation in a common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	R_{GS} (Ω)
CW, class-B	108	50	30	30	typ. 20	typ. 65	10



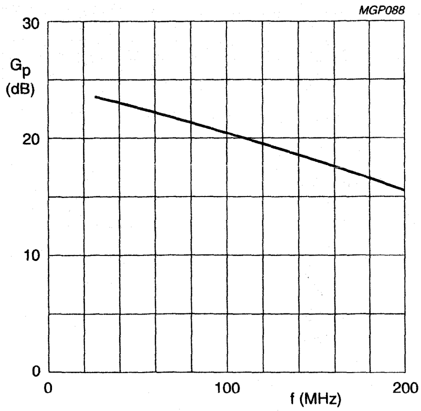
Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.24 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.25 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.26 Power gain as a function of frequency, typical values.

HF/VHF power MOS transistor BLF177

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

APPLICATIONS

- Designed for industrial and military applications in the HF/VHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT121B flanged package, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the handbook 'General' section for further information.

PINNING

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

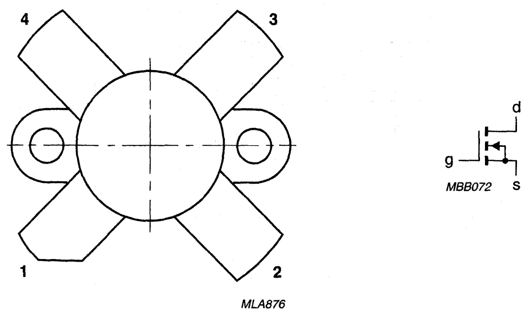


Fig.1 Simplified outline (SOT121B) and symbol.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)	d_5 (dB)
SSB class-AB	28	50	150 (PEP)	>20	>35	<−30	<−30
CW class-B	108	50	150	typ. 19	typ. 70	−	−

HF/VHF power MOS transistor BLF177

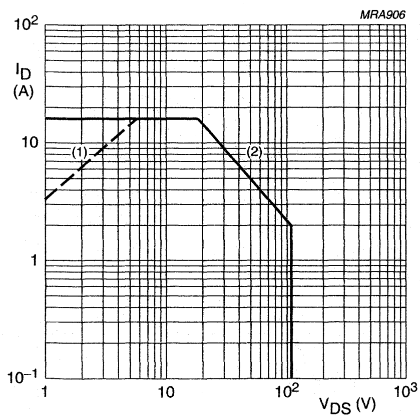
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	16	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	220	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

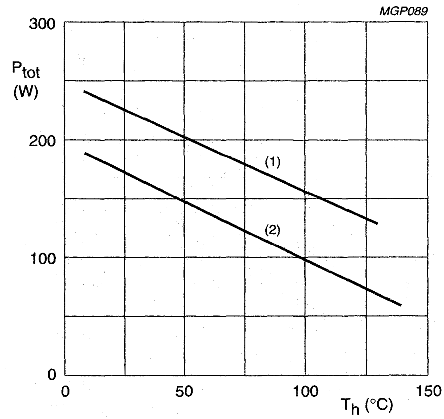
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	max. 0.8	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	max. 0.2	K/W



(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



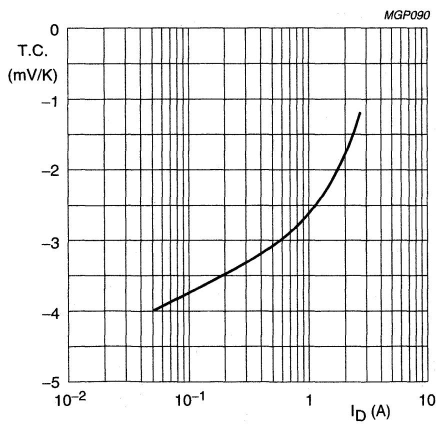
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power derating curves.

CHARACTERISTICS

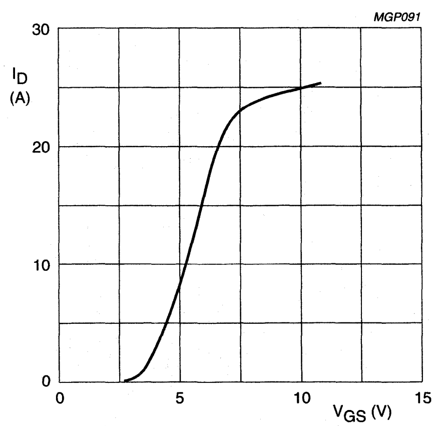
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 50 mA; V_{GS} = 0	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
R_{DSon}	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF



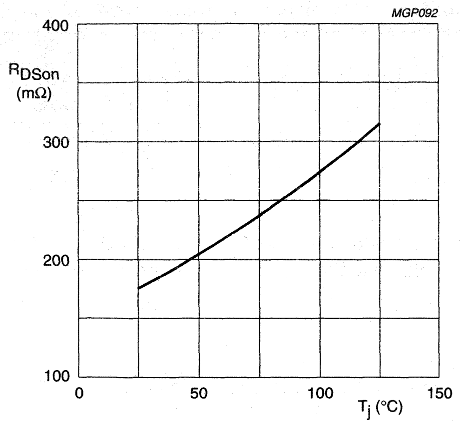
V_{DS} = 10 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



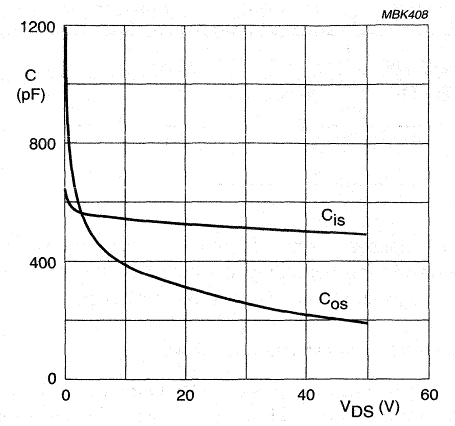
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage; typical values.



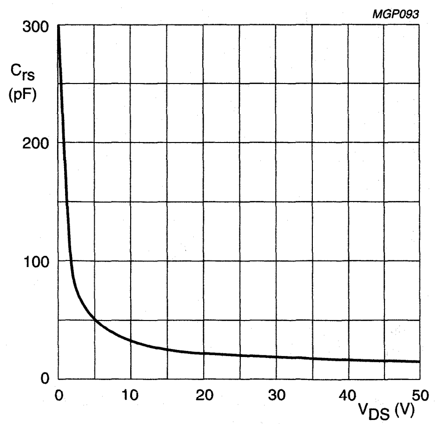
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

RF performance in SSB operation in a common source class-AB test circuit (see Fig.13).
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; Z_L = 6.25 + j0 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz unless otherwise specified.

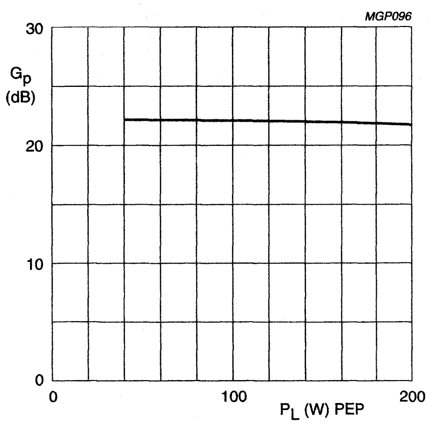
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)
SSB, class-AB	28	50	0.7	20 to 150 (PEP)	>20 typ. 35	>35 typ. 40	<−30 typ. −35	<−30 typ. −38

Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

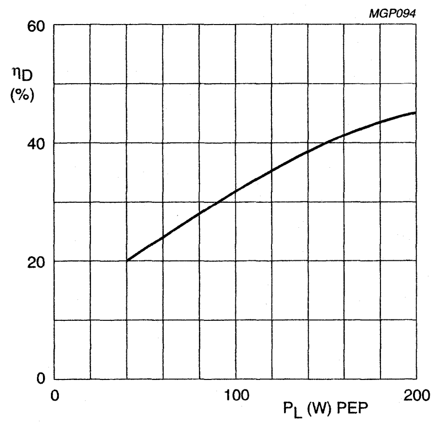
Ruggedness in class-AB operation

The BLF177 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions: f = 28 MHz; V_{DS} = 50 V at rated output power.



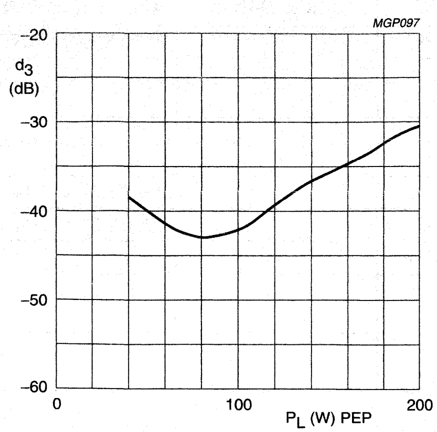
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.9 Power gain as a function of load power; typical values.



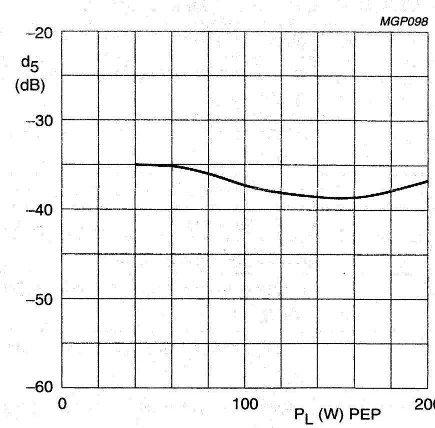
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.10 Two tone efficiency as a function of load power; typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.11 Third order intermodulation distortion as a function of load power; typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.12 Fifth order intermodulation distortion as a function of load power; typical values.

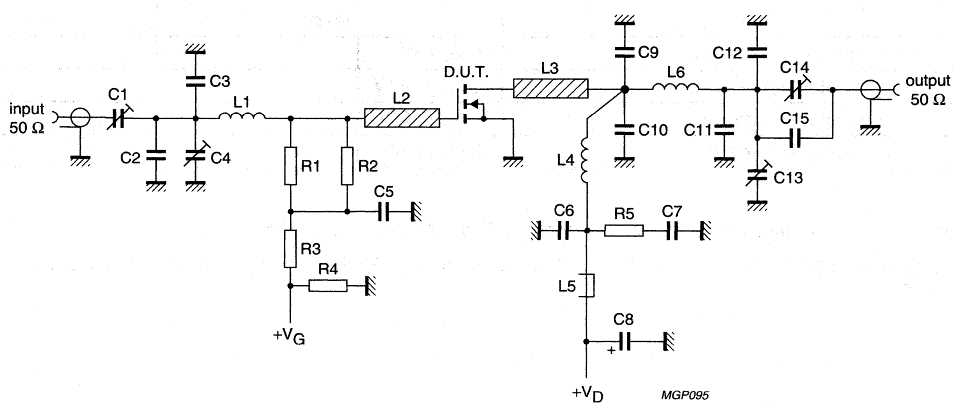


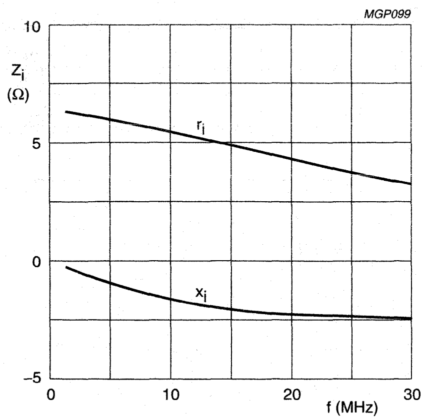
Fig.13 Test circuit for class-AB operation at 28 MHz.

List of components class-AB test circuit (see Fig.13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C4, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2	multilayer ceramic chip capacitor (note 1)	56 pF		
C3, C11	multilayer ceramic chip capacitor (note 1)	62 pF		
C5, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C8	electrolytic capacitor	2.2 µF, 63 V		
C9, C10	multilayer ceramic chip capacitor (note 1)	20 pF		
C12	multilayer ceramic chip capacitor (note 1)	100 pF		
C15	multilayer ceramic chip capacitor (note 1)	150 pF		
L1	5 turns enamelled 0.7 mm copper wire	133 nH	length 4.5 mm; int. dia. 6 mm; leads 2 × 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 × 6 mm	
L4	7 turns enamelled 1.5 mm copper wire	236 nH	length 12.5 mm; int. dia. 8 mm; leads 2 × 5 mm	
L5	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L6	5 turns enamelled 2 mm copper wire	170 nH	length 11.5 mm; int. dia. 8 mm; leads 2 × 5 mm	
R1, R2	metal film resistor	10 Ω, 1 W		
R2	metal film resistor	10 kΩ, 0.4 W		
R3	metal film resistor	1 MΩ, 0.4 W		
R5	metal film resistor	10 kΩ, 1 W		

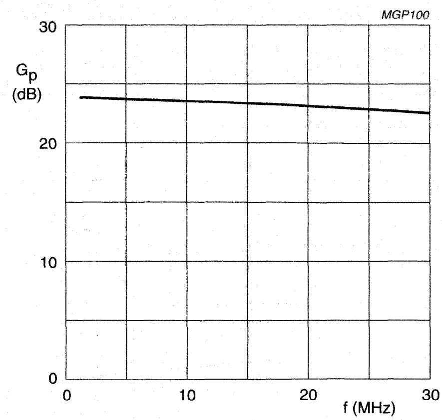
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness 1.6 mm.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.14 Input impedance as a function of frequency (series components); typical values.



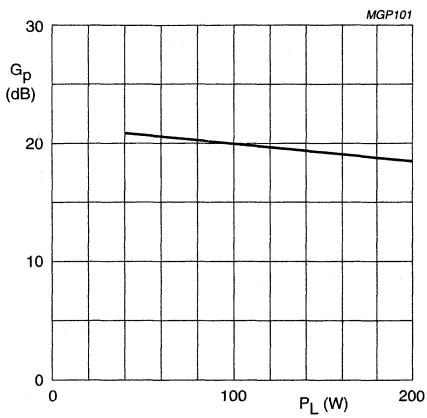
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.15 Power gain as a function of frequency; typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

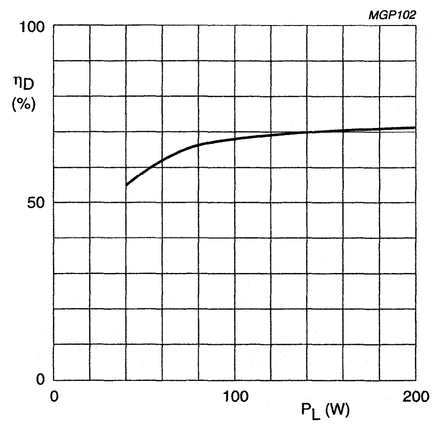
RF performance in CW operation in a common source class-B test circuit (see Fig.19).
T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; R_{GS} = 15.8 Ω unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	0.1	150	typ. 19	typ. 70



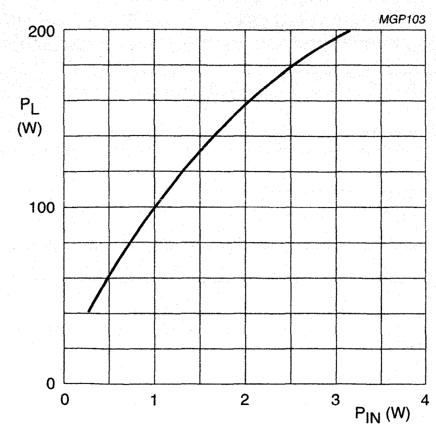
Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA;
R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.16 Power gain as a function of load power; typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA;
R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.17 Two tone efficiency as a function of load power; typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA;
R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.18 Load power as a function of input power; typical values.

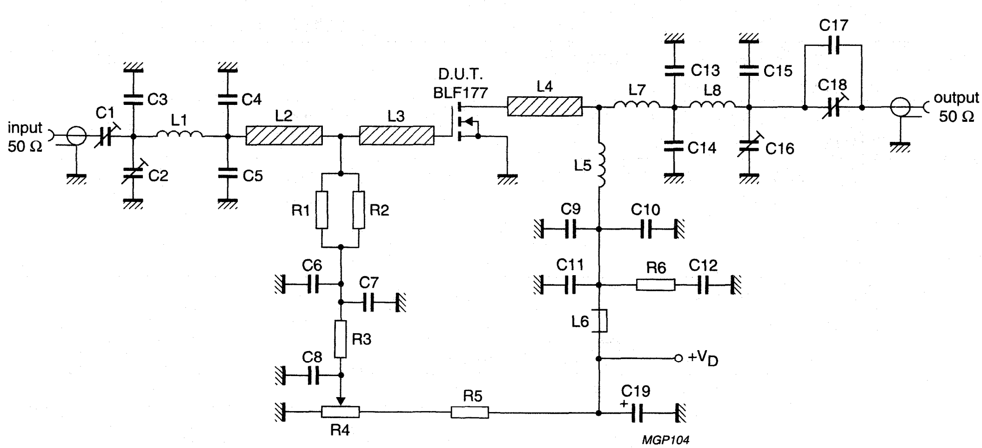


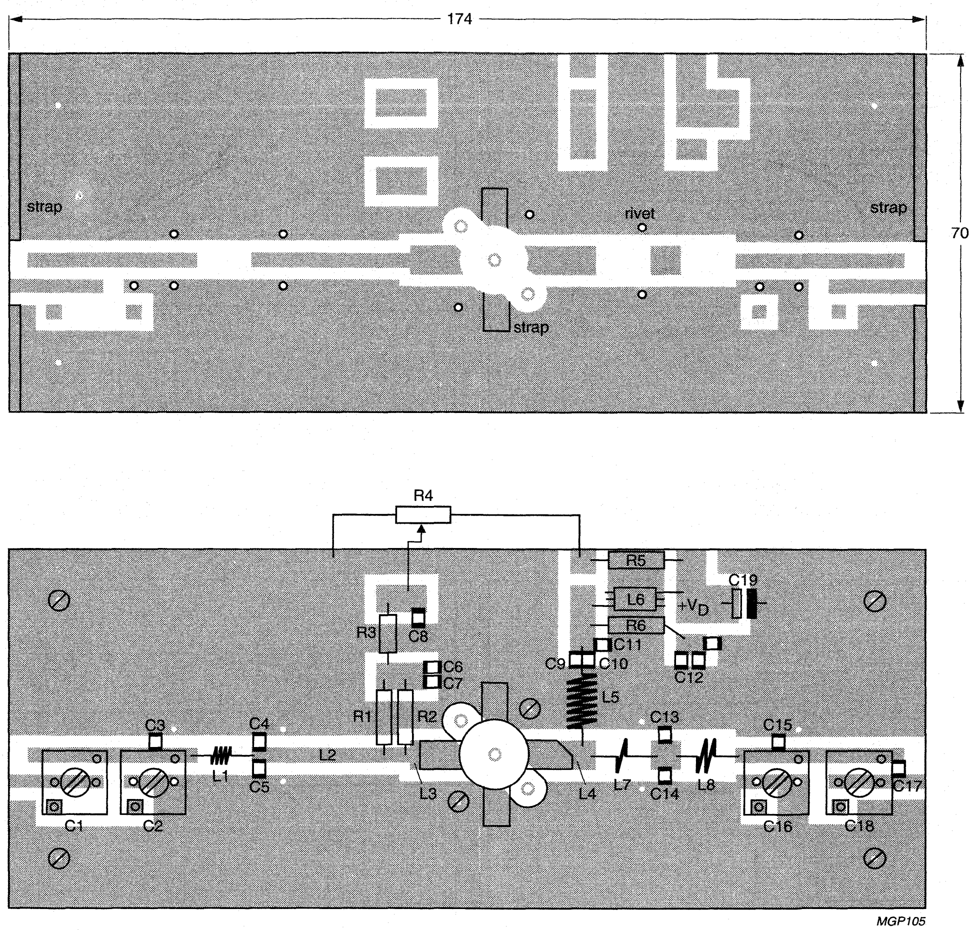
Fig.19 Test circuit for class-B operation at 108 MHz.

List of components class-B test circuit (see Fig.19)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C16, C18	film dielectric trimmer	2.5 to 20 pF		2222 809 07004
C3	multilayer ceramic chip capacitor (note 1)	20 pF		
C4, C5	multilayer ceramic chip capacitor (note 1)	62 pF		
C6, C7, C9, C10	multilayer ceramic chip capacitor (note 1)	1 nF		
C8	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C12	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C13, C14	multilayer ceramic chip capacitor (note 1)	36 pF		
C15	multilayer ceramic chip capacitor (note 1)	12 pF		
C17	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C19	electrolytic capacitor	4.4 μF, 63 V		2222 030 28478
L1	3 turns enamelled 0.8 mm copper wire	22 nH	length 5.5 mm; int. dia. 3 mm; leads 2 × 5 mm	
L2	stripline (note 2)	64.7 Ω	31 × 3 mm	
L3, L4	stripline (note 2)	41.1 Ω	10 × 6 mm	
L5	6 turns enamelled 1.6 mm copper wire	122 nH	length 13.8 mm; int. dia. 6 mm; leads 2 × 5 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	1 turn enamelled 1.6 mm copper wire	16.5 nH	int. dia. 9 mm; leads 2 × 5 mm	
L8	2 turns enamelled 1.6 mm copper wire	34.4 nH	length 3.9 mm; int. dia. 6 mm; leads 2 × 5 mm	
R1, R2	metal film resistor	31.6 Ω, 1 W		
R3	metal film resistor	1 kΩ, 0.4 W		
R4	cermet potentiometer	5 kΩ		
R5	metal film resistor	44.2 Ω, 0.4 W		
R6	metal film resistor	10 Ω, 1 W		

Notes

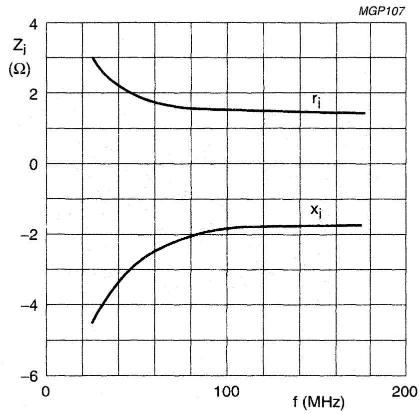
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness 1.6 mm.



Dimensions in mm.

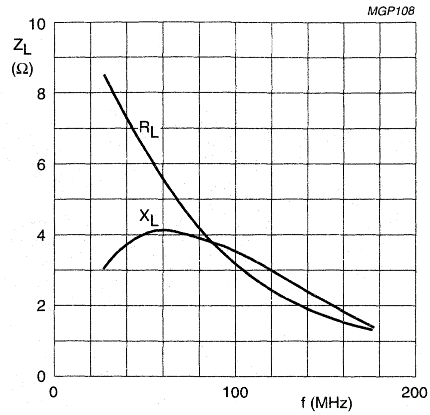
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of hollow rivets, whilst under the source leads and at the input and output copper straps are used for a direct contact between upper and lower sheets.

Fig.20 Component layout for 108 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.21 Input impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.22 Load impedance as a function of frequency (series components); typical values.

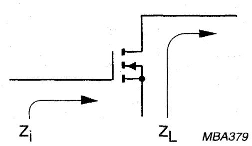
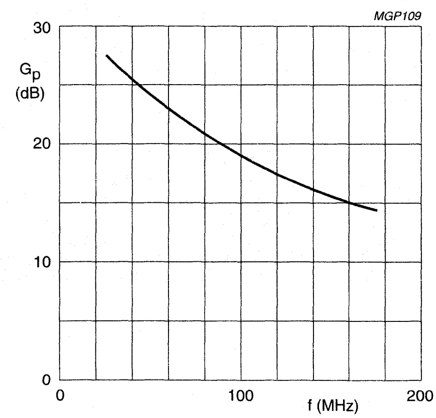


Fig.23 Definition of transistor impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.24 Power gain as a function of frequency; typical values.

HF/VHF power MOS transistor | BLF202

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch.

APPLICATIONS

- Communications transmitters in the HF/VHF range with a nominal supply voltage of 12.5 V.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor in an 8-lead SOT409A SMD package with a ceramic cap.

PINNING - SOT409A

PIN	DESCRIPTION
1, 8	source
2, 3	gate
4, 5	source
6, 7	drain

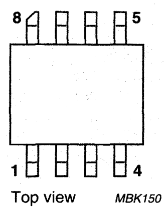


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	2	>10	>50

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

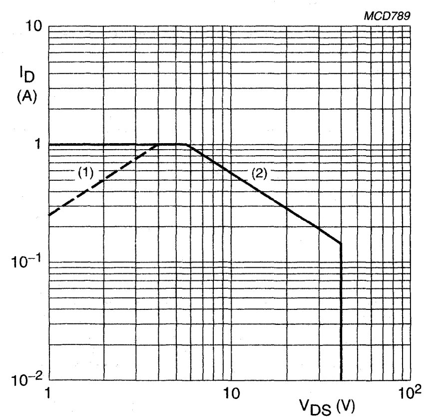
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
V_{GS}	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	$T_{mb} \leq 85$ °C	–	5.7	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_{mb} \leq 85$ °C, $P_{tot} = 5.7$ W	20.5	K/W



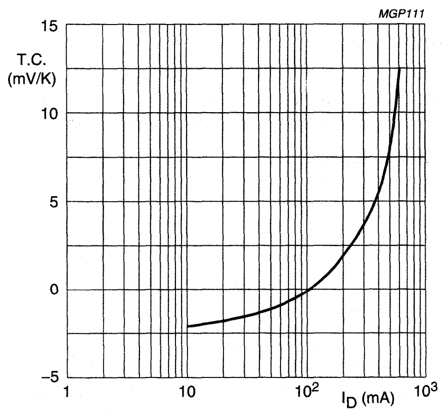
(1) Current is this area may be limited by $R_{DS(on)}$.
(2) $T_{mb} = 85$ °C.

Fig.2 DC SOAR.

CHARACTERISTICS

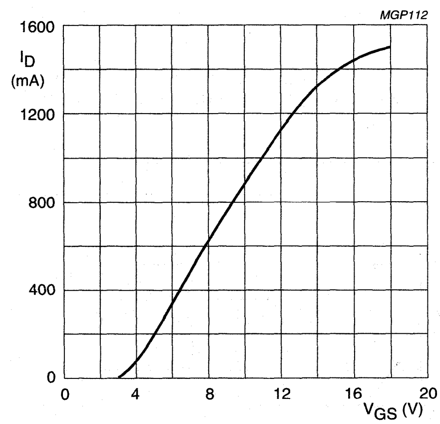
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 3 mA; V_{GS} = 0	40	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	10	μA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	1.3	–	A
R_{DSon}	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.5	4	Ω
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	80	135	–	mS
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	5.3	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	7.8	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	1.8	–	pF



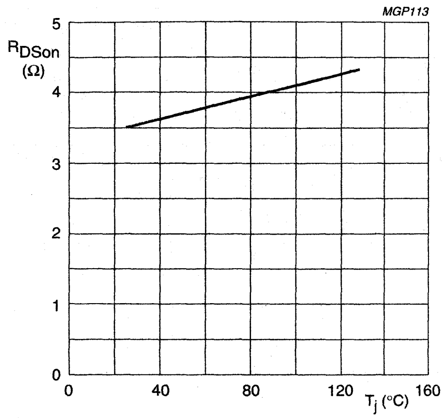
V_{DS} = 10 V.

Fig.3 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



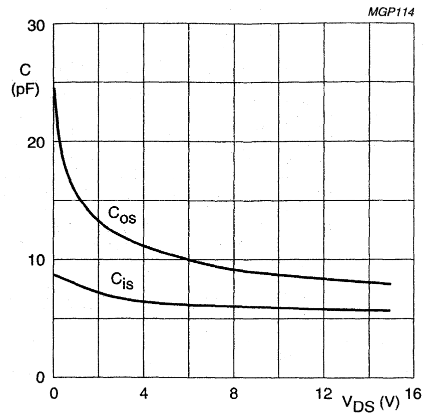
V_{DS} = 10 V; T_j = 25 °C.

Fig.4 Drain current as a function of gate-source voltage; typical values.



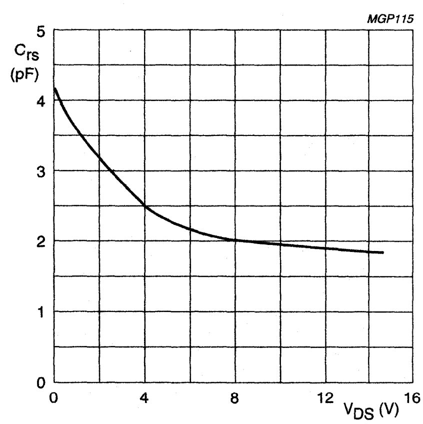
V_{GS} = 15 V; I_D = 0.3 A.

Fig.5 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.6 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Feedback capacitance as a function of drain-source voltage; typical values.

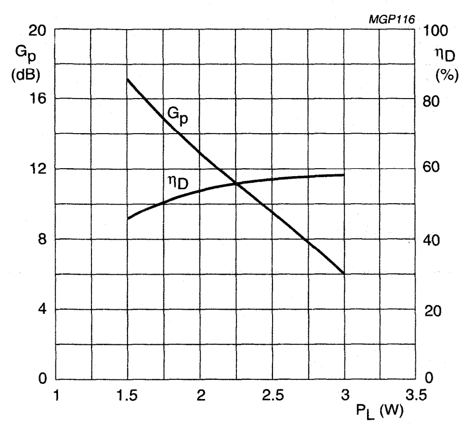
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_{mb} = 25 °C; R_{GS} = 237 Ω; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	20	2	>10; typ. 13	>50; typ. 55

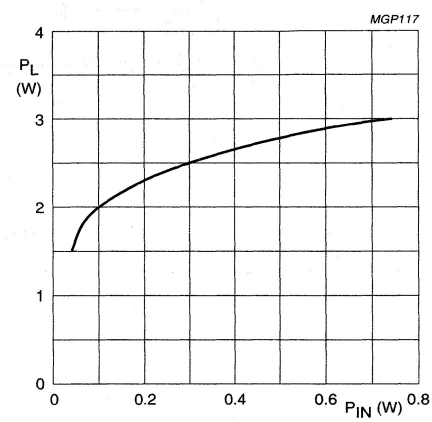
Ruggedness in class-B operation

The BLF202 is capable of withstanding a load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions: V_{DS} = 15.5 V; f = 175 MHz at rated load power.



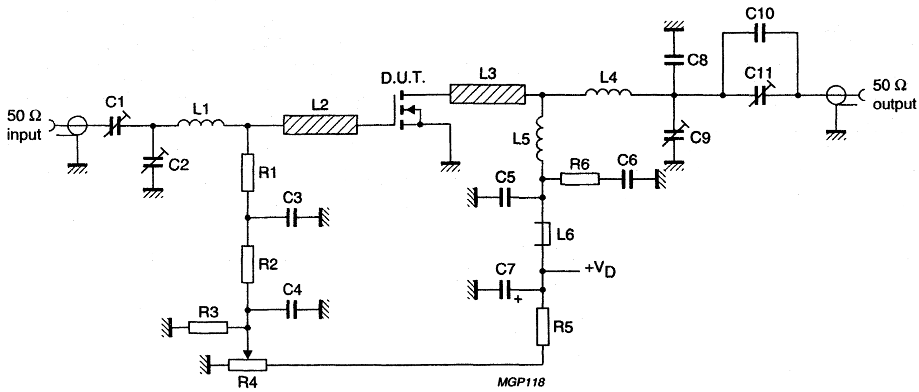
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20mA; f = 175 MHz.

Fig.8 Power gain and efficiency as a functions of load power; typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; f = 175 MHz.

Fig.9 Load power as a function of input power; typical values.



f = 175 MHz.

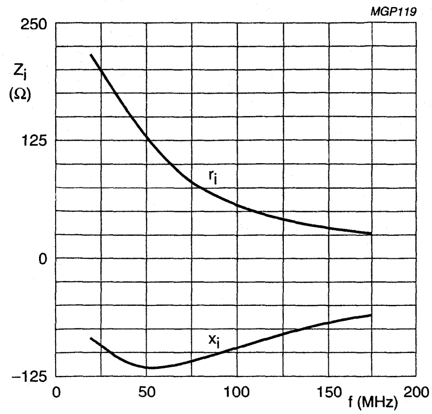
Fig.10 Test circuit for class-B operation.

List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C11	film dielectric trimmer	2 to 9 pF		2222 809 09005
C2, C9	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3, C5	multilayer ceramic chip capacitor; note 1	1 nF; 500 V		
C4, C6	multilayer ceramic chip capacitor	2 × 100 nF in parallel, 50 V		2222 852 47104
C7	Sprague electrolytic tantalum capacitor	2.2 μF; 35 V		
C8	multilayer ceramic chip capacitor; note 1	5.1 pF; 500 V		
C10	multilayer ceramic chip capacitor; note 1	9.1 pF; 500 V		
L1	8 turns enamelled 0.8 mm copper wire	137 nH	length 5.1 mm; int. dia. 4 mm; leads 2 × 5 mm	
L2, L3	stripline; note 2	81 Ω	8 mm × 2 mm	
L4	3 turns enamelled 1 mm copper wire	57 nH	length 5 mm; int. dia. 6 mm; leads 2 × 5 mm	
L5	9 turns enamelled 1 mm copper wire	355 nH	length 11 mm; int. dia. 7 mm; leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36642
R1	0.4 W metal film resistor	237 Ω		2322 151 72371
R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	0.4 W metal film resistor	1 MΩ		2322 151 71005
R4	10 turns cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

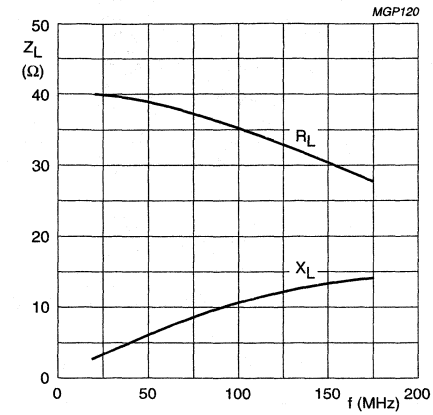
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed-circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm.



Class B-operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA;
R_{GS} = 237 Ω; P_L = 2 W.

Fig.11 Input impedance as a function of frequency (series of components); typical values.



Class B-operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA;
R_{GS} = 237 Ω; P_L = 2 W.

Fig.12 Load impedance as a function of frequency (series components); typical values.

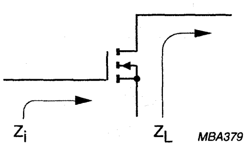
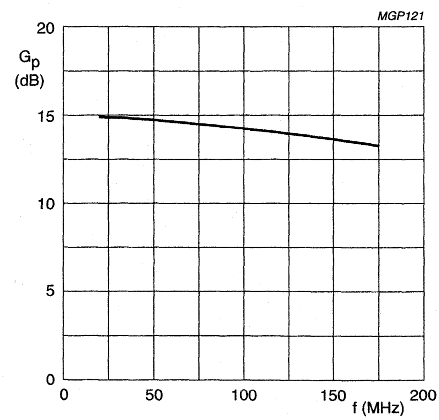


Fig.13 Definition of MOS impedance.

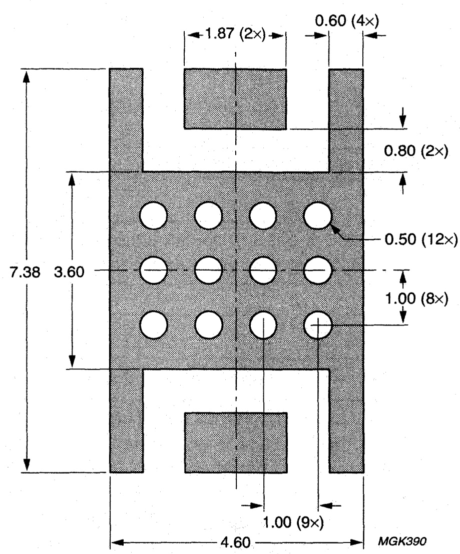


Class B-operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA;
R_{GS} = 237 Ω; P_L = 2 W.

Fig.14 Power gain as a function of frequency; typical values.

MOUNTING RECOMMENDATIONS

Both the metallized groundplate and leads contribute to the heatflow. It is recommended that the transistor is mounted on a grounded metallized area of 0.8 mm maximum thickness on the printed-circuit board, equipped with at least 12 (0.5 mm diameter) through metallized holes filled with solder.
A thermal resistance $R_{th(mb-h)}$ of 5 K/W can be achieved if heatsink compound is applied when the transistor is mounted on the printed-circuit board.



Dimensions in mm.

Fig.15 Footprint SOT409A.

HF/VHF power MOS transistor | BLF242

FEATURES

- High power gain
- Low noise
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for professional transmitter applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

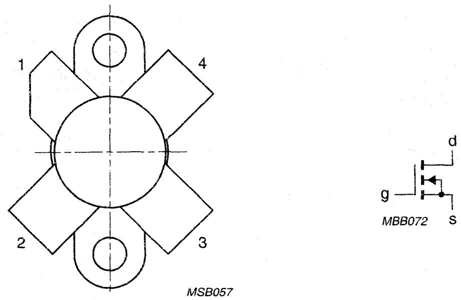


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	5	> 13 typ. 16	> 50 typ. 60

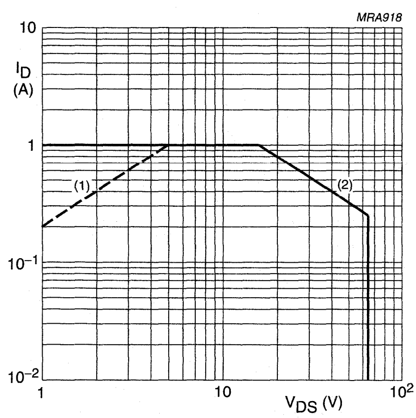
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	16	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

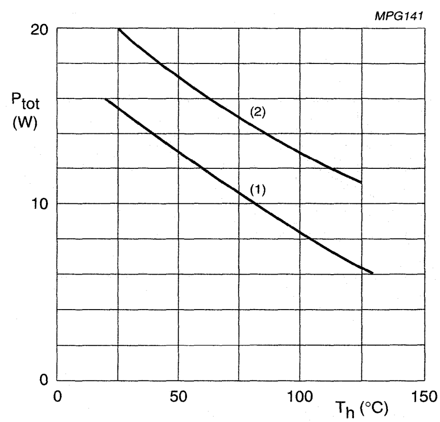
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 16 W	11 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 16 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



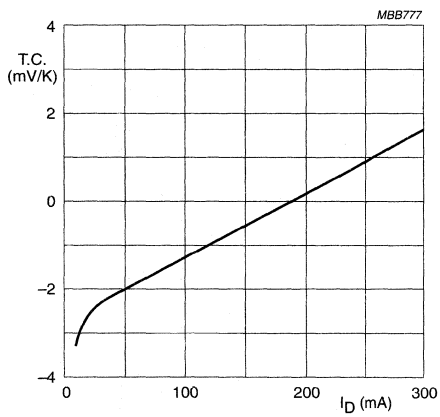
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

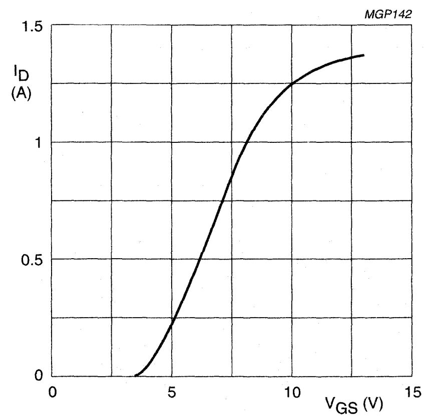
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.1 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	0.16	0.24	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 1 V	–	3.3	5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{GS} = 10 V	–	1.2	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	13	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	9.4	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	1.7	–	pF



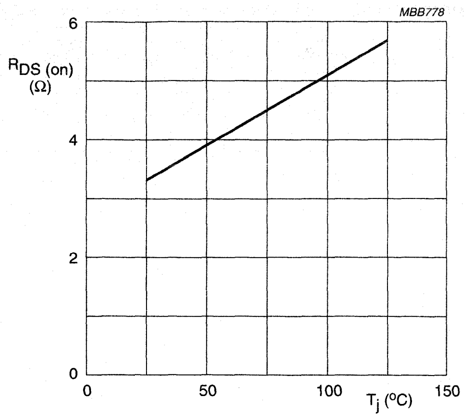
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



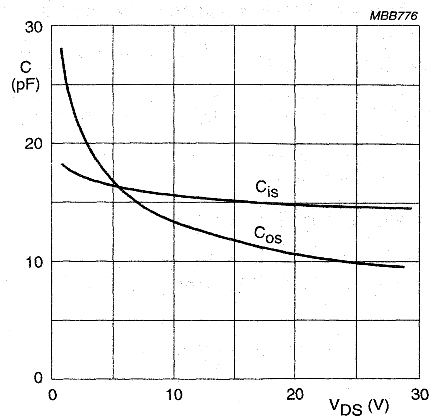
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



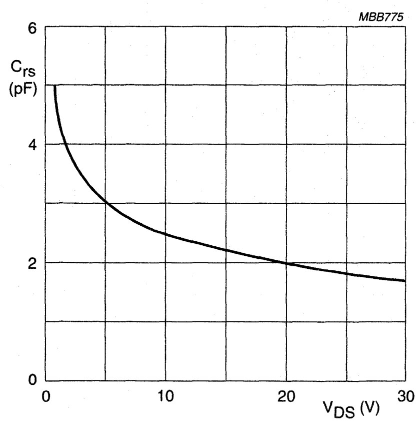
I_D = 0.3 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	R_{GS} (Ω)
CW, class-B	175	28	10	5	> 13 typ. 16	> 50 typ. 60	47

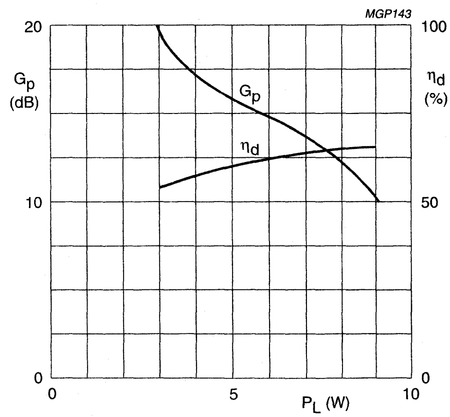
Ruggedness in class-B operation

The BLF242 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f =175 MHz at rated output power.

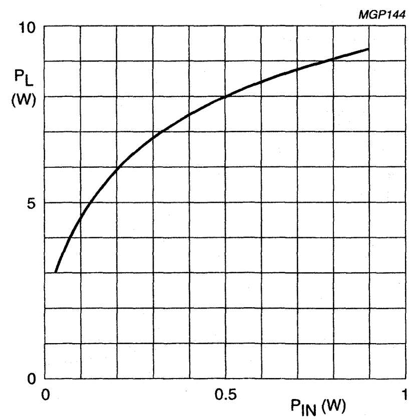
Noise figure (see Fig.11)

V_{DS} = 28 V; I_D = 0.2 A; f = 175 MHz;
R_{GS} = 47 Ω; T_h = 25 °C. Input and output power matched for P_L = 5 W;
F = typ. 5.5 dB.



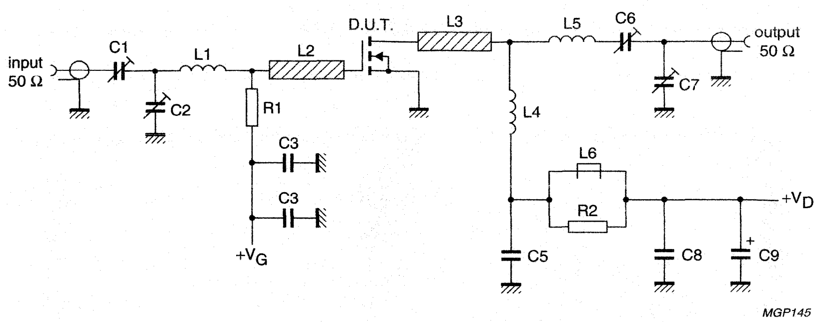
Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA;
R_{GS} = 47 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA;
R_{GS} = 47 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

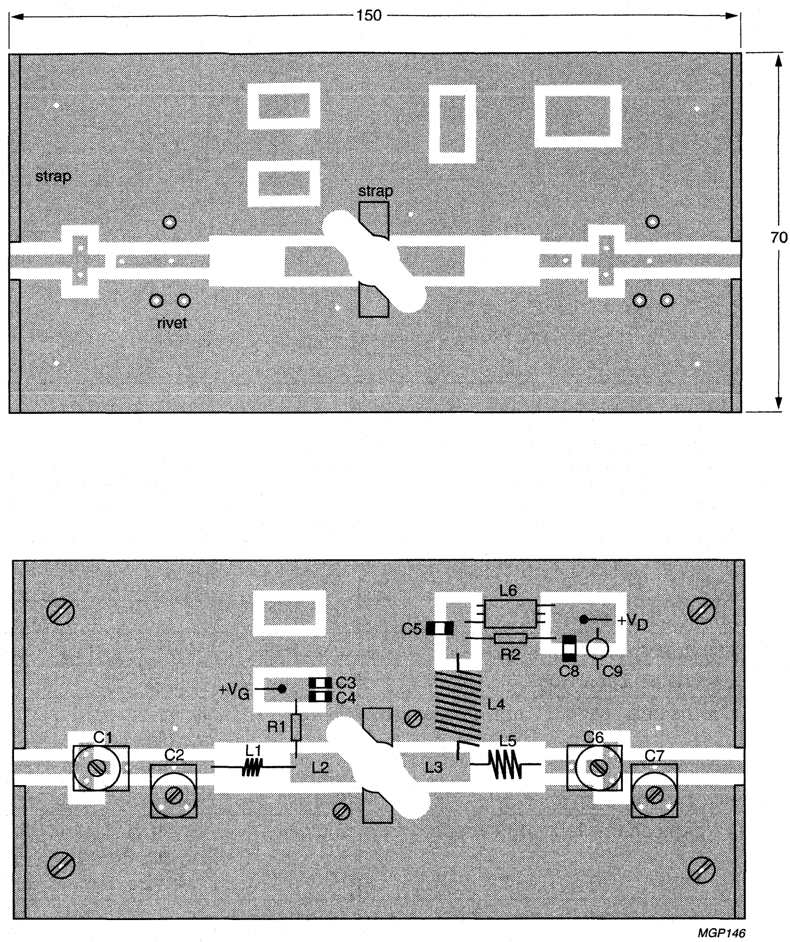
Fig.11 Test circuit for class-B operation.

List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7	film dielectric trimmer	4 to 40 pF		2222 809 08002
C3	multilayer ceramic chip capacitor (note 1)	100 pF		
C4, C8	ceramic chip capacitor	100 nF		2222 852 47104
C6	film dielectric trimmer	5 to 60 pF		2222 809 08003
C9	electrolytic capacitor	2.2 μF, 40 V		
L1	5 turns enamelled 0.7 mm copper wire	53 nH	length 5.4 mm int. dia. 3 mm leads 2 × 5 mm	
L2, L3	stripline (note 2)	30 Ω	10 × 6 mm	
L4	11 turns enamelled 1 mm copper wire	500 nH	length 15.5 mm int. dia. 8 mm leads 2 × 5 mm	
L5	5 turns enamelled 1 mm copper wire	79 nH	length 9.1 mm int. dia. 5 mm leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.5 W metal film resistor	47 Ω		
R2	0.5 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric ($\varepsilon_r = 4.5$), thickness $^1\!/_{16}$ inch.

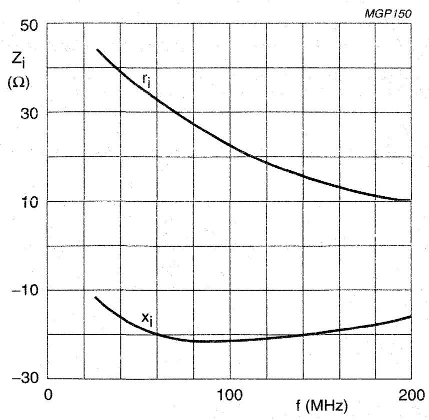


The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by fixing screws, copper straps and hollow rivets at the edges of the board and under the source.

Dimensions in mm.

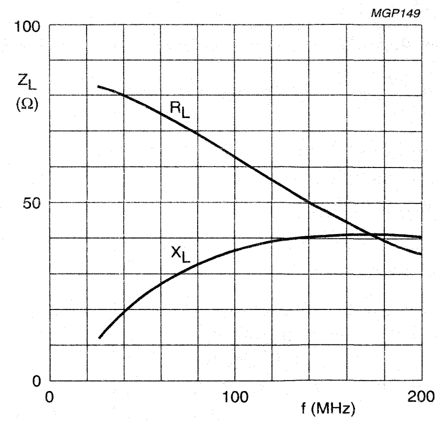
Fig.12 Component layout for 175 MHz class-B test circuit.

HF/VHF power MOS transistor BLF242



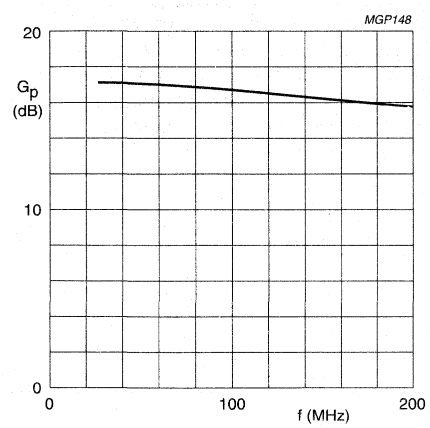
Class-B operation; V_{DS} = 28 V; P_L = 30 W;
R_{GS} = 47 Ω; T_h = 25 °C.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; P_L = 30 W;
R_{GS} = 47 Ω; T_h = 25 °C.

Fig.14 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; P_L = 30 W;
R_{GS} = 47 Ω; T_h = 25 °C.

Fig.15 Power gain as a function of frequency, typical values.

VHF power MOS transistor — BLF244

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

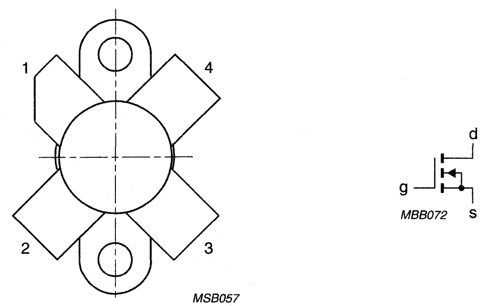


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	15	> 13	> 50

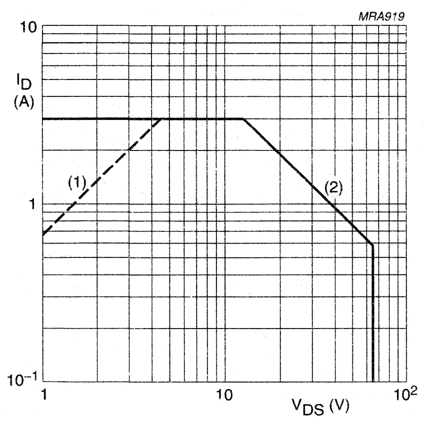
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	3	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	38	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

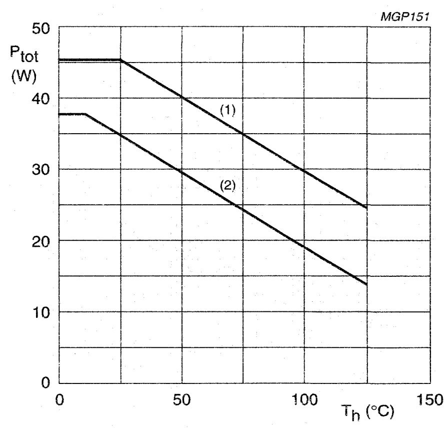
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 38 W	4.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 38 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



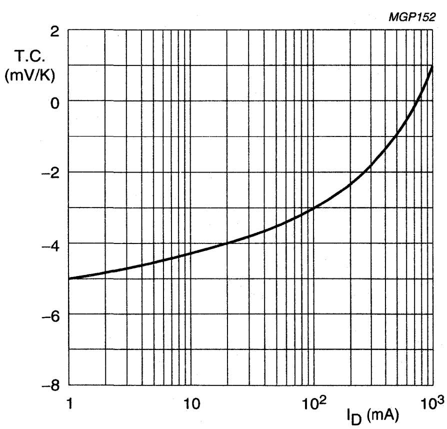
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

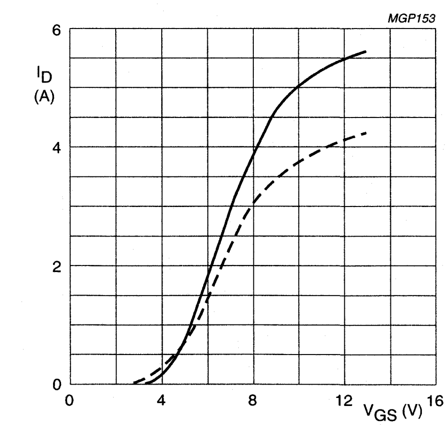
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 5 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 5 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 0.75 A; V_{DS} = 10 V	0.6	–	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.75 A; V_{GS} = 10 V	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	4.5	–	pF
F	noise figure (see Fig. 13)	I_D = 0.5 A; V_{DS} = 28 V; R1 = 23 Ω; T_h = 25 °C; f = 175 MHz; $R_{th\ mb\text{-}h}$ = 0.3 K/W	–	4.3	–	dB



V_{DS} = 10 V; valid for T_j = 25 to 125 °C.

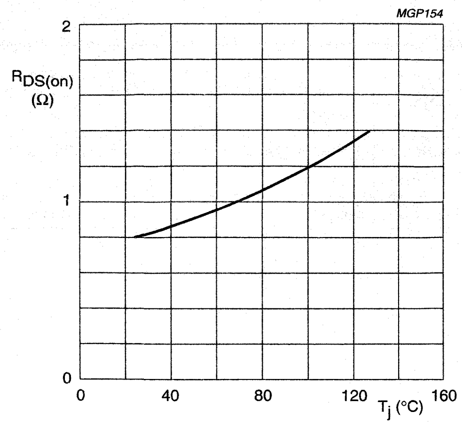
Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



V_{DS} = 10 V.
solid line: T_j = 25 °C.
dotted line: T_j = 125 °C.

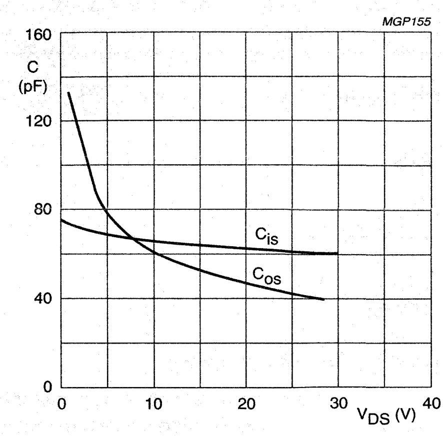
Fig.5 Drain current as a function of gate-source voltage, typical values.

VHF power MOS transistor BLF244



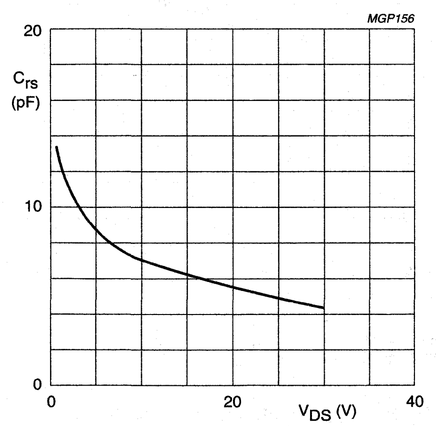
V_{GS} = 10 V; I_D = 0.75 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 3 K/W; unless otherwise specified.
RF performance in CW operation in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	Z_i (Ω) (note 1)	Z_L (Ω)	R1 (Ω)
CW, class-B	175	28	25	15	> 13 typ. 17	> 50 typ. 65	3.0 – j4.0	6.3 + j9.8	46.4//46.4
	175	12.5	25	6	typ. 15	typ. 60	3.0 – j4.0	4.5 + j3.3	100

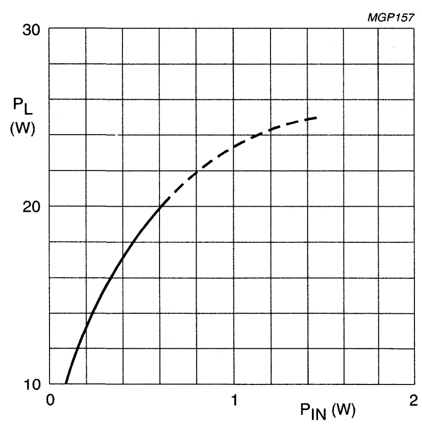
Note

1. R1 included.

Ruggedness in class-B operation

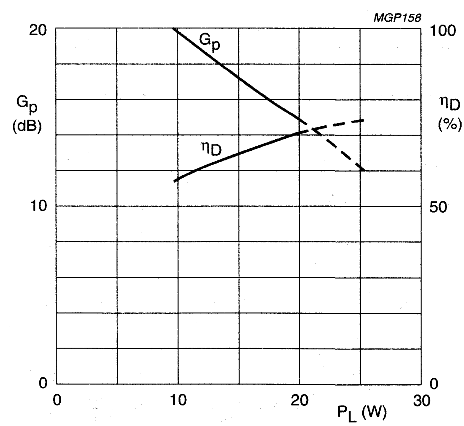
The BLF244 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; at rated load power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.9 Load power as a function of input power, typical values.

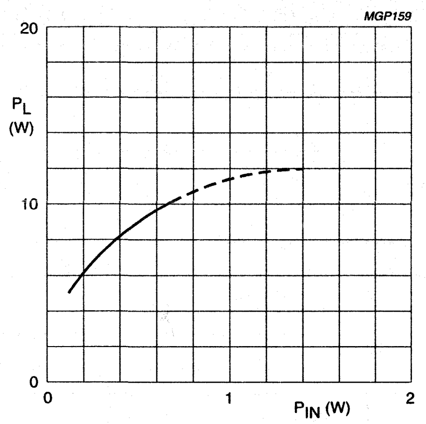


Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.10 Power gain and efficiency as functions of load power, typical values.

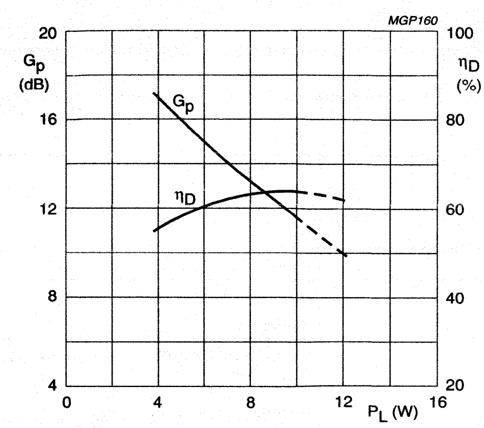
VHF power MOS transistor

BLF244



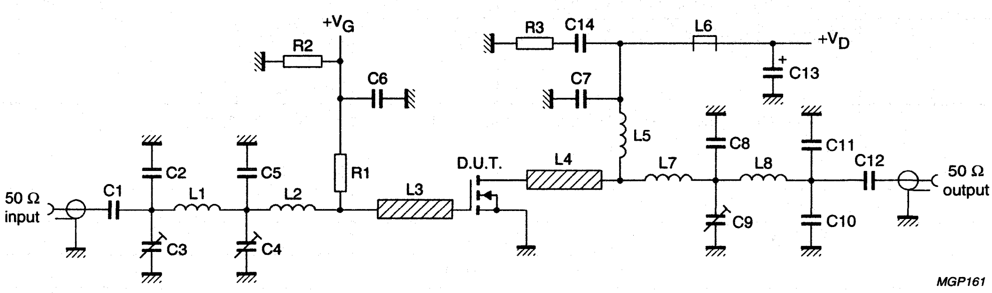
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.11 Load power as a function of input power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 25 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.12 Power gain and efficiency as functions of load power, typical values.



f = 175 MHz.

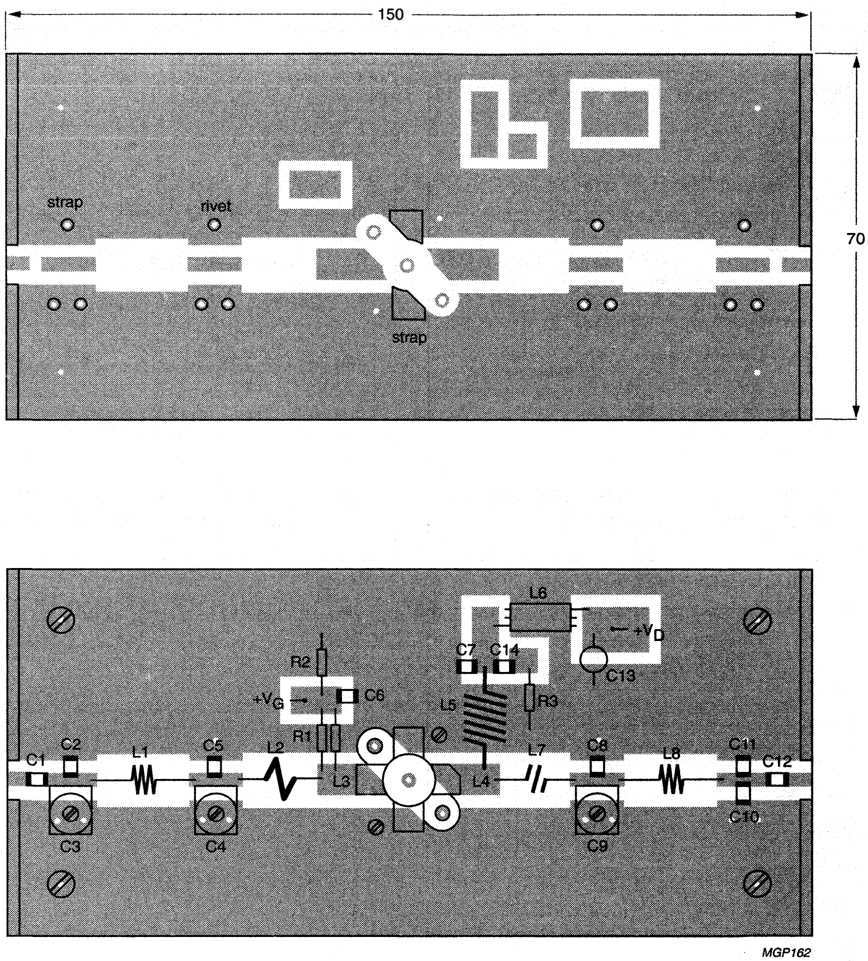
Fig.13 Test circuit for class-B operation.

List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C12	multilayer ceramic chip capacitor (note 1)	680 nF		
C2	multilayer ceramic chip capacitor (note 1)	20 pF		
C3, C4, C9	film dielectric trimmer	5 to 60 pF		2222 809 08003
C5	multilayer ceramic chip capacitor (note 1)	75 pF		
C6	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor (note 1)	100 pF		
C8	multilayer ceramic chip capacitor (note 1)	47 pF		
C10, C11	multilayer ceramic chip capacitor (note 1)	11 pF		
C13	solid tantalum capacitor	2.2 μF		
C14	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	4 turns enamelled 1 mm copper wire	32 nH	length 6.3 mm int. dia. 3 mm leads 2 × 5 mm	
L2	1 turn enamelled 1 mm copper wire	12.2 nH	int. dia. 5.6 mm leads 2 × 5 mm	
L3, L4	stripline (note 2)	30 Ω	15 × 6 mm	
L5	6 turns enamelled 1 mm copper wire	119 nH	length 10.4 mm int. dia. 6 mm leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
L7	2 turns enamelled 1 mm copper wire	19 nH	length 2.4 mm int. dia. 3 mm leads 2 × 5 mm	
L8	4 turns enamelled 1 mm copper wire	28.5 nH	length 8.5 mm int. dia. 3 mm leads 2 × 5 mm	
R1	metal film resistor (note 3)			
R2	0.4 W metal film resistor	1 MΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric ($\varepsilon_r = 4.5$), thickness $^1\!/_{16}$ inch.
3. Refer to Application Information for value.



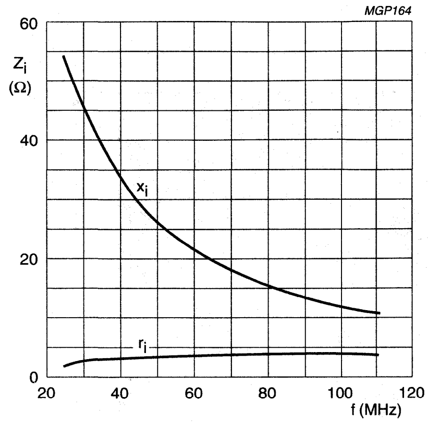
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being unetched copper to serve as ground plane. Earth connections are made by fixing screws, copper straps and hollow rivets under the sources and around the edges to provide a direct contact between the copper on the component side and the ground plane.

Dimensions in mm.

Fig.14 Component layout for 175 MHz class-B test circuit.

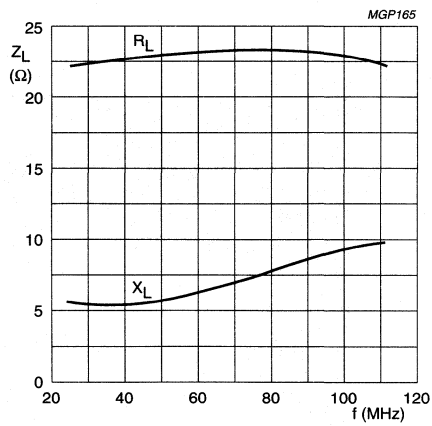
VHF power MOS transistor

BLF244



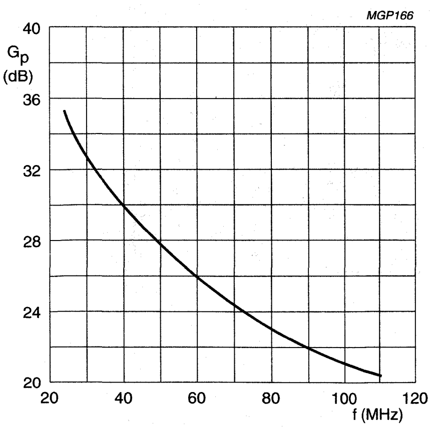
Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.15 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.16 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.17 Power gain as function of frequency, typical values.

VHF power MOS transistor BLF245

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PIN CONFIGURATION

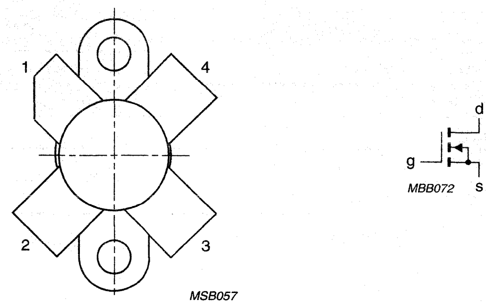


Fig.1 Simplified outline and symbol.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	30	> 13	> 50

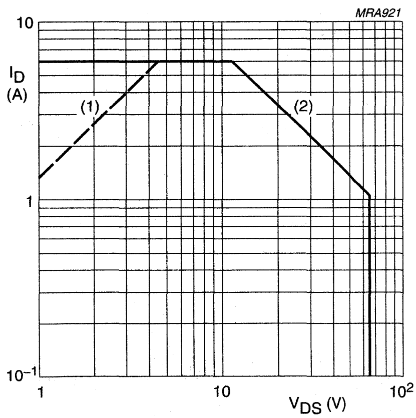
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	$V_{GS} = 0$	–	65	V
$\pm V_{GS}$	gate-source voltage	$V_{DS} = 0$	–	20	V
I_D	DC drain current		–	6	A
P_{tot}	total power dissipation	up to $T_{mb} = 25$ °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

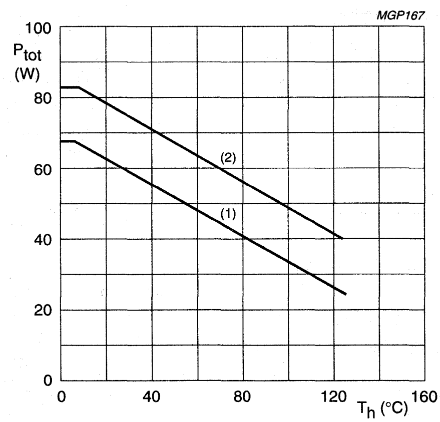
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25$ °C; $P_{tot} = 68$ W	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	$T_{mb} = 25$ °C; $P_{tot} = 68$ W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) $T_{mb} = 25$ °C.

Fig.2 DC SOAR.



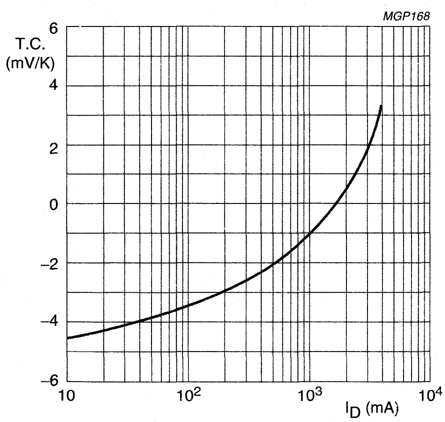
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

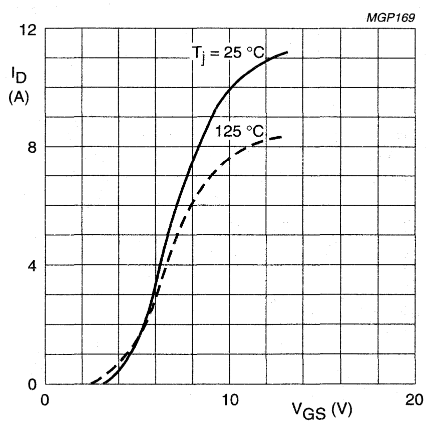
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	1.9	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	7	–	pF
F	noise figure (see Fig.14)	input and output power matched for: I_D = 1 A; V_{DS} = 28 V; P_L = 30 W; R1 = 1 kΩ; T_h = 25 °C; f = 175 MHz	–	2	–	dB



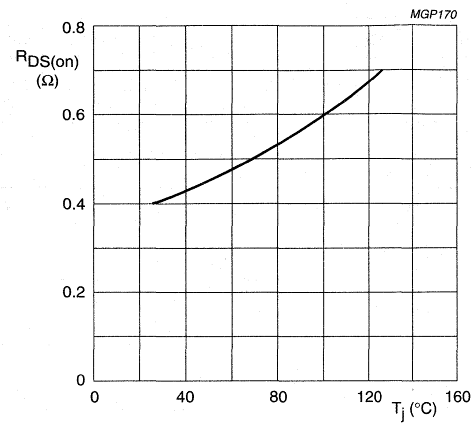
V_{DS} = 10 V; valid for T_j = 25 to 125 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



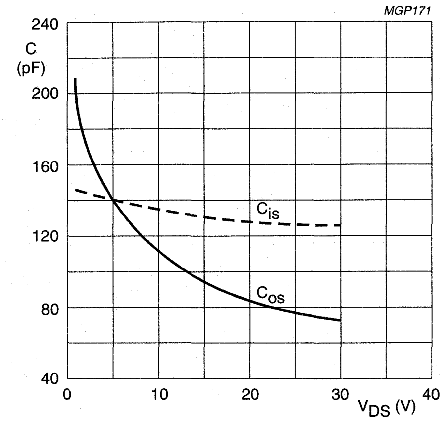
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



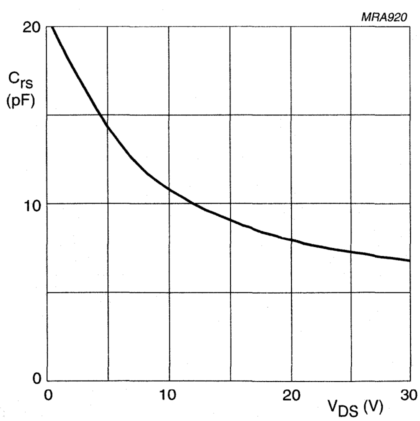
V_{GS} = 10 V;
I_D = 1.5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; R1 = 1 kΩ.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	Z_i (Ω) (note 1)	Z_L (Ω)
CW, class-B	175	28	50	30	> 13 typ. 15.5	< 50 typ. 67	2.0 − j2.7	3.9 + j4.4
	175	12.5	50	12	typ. 12	typ. 66	2.4 − j2.5	3.8 + j1.3

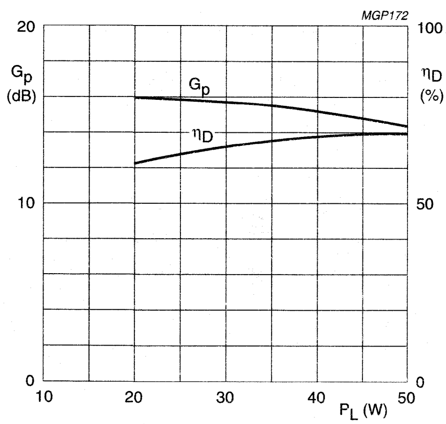
Note

1. R1 included.

Ruggedness in class-B operation

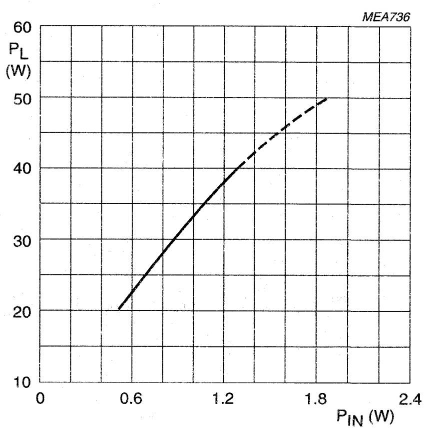
The BLF245 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; at rated load power.



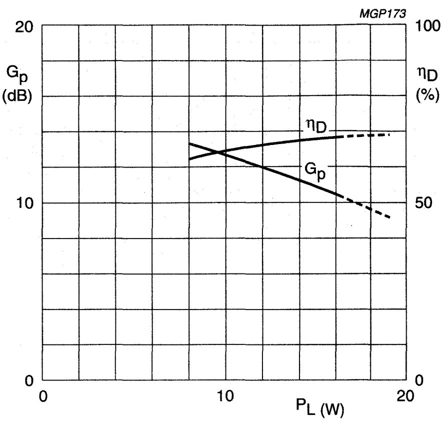
Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.9 Power gain and efficiency as functions of load power, typical values.



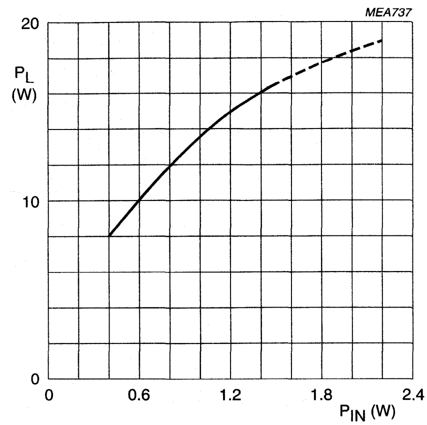
Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.10 Load power as a function of input power, typical values.



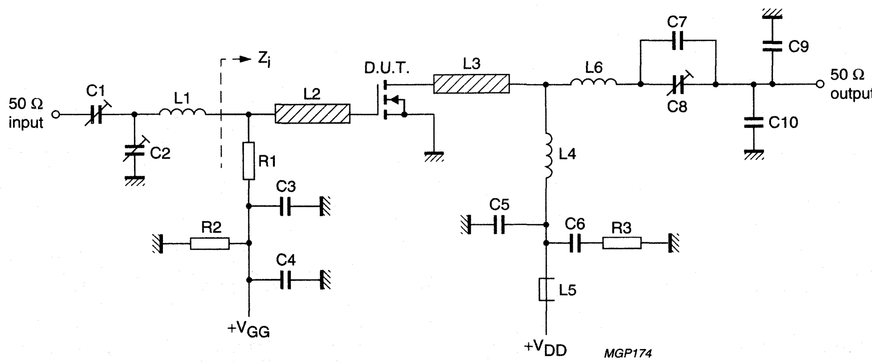
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.11 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.12 Load power as a function of input power, typical values.



f = 175 MHz.

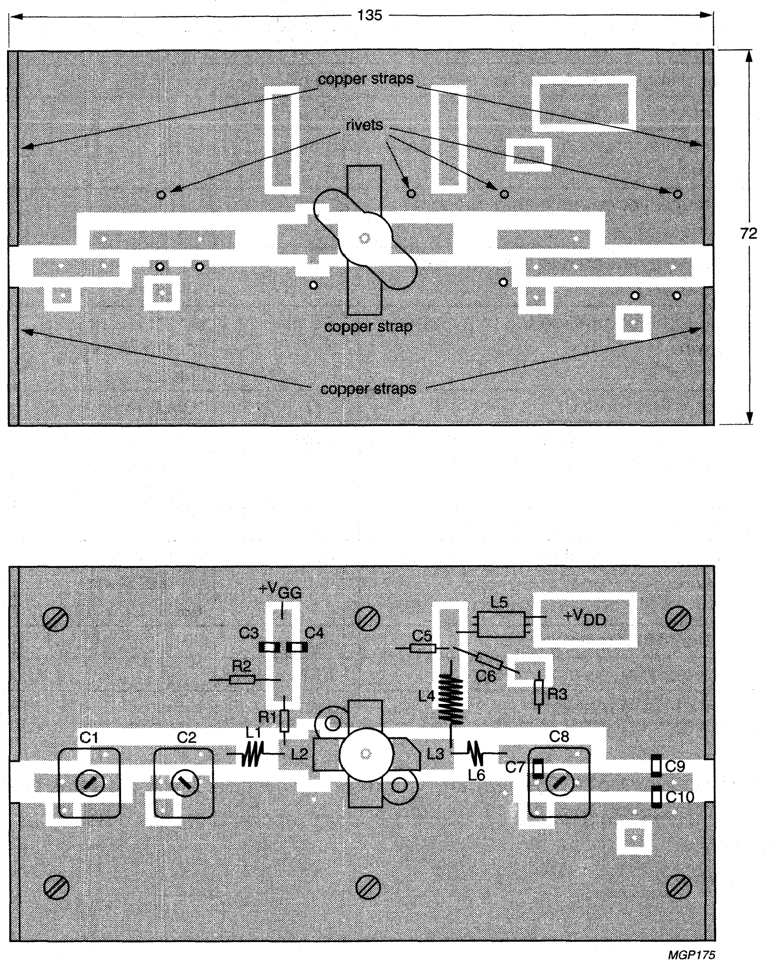
Fig.13 Test circuit for class-B operation.

List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	4 to 40 pF		2222 809 07008
C2, C8	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3	multilayer ceramic chip capacitor	100 pF		2222 854 13101
C4, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5	ceramic capacitor	100 pF		2222 680 10101
C7	multilayer ceramic chip capacitor (note 1)	18 pF		
C9	multilayer ceramic chip capacitor (note 1)	27 pF		
C10	multilayer ceramic chip capacitor (note 1)	24 pF		
L1	3 turns enamelled 0.5 mm copper wire	13.5 nH	length 3.5 mm int. dia. 2 mm leads 2 × 2 mm	
L2, L3	stripline (note 2)	30 Ω	10 × 6 mm	
L4	6 turns enamelled 1.5 mm copper wire	98 nH	length 12.5 mm int. dia. 5 mm leads 2 × 2 mm	
L5	grade 3B Ferroxcube RF choke			4312 020 36640
L6	2 turns enamelled 1.5 mm copper wire	24.5 nH	length 4 mm int. dia. 5 mm leads 2 × 2 mm	
R1	metal film resistor	1 kΩ		
R2	metal film resistor	1 MΩ		
R3	metal film resistor	10 Ω		

Notes

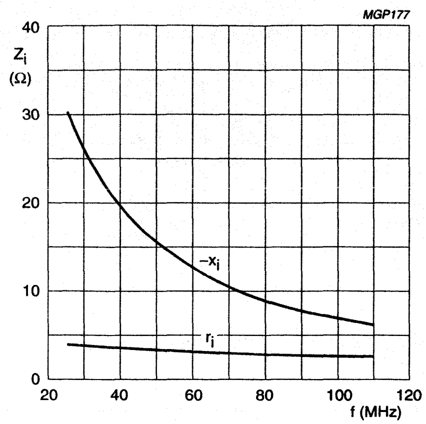
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are mounted on a double copper-clad PCB with epoxy fibre-glass dielectric ($\varepsilon_r = 4.5$), thickness $^1/_{16}$ inch.



The circuit and components are situated on one side of the epoxy fiber-glass board; the other side is unetched copper and serves as an earth. Earth connections are made by means of fixing screws, hollow rivets and copper straps under the sources and around the edges, to provide a direct contact between the copper on the component side and the ground plane.

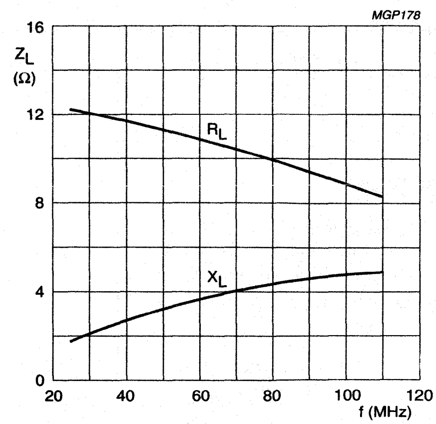
Dimensions in mm.

Fig.14 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.15 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.16 Load impedance as a function of frequency (series components), typical values.

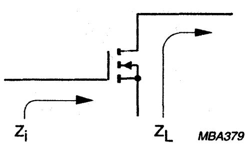
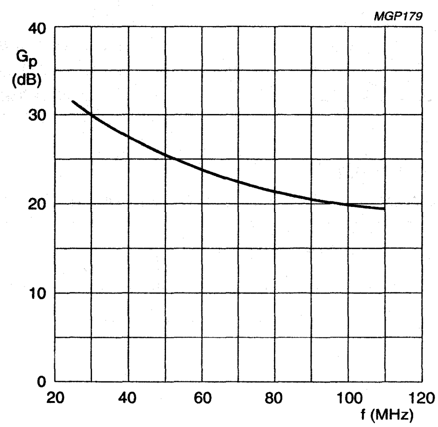


Fig.17 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.18 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor | BLF245B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

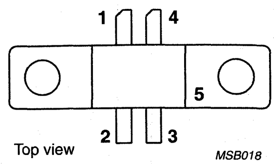
Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT279 balanced flange envelope, with a ceramic cap. The mounting flange provides the common source connection for the transistors.

PINNING - SOT279

PIN	DESCRIPTION
1	gate 1
2	drain 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION



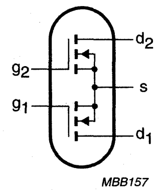


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	175	28	30	> 14	> 55

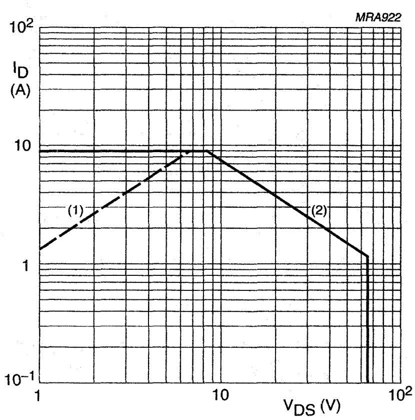
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	75	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

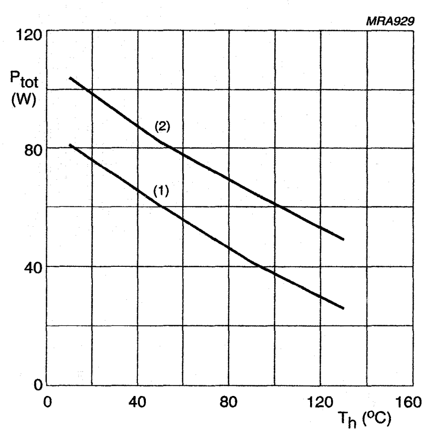
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	2.3 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.3 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



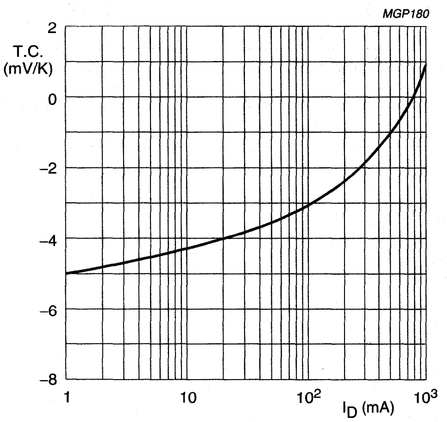
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (PER SECTION)

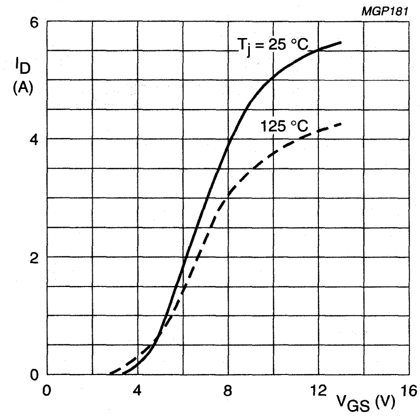
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 5 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 5 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.75 A; V_{DS} = 10 V	600	850	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.75 A; V_{GS} = 10 V	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	4.5	–	pF



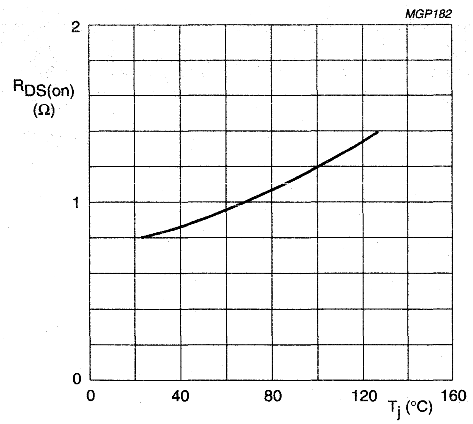
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



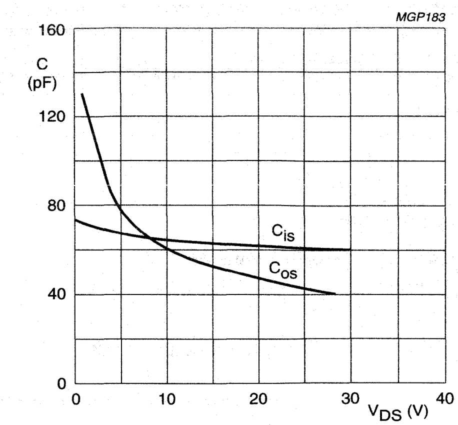
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



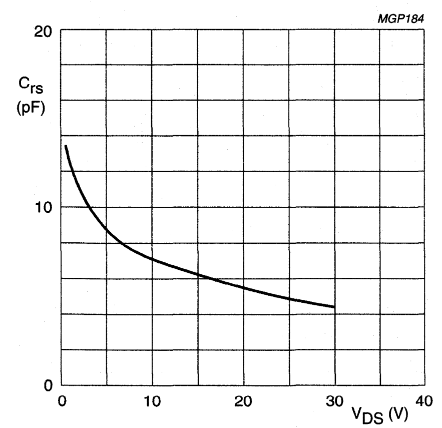
I_D = 0.75 A; V_{GS} = 10 V

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

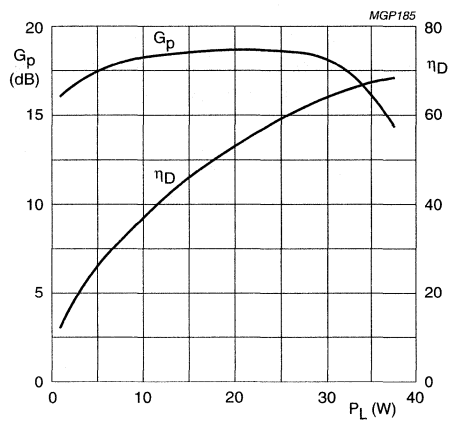
T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	175	28	2 × 25	30	> 14 typ. 18	> 55 typ. 65

Ruggedness in class-B operation

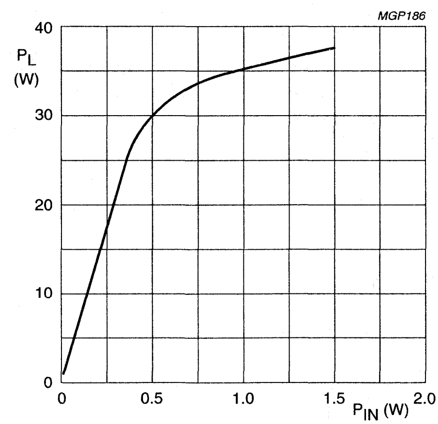
The BLF245B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:

V_{DS} = 28 V, f = 175 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
Z_L = 8.8 + j12.7 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of output power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
Z_L = 8.8 + j12.7 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.

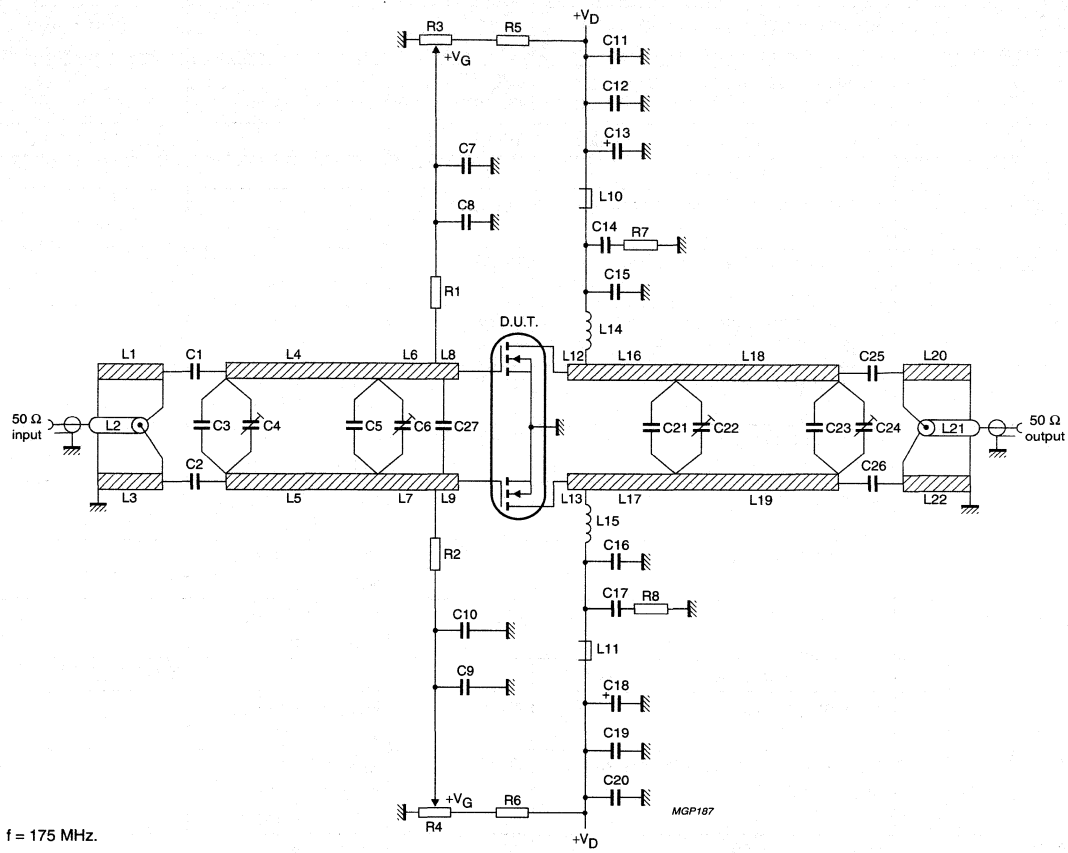


Fig.11 Test circuit for class-B operation.

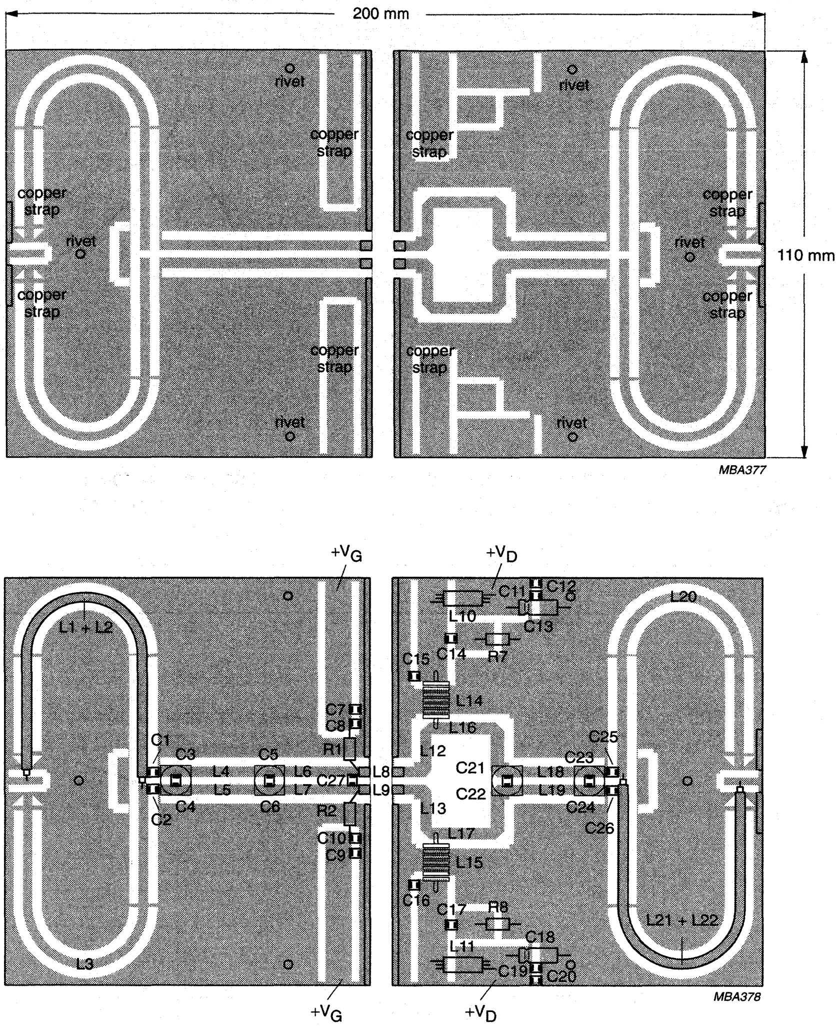
List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	270 pF		
C3	multilayer ceramic chip capacitor (note 1)	24 pF		
C4	film dielectric trimmer	4 to 60 pF		2222 809 08002
C5, C25, C26	multilayer ceramic chip capacitor (note 1)	91 pF		
C6, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C8, C10	multilayer ceramic chip capacitor (note 1)	680 pF		
C11, C20	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 μF, 63 V		
C15, C16	multilayer ceramic chip capacitor (note 1)	100 pF		
C21, C27	multilayer ceramic chip capacitor (note 1)	75 pF		
C23	multilayer ceramic chip capacitor (note 1)	36 pF		
L1, L3, L20, L22	stripline (note 2)	55 Ω	length 111 mm width 2.5 mm	
L2, L21	semi-rigid cable	50 Ω	length 111 mm ext. dia. 2.2 mm	
L4, L5	stripline (note 2)	49.5 Ω	length 28 mm width 3 mm	
L6, L7	stripline (note 2)	49.5 Ω	length 22.5 mm width 3 mm	
L8, L9	stripline (note 2)	49.5 Ω	length 4.5 mm width 3 mm	
L10, L11	grade 3B Ferroxcube RF choke			4312 020 36642
L12, L13	stripline (note 2)	49.5 Ω	length 21 mm width 3 mm	
L14, L15	4 turns enamelled 1 mm copper wire	70 nH	length 9 mm int. dia. 6 mm leads 2 × 5 mm	
L16, L17	stripline (note 2)	49.5 Ω	length 30 mm width 3 mm	
L18, L19	stripline (note 2)	49.5 Ω	length 26 mm width 3 mm	
R1, R2	0.4 W metal film resistor	10 Ω		
R3, R4	10 turns potentiometer	50 Ω		
R5, R6	0.4 W metal film resistor	205 kΩ		
R7, R8	0.4 W metal film resistor	10 Ω		

Notes

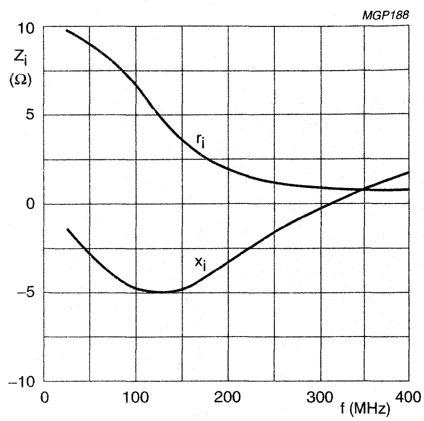
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric ($\varepsilon_r = 4.5$), thickness $1/16$ inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.



The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

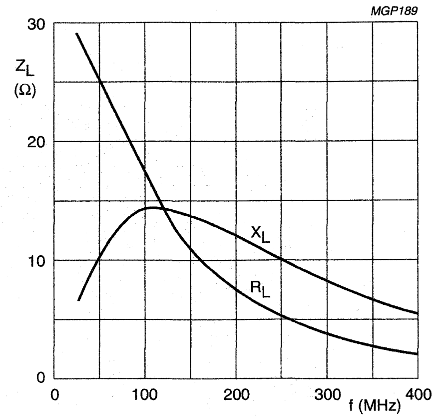
Fig.12 Component layout for 175 MHz test circuit.

VHF push-pull power MOS transistor BLF245B



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

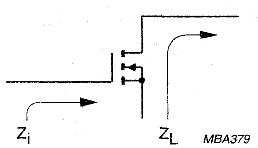
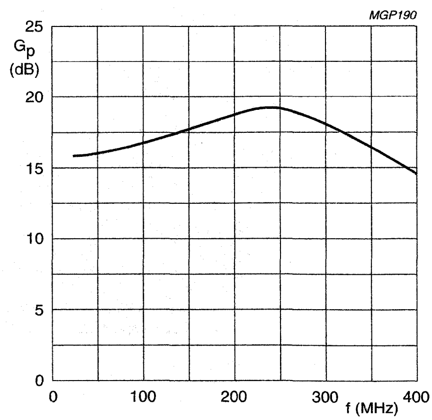


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

VHF power MOS transistor BLF246

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

APPLICATIONS

- Large signal amplifier applications in the VHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT121 flange package, with a ceramic cap. All leads are isolated from the flange. A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the General section of Data Handbook SC19a for further information.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT121

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	s	source
3	g	gate
4	s	source

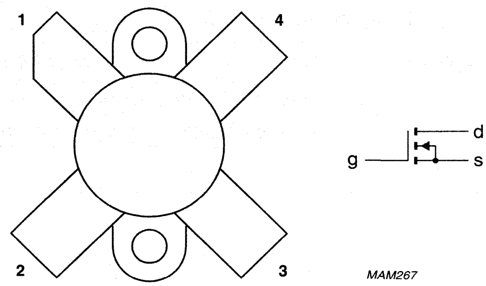


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	28	80	≥16	≥55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

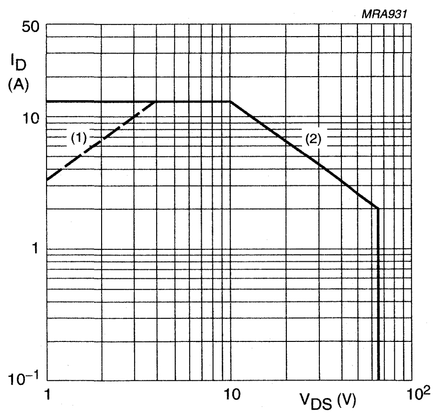
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	DC drain current		–	13	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	130	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

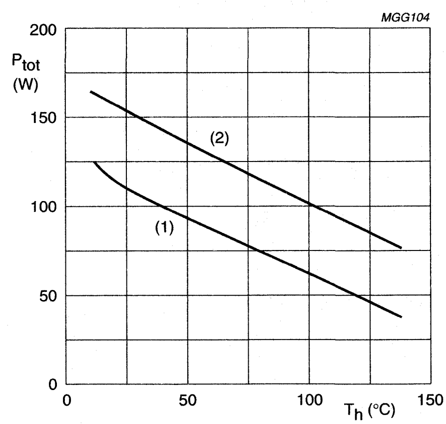
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	1.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.2	K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



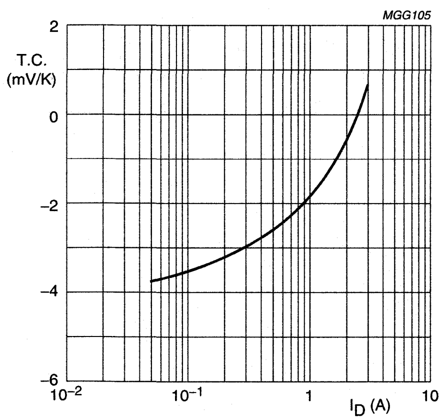
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

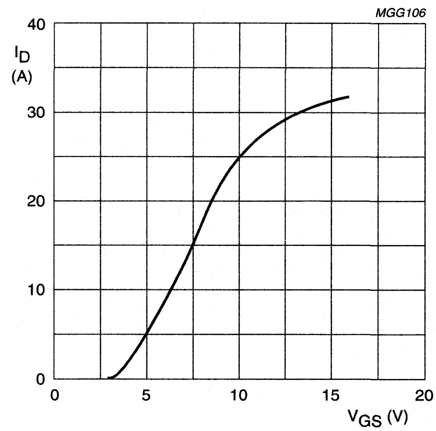
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 2.5 A or 5 A; V_{DS} = 10 V	3	4.2	–	S
R_{DSon}	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	22	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	225	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	180	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF



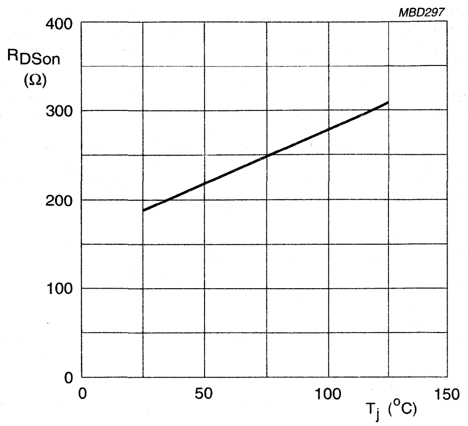
V_{DS} = 10 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



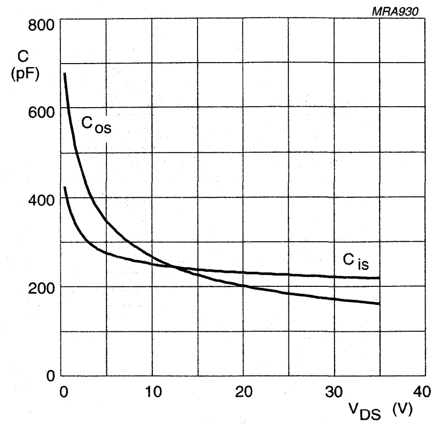
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



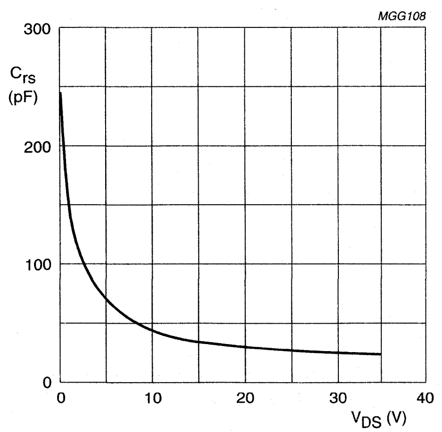
V_{GS} = 10 V; I_D = 5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION

RF performance in CW operation in a common source test circuit.
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; R_{GS} = 12 Ω unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	28	0.1	80	>16	>55
CW, class-B	108	28	0.1	80	typ. 18	typ. 65
CW, class-C	108	28	0(1)	80	typ. 15	typ. 72

Note

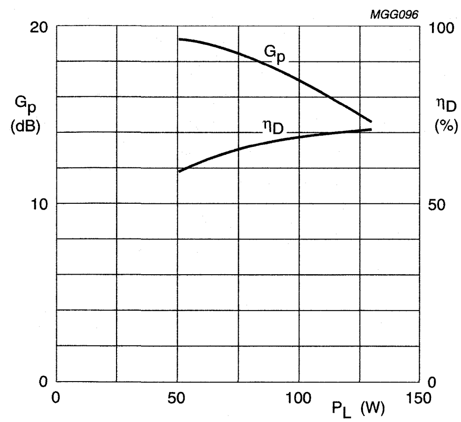
1. V_{GS} = 0 (class-C).

Ruggedness in class-B operation

The BLF246 is capable of withstanding a load mismatch corresponding to VSWR = 50: 1 through all phases under the following conditions: V_{DS} = 28 V; f = 108 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W at rated output power.

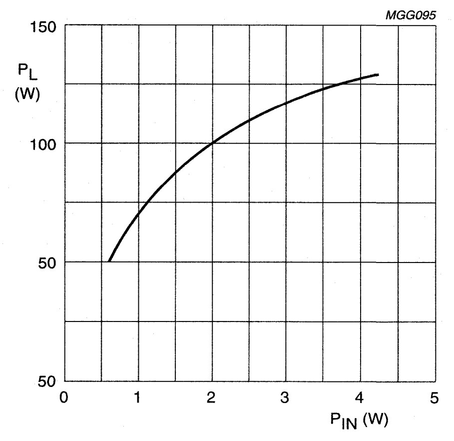
Noise figure

Measured with 80 W power-matched source and load in the test circuit (see Fig.9) with V_{DS} = 28 V; I_D = 2 A; f = 108 MHz; R_{GS} = 27 Ω; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; F = typ. 3 dB.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A; R_{GS} = 12 Ω;
f = 108 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A; R_{GS} = 12 Ω;
f = 108 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.10 Load power as a function of input power, typical values.

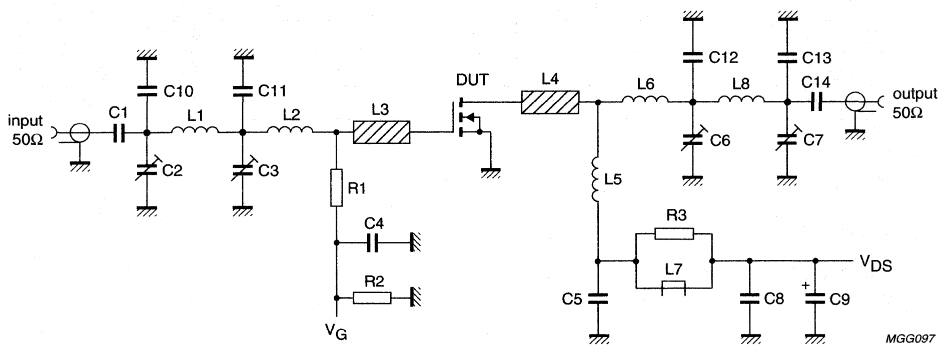


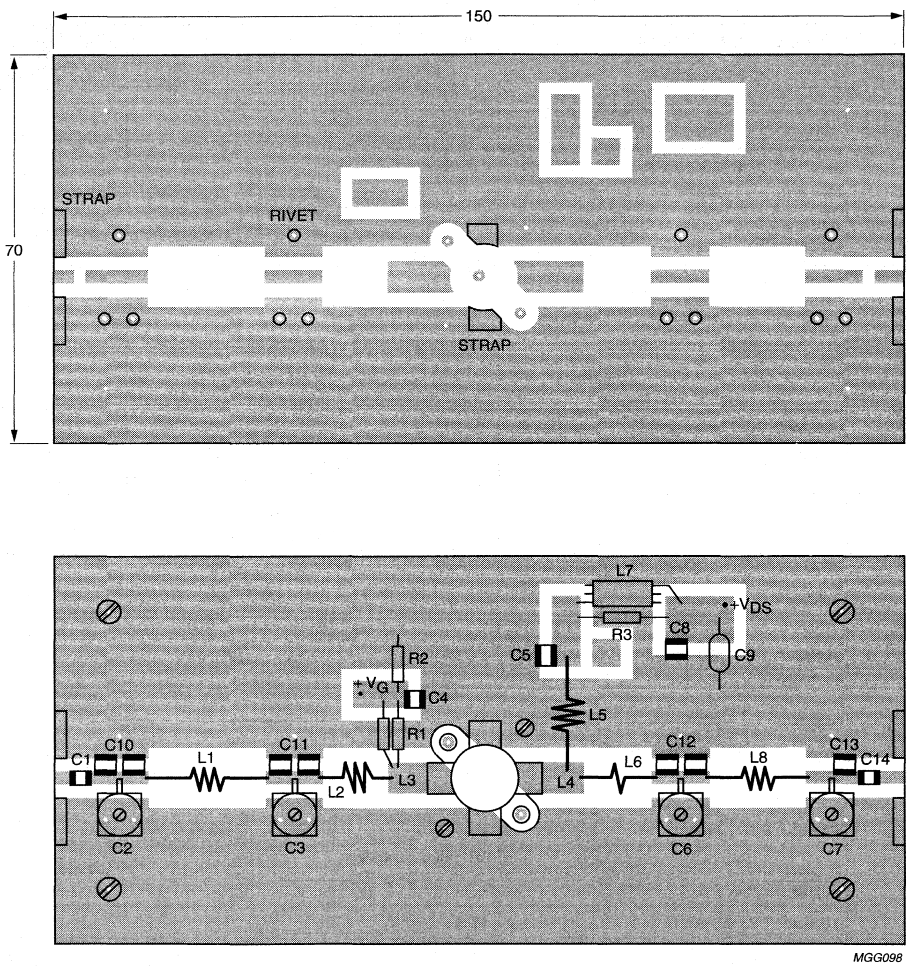
Fig.11 Test circuit for class-B operation at 108 MHz.

List of components (see Figs 11 and 12).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C4, C5, C8, C14	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C2, C3, C6, C7	film dielectric trimmer	5 to 60 pF		2222 809 08003
C9	electrolytic capacitor	2.2 μF, 63 V		2222 030 38228
C10	multilayer ceramic chip capacitor; note 1	68 pF + 39 pF in parallel		
C11	multilayer ceramic chip capacitor; note 1	69 pF + 100 pF in parallel		
C12	multilayer ceramic chip capacitor; note 1	2x 100 pF in parallel		
C13	multilayer ceramic chip capacitor; note 1	62 pF		
L1	5 turns enamelled 0.6 mm copper wire	52 nH	length 6.5 mm int. dia. 3 mm leads 2 × 10 mm	
L2	2 turns enamelled 0.6 mm copper wire	19 nH	length 3.5 mm int. dia. 3 mm leads 2 × 7.5 mm	
L3, L4	stripline; note 2	31 Ω	length 13 mm width 6 mm	
L5	3 turns enamelled 1.6 mm copper wire	36 nH	length 12 mm int. dia. 6 mm leads 2 × 5 mm	
L6	hairpin of enamelled 1.6 mm copper wire	14 nH	length 20 mm	
L7	grade 3B Ferroxcube HF choke			4312 020 36640
L8	3 turns enamelled 1.6 mm copper wire	52 nH	length 8 mm int. dia. 6 mm leads 2 × 9 mm	
R1	metal film resistor	2 × 24 Ω in parallel, 0.4 W		
R2	metal film resistor	100 kΩ, 0.4 W		
R3	metal film resistor	10 Ω, 0.4 W		

Notes

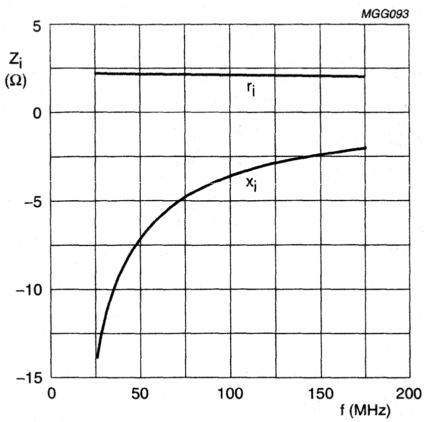
1. American Technical Ceramics capacitor, type 100B or other capacitor of the same quality.
2. The striplines are mounted on a double copper-clad PCB with epoxy fibre-glass dielectric (ε_r = 4.5), thickness 1.6 mm.



Dimensions in mm.

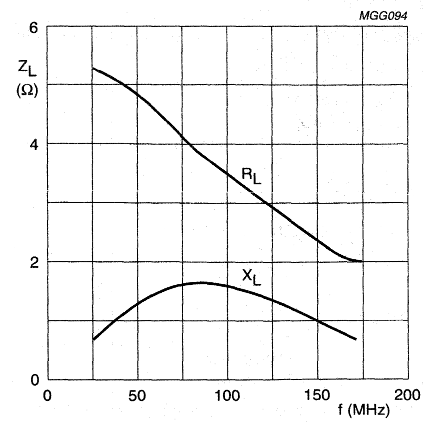
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of hollow rivets, whilst under the source leads, copper straps are used for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 108 MHz class-B test circuit.



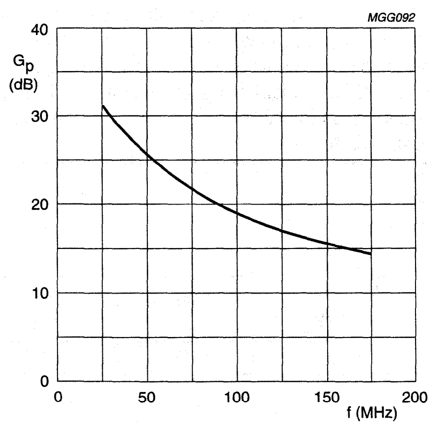
Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A; R_{GS} = 12 Ω;
P_L = 80 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A; R_{GS} = 12 Ω;
P_L = 80 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.14 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A; R_{GS} = 12 Ω;
P_L = 80 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.15 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor | BLF246B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

Large signal applications in the VHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor encapsulated in an 8-lead SOT161A balanced flange package with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT161A

PIN	DESCRIPTION
1	source
2	source
3	drain 1
4	gate 1
5	drain 2
6	gate 2
7	source
8	source

PIN CONFIGURATION

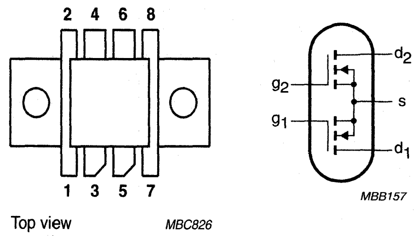


Fig.1 Simplified outline and symbol.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	175	28	60	>14	>55

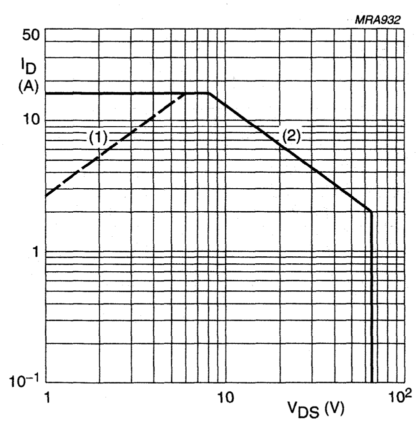
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	8	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C total device; both sections equally loaded	–	130	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	200	°C

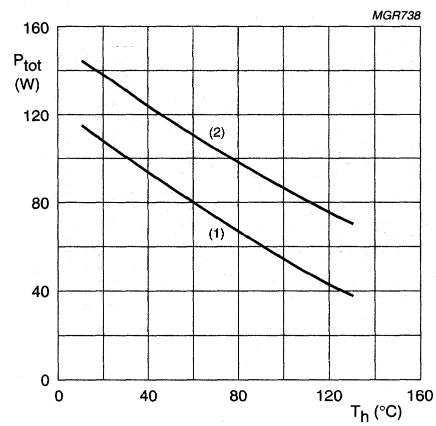
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25	K/W



(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



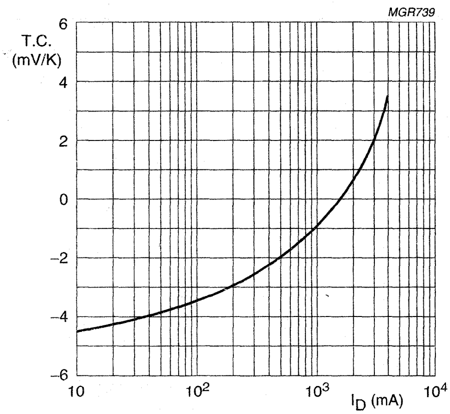
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

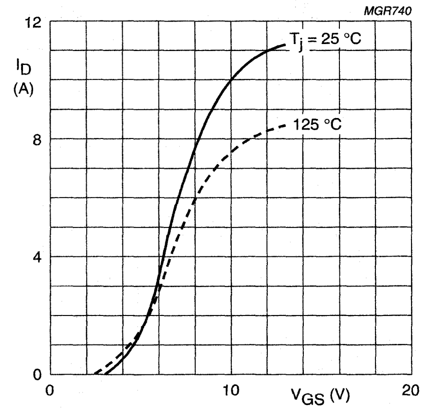
$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 10$ mA	65	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 28$ V	–	–	2	mA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm20$ V; $V_{DS} = 0$	–	–	1	μA
V_{GSth}	gate-source threshold voltage	$I_D = 10$ mA; $V_{DS} = 10$ V	2	–	4.5	V
g_{fs}	forward transconductance	$I_D = 1.5$ A; $V_{DS} = 10$ V	1.2	1.8	–	S
R_{DSon}	drain-source on-state resistance	$I_D = 1.5$ A; $V_{GS} = 10$ V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	$V_{GS} = 10$ V; $V_{DS} = 10$ V	–	10	–	A
C_{is}	input capacitance	$V_{GS} = 0$; $V_{DS} = 28$ V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	$V_{GS} = 0$; $V_{DS} = 28$ V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 28$ V; f = 1 MHz	–	11	–	pF



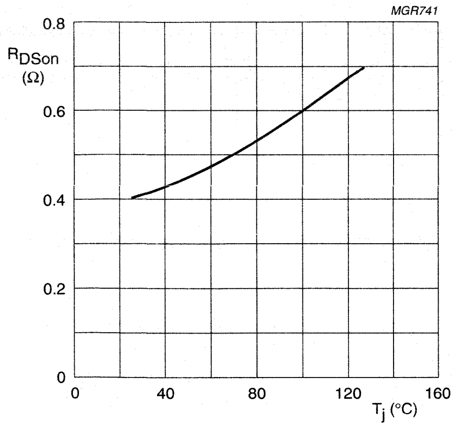
$V_{DS} = 10$ V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



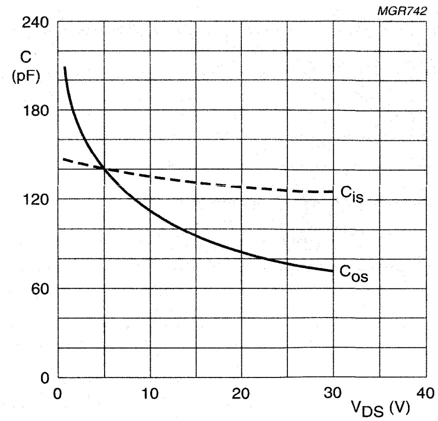
$V_{DS} = 10$ V.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



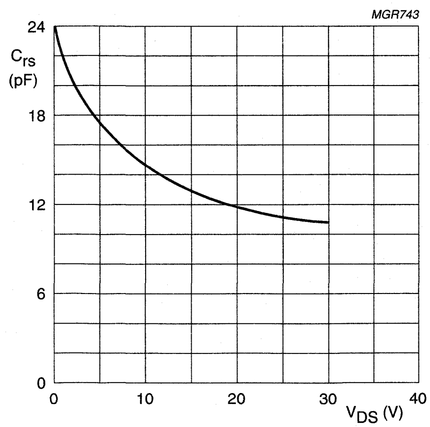
V_{GS} = 10 V; I_D = 1.5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

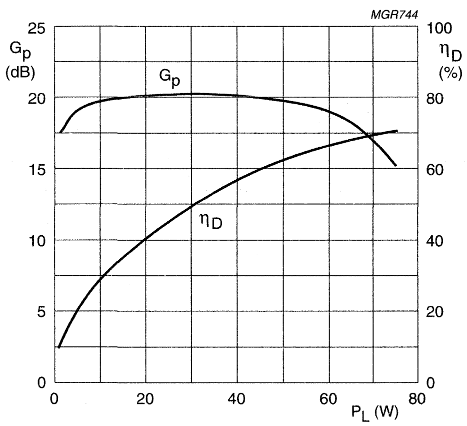
APPLICATION INFORMATION

RF performance in CW operation in a push-pull, common source, class-B circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.25 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	2 × 50	60	>14 typ. 19	>55 typ. 65

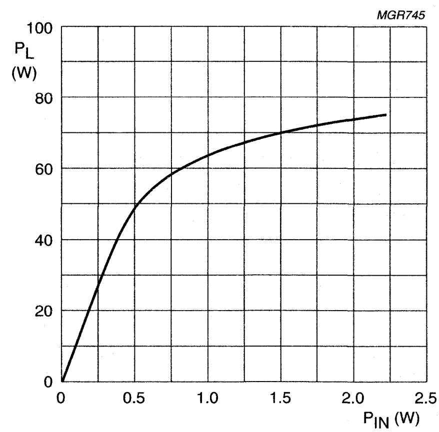
Ruggedness in class-B operation

The BLF246B is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 175 MHz at rated output power.



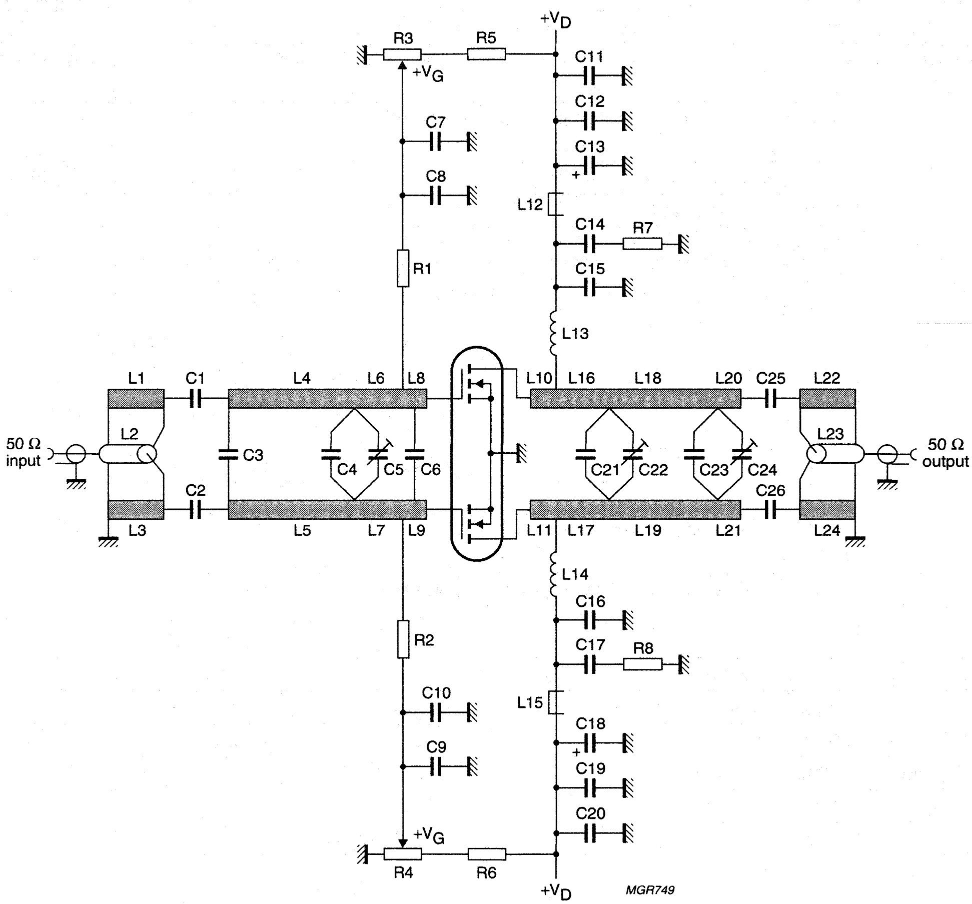
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA; Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as a function of load power; typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA; Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power; typical values per section.



f = 175 MHz.

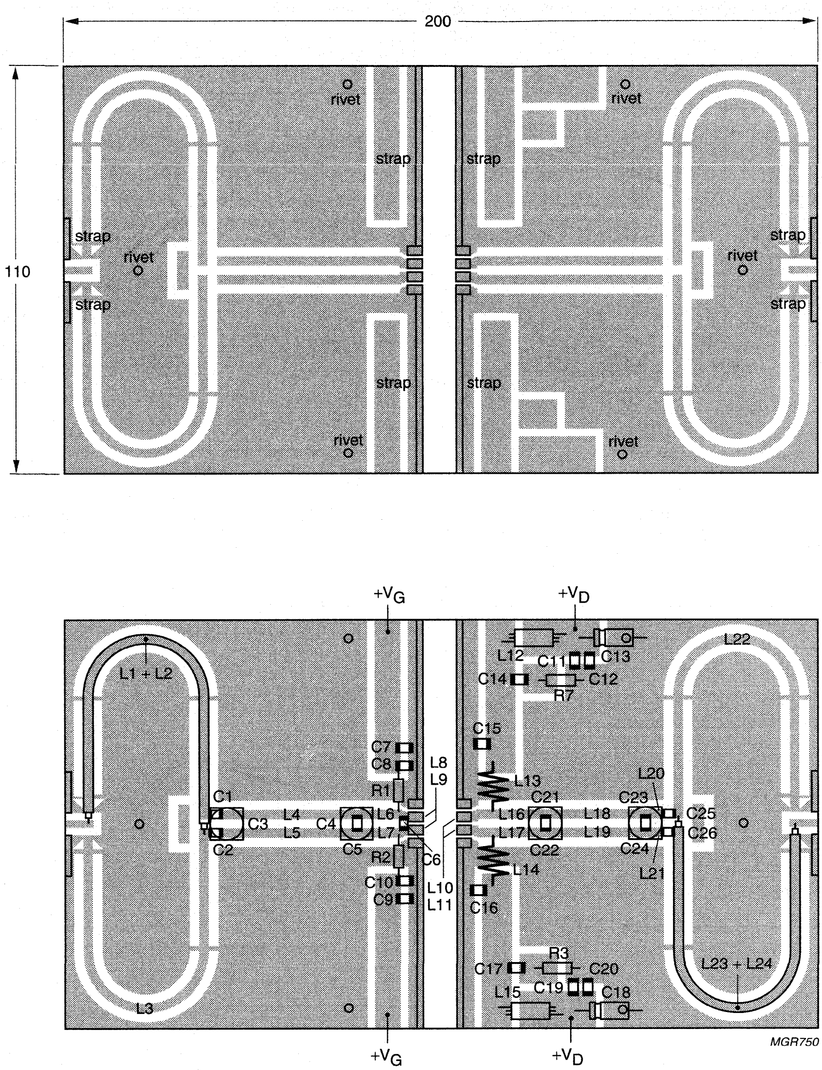
Fig.11 Test circuit for class-B operation.

List of components class-B test circuit (see Figs 11 and 12)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C25, C26	multilayer ceramic chip capacitor; note 1	91 pF		
C3	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4	multilayer ceramic chip capacitor; note 1	180 pF		
C5, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6	multilayer ceramic chip capacitor; note 1	100 pF		
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor; note 1	100 nF		2222 852 47104
C8, C10, C15, C16	multilayer ceramic chip capacitor; note 1	680 pF		
C11, C20	multilayer ceramic chip capacitor; note 1	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 μF, 63 V		
C21	multilayer ceramic chip capacitor; note 1	82 pF		
C23	multilayer ceramic chip capacitor; note 1	33 pF		
L1, L3, L22, L24	stripline; note 2	55 Ω	111 × 2.5 mm	
L2, L23	semi-rigid cable	50 Ω	length 111 mm ext. dia 2.2 mm	
L4, L5	stripline; note 2	50 Ω	6.5 × 2.8 mm	
L6, L7	stripline; note 2	50 Ω	35 × 2.8 mm	
L8, L9	stripline; note 2	50 Ω	5 × 2.8 mm	
L10, L11	stripline; note 2	50 Ω	9 × 2.8 mm	
L12, L15	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L13, L14	4 turns enamelled 1 mm copper wire	50 nH	length 6.5 mm int. dia. 4 mm leads 2 × 5 mm	
L16, L17	stripline; note 2	50 Ω	17 × 2.8 mm	
L18, L19	stripline; note 2	50 Ω	26 × 2.8 mm	
L20, L21	stripline; note 2	50 Ω	4 × 2.8 mm	
R1, R2, R7, R8	metal film resistor	0.4 W, 10 Ω		
R3, R4	10 turns potentiometer	50 kΩ		
R5, R6	metal film resistor	0.4 W, 205 kΩ		

Notes

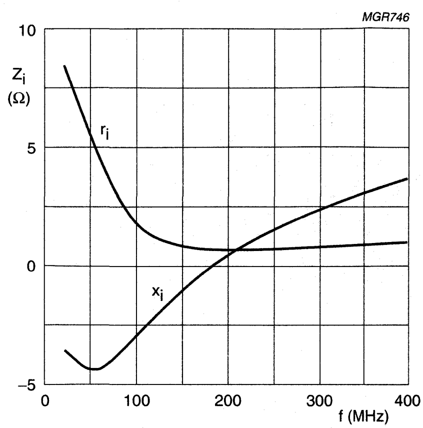
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed-circuit board with epoxy glass dielectric ($\varepsilon_r = 4.5$); thickness $^1/_{16}$ inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.



Dimensions in mm.

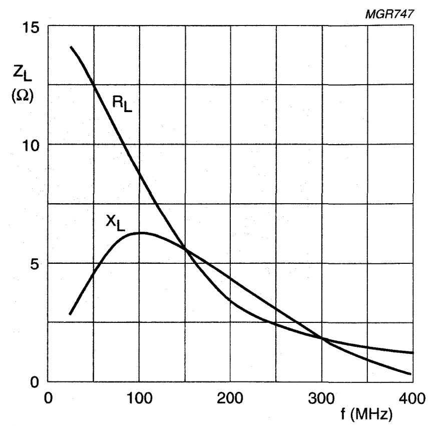
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.13 Input impedance as a function of frequency (series components); typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.14 Load impedance as a function of frequency (series components); typical values per section.

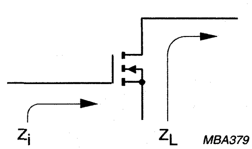
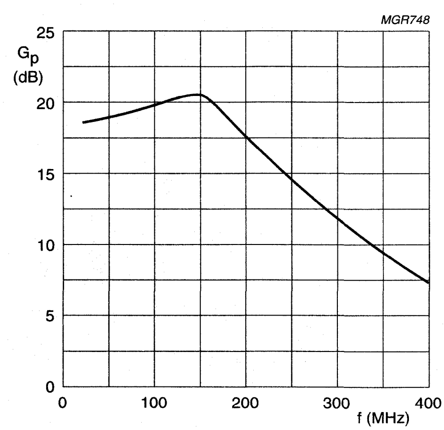


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.16 Power gain as a function of frequency; typical values per section.

VHF push-pull power MOS transistor — BLF248

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262 A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262 A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

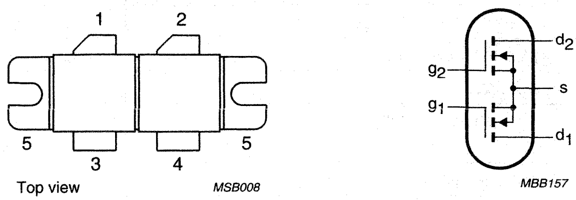


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_P (dB)	η_D (%)
class-AB	225	28	300	> 10	> 55
	175	28	300	typ. 13	typ. 67

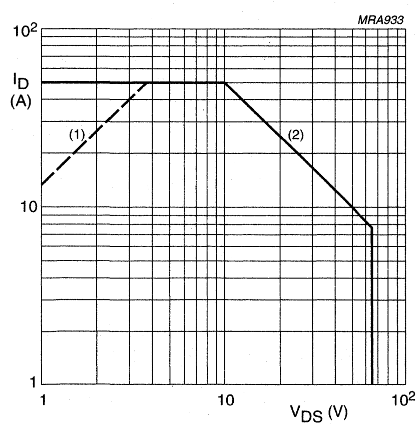
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C

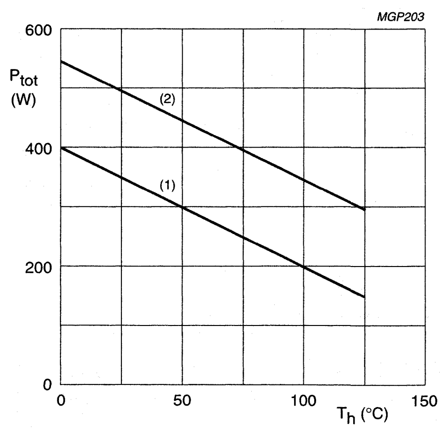
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	0.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



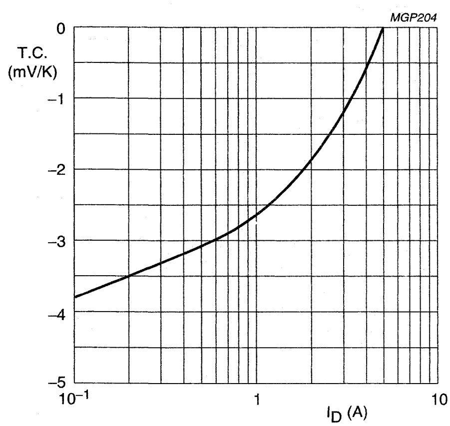
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (PER SECTION)

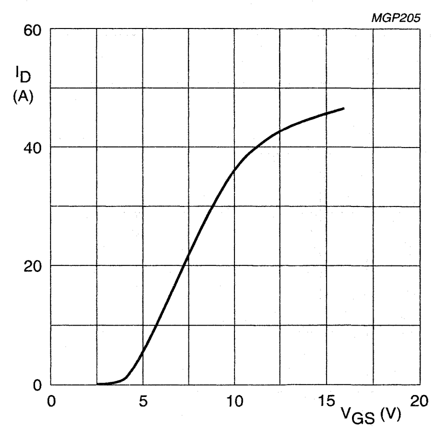
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 100 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 100 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	I_D = 100 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	I_D = 8 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	500	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	360	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	46	–	pF



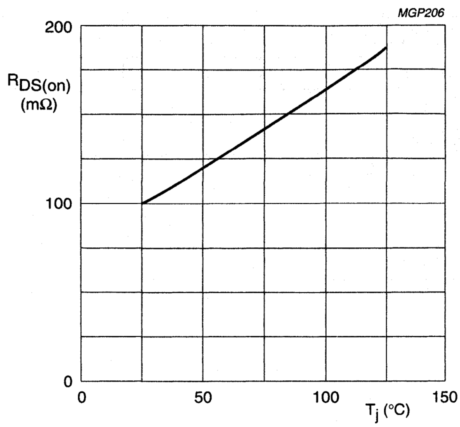
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



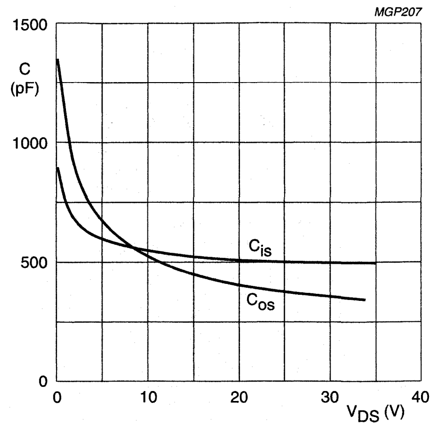
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



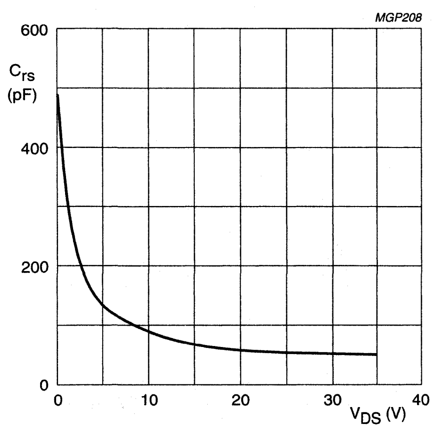
I_D = 8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

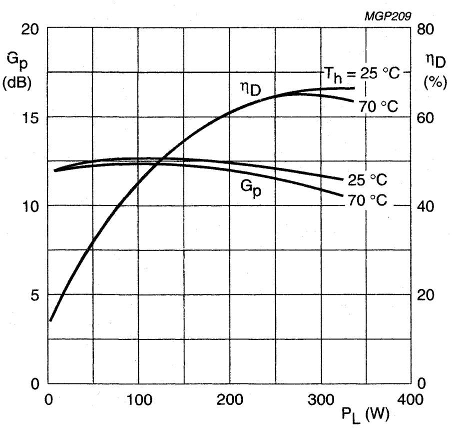
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W, unless otherwise specified.
RF performance in a linear amplifier in a common source class-AB circuit.
R_{GS} = 536 Ω per section; optimum load impedance per section = 0.79 − j0.11 Ω.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_P (dB)	η_D (%)
class-AB	225	28	300	> 10 typ. 11.5	> 55 typ. 65
	175	28	300	typ. 13	typ. 67

Ruggedness in class-AB operation

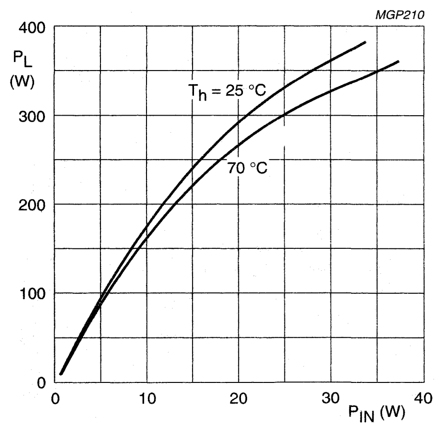
The BLF248 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 225 MHz at rated output power.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 2 × 250 mA; R_{GS} = 536 Ω (per section); Z_L = 0.79 − j0.11 Ω (per section); f = 225 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 2 × 250 mA; R_{GS} = 536 Ω (per section); Z_L = 0.79 − j0.11 Ω (per section); f = 225 MHz.

Fig.10 Load power as a function of input power, typical values.

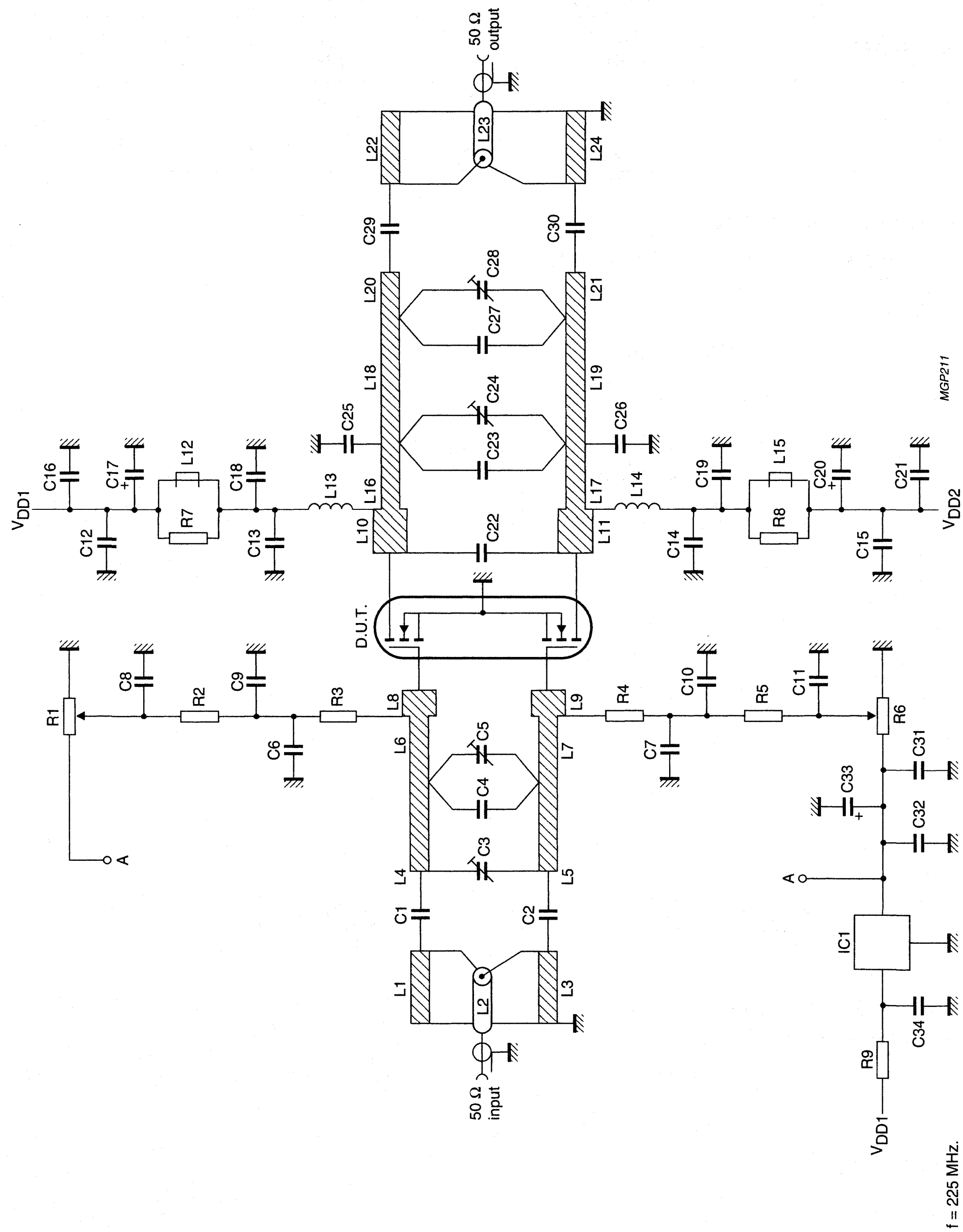


Fig.11 Test circuit for class-AB operation.

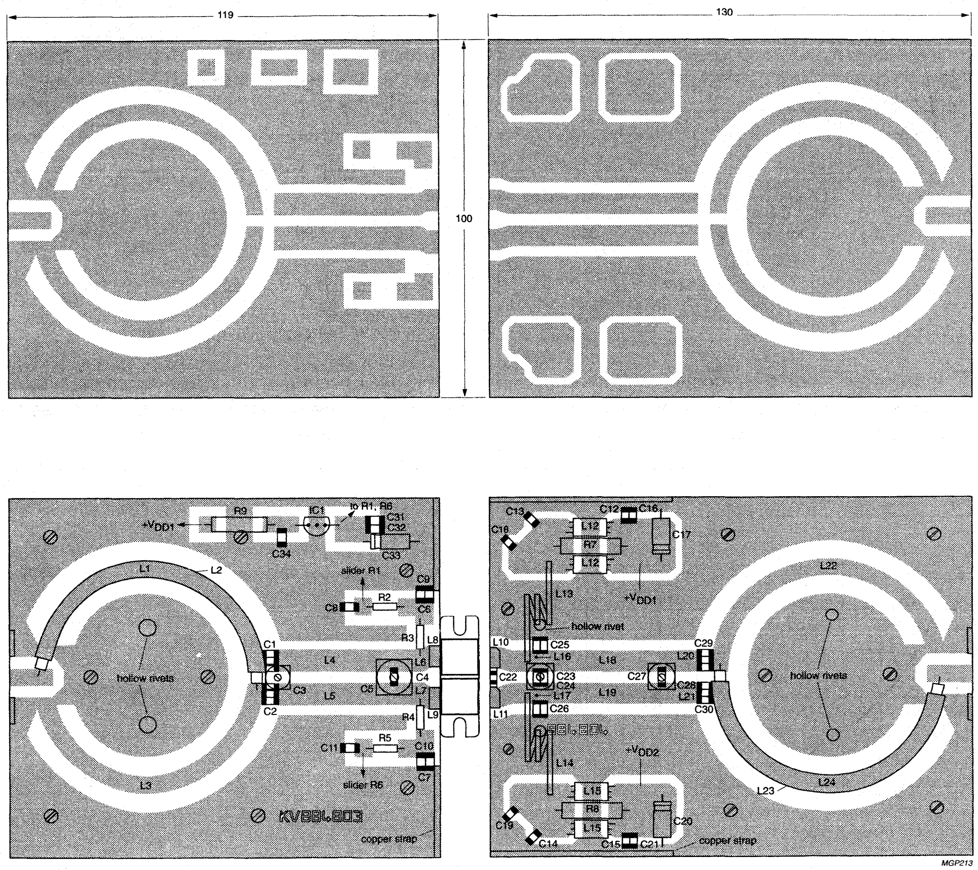
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	2 × 56 pF + 18 pF in parallel, 500 V		
C3	film dielectric trimmer	2 to 9 pF		2222 809 09005
C4	multilayer ceramic chip capacitor (note 1)	47 pF, 500 V		
C5	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6, C7, C9, C10, C12, C15, C31, C34	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C8, C11, C16, C21, C32	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C13, C14, C18, C19	multilayer ceramic chip capacitor (note 1)	510 pF, 500 V		
C17, C20, C33	electrolytic capacitor	10 μF, 63 V		
C22	multilayer ceramic chip capacitor (note 1)	82 pF, 500 V		
C23	multilayer ceramic chip capacitor (note 1)	10 pF + 30 pF in parallel, 500 V		
C24, C28	film dielectric trimmer	2 to 18 pF		2222 809 09006
C25, C26	multilayer ceramic chip capacitor (note 1)	39 pF + 47 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C29, C30	multilayer ceramic chip capacitor (note 1)	3 × 100 pF in parallel, 500 V		
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8 × 80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. dia. 3.6 mm ext. conductor length 80 mm	
L4, L5	stripline (note 2)	43 Ω	6 × 32.5 mm	
L6, L7, L10, L11	stripline (note 2)	43 Ω	6 × 10.5 mm	
L8, L9	stripline (note 2)	43 Ω	6 × 3 mm	
L12, L15	grade 3B Ferroxcube wide-band HF choke	2 in parallel		4312 020 36642
L13, L14	2 turns enamelled 1.6 mm copper wire	25 nH	int. dia. 5 mm leads 2 × 7 mm space 2.5 mm	
L16, L17	stripline (notes 2 and 4)	43 Ω	6 × 3 mm	
L18, L19	stripline (notes 2 and 4)	43 Ω	6 × 35 mm	
L20, L21	stripline (notes 2 and 4)	43 Ω	6 × 9 mm	
R1, R6	10 turns potentiometer	50 kΩ		
R2, R5	0.4 W metal film resistor	1 kΩ		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
R3, R4	0.4 W metal film resistor	536 Ω		
R7, R8	1 W metal film resistor	10 Ω ±5%		
R9	1 W metal film resistor	3.16 kΩ		
IC1	78L05 voltage regulator			

Notes

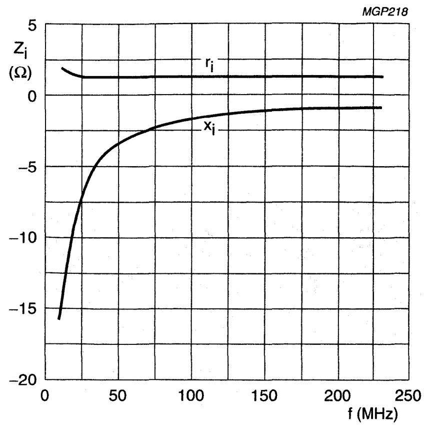
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. L1, L3 - L11, L16 - L22 and L24 are micro-striplines on a double copper-clad printed circuit board, with glass microfibre PTFE dielectric ($\varepsilon_r = 2.2$), thickness $1/16$ inch, thickness of copper sheet 2×35 µm.
3. L2 and L23 are soldered on striplines L1 and L24 respectively.
4. A copper strap, thickness 0.8 mm, is soldered on striplines L16 - L21.



The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

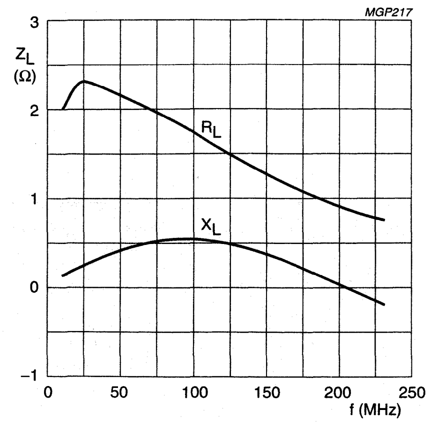
Dimensions in mm.

Fig.12 Component layout for 225 MHz class-AB test circuit.



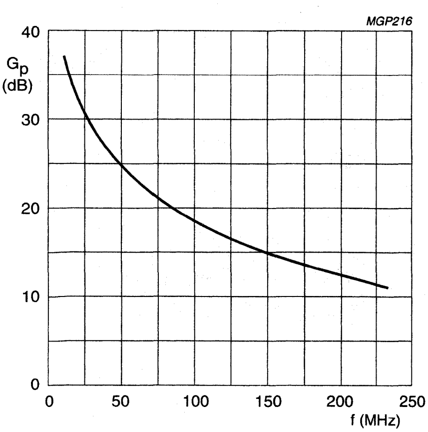
Class-AB operation; V_{DS} = 28 V; I_D = 2 × 250 mA;
R_{GS} = 536 Ω (per section);
P_L = 300 W (total device); T_h = 25 °C.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 28 V; I_D = 2 × 250 mA;
R_{GS} = 536 Ω (per section);
P_L = 300 W (total device); T_h = 25 °C.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 28 V; I_D = 2 × 250 mA;
R_{GS} = 536 Ω (per section);
P_L = 300 W (total device); T_h = 25 °C.

Fig.15 Power gain as a function of frequency, typical values per section.

VHF power MOS transistor | BLF277

FEATURES

- High power gain
- Easy power control
- Gold metallization ensures excellent reliability
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 6-lead, SOT119 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT119

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

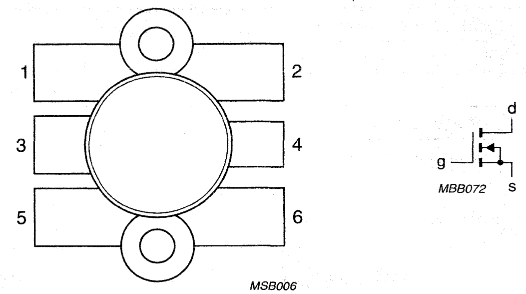


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	50	150	> 14	> 50

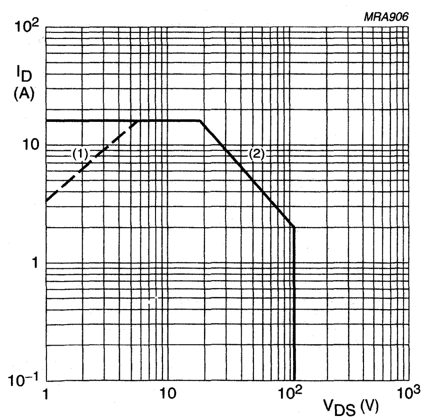
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	16	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

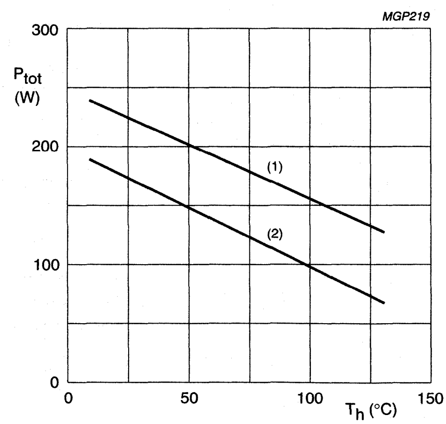
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 220 W	0.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 220 W	0.2 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



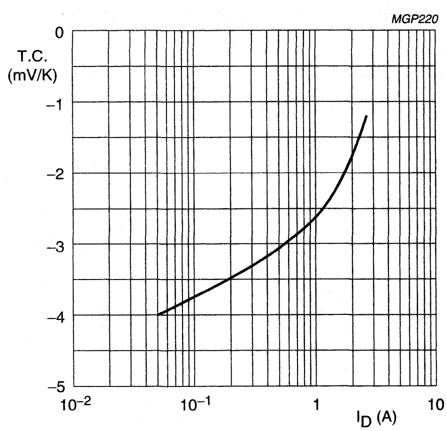
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

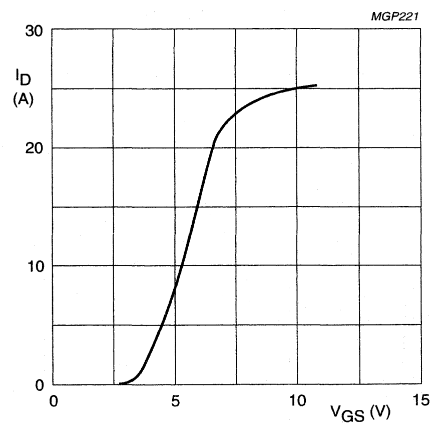
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF



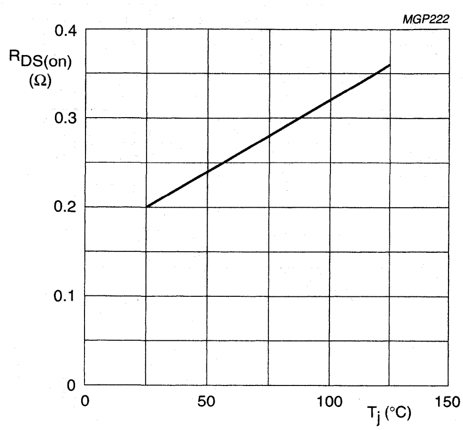
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



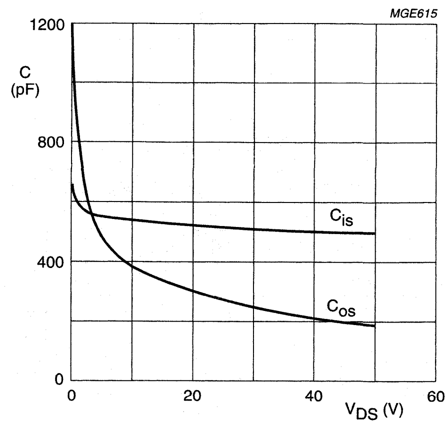
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



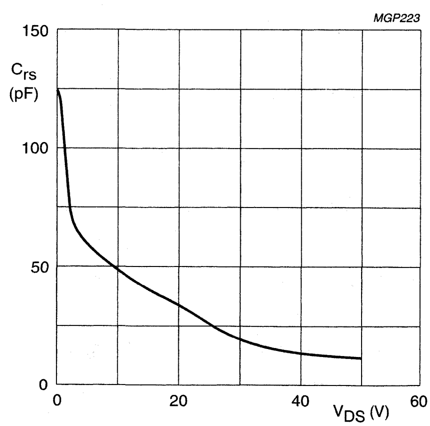
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

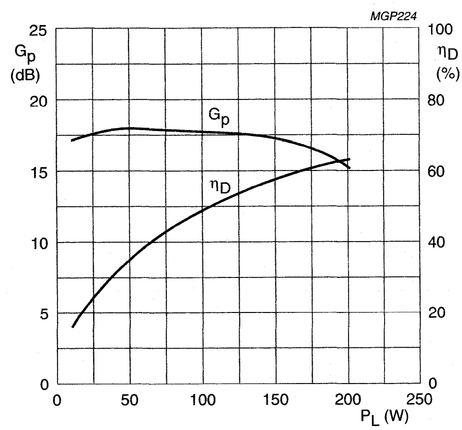
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; R_{GS} = 16 Ω; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	50	0.1	150	> 14 typ. 17	> 50 typ. 58

Ruggedness in class-B operation

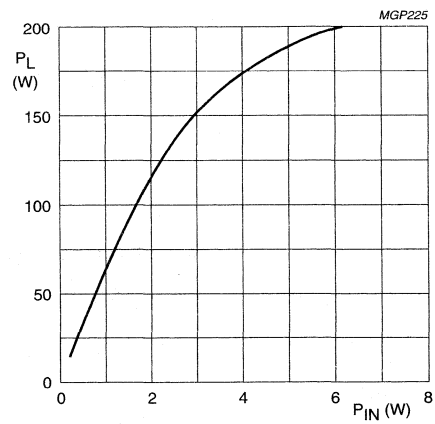
The BLF277 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 50 V; f = 175 MHz at rated load power.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
Z_L = 1.4 + j1.6 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
Z_L = 1.4 + j1.6 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.

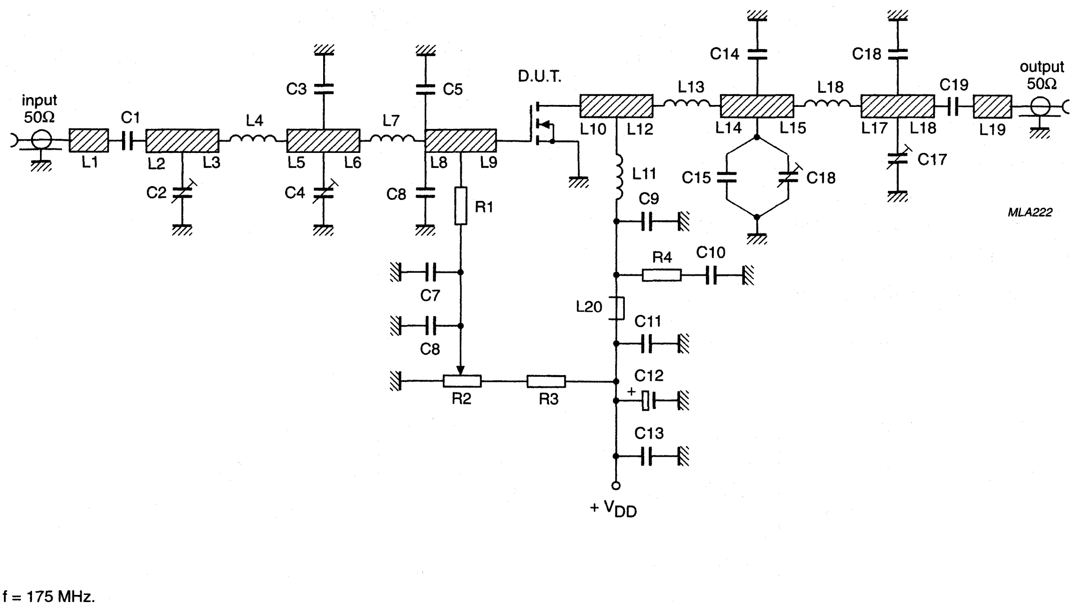


Fig.11 Test circuit for class-B operation.

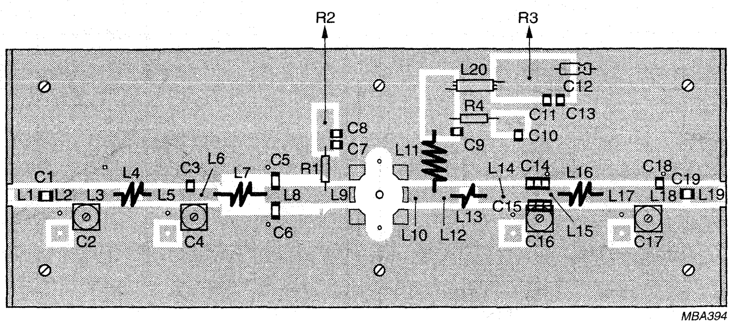
List of components (class-B test circuit)

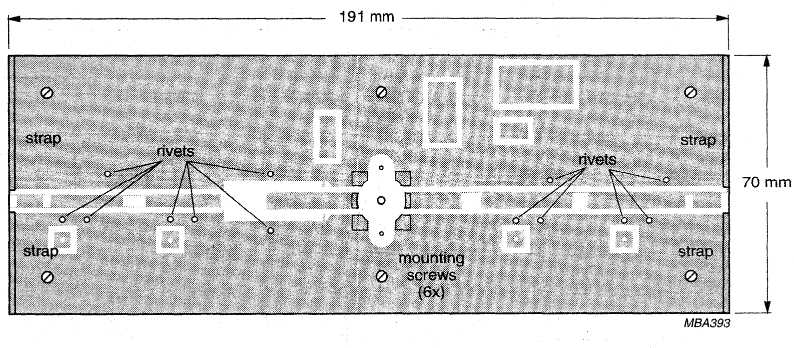
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C19	multilayer ceramic chip capacitor (note 1)	680 pF		
C2, C4, C17	film dielectric trimmer	5 to 60 pF		2222 809 08003
C3	multilayer ceramic chip capacitor (note 1)	33 pF		
C5, C6, C9	multilayer ceramic chip capacitor (note 1)	100 pF		
C7, C10, C13	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C12	electrolytic capacitor	10 µF, 63 V		
C14, C15	multilayer ceramic chip capacitor (note 2)	3 × 22 pF in parallel		
C16	film dielectric trimmer	4 to 40 pF		2222 809 08002
C18	multilayer ceramic chip capacitor (note 1)	18 pF		
L1	stripline (note 3)	49 Ω	length 8 mm width 4 mm	
L2	stripline (note 3)	49 Ω	length 12 mm width 4 mm	
L3	stripline (note 3)	49 Ω	length 7.5 mm width 4 mm	
L4	2 turns enamelled 1.5 mm copper wire	25 nH	length 3.7 mm int. dia. 5 mm leads 2 × 1 mm	
L5	stripline (note 3)	49 Ω	length 15.5 mm width 4 mm	
L6	stripline (note 3)	49 Ω	length 5 mm width 4 mm	
L7	2 turns enamelled 1.5 mm copper wire	25 nH	length 4.2 mm int. dia. 5 mm leads 2 × 4 mm	
L8	stripline (note 3)	31 Ω	length 18 mm width 6 mm	
L9	stripline (note 3)	31 Ω	length 6 mm width 6 mm	
L10, L12	stripline (note 3)	31 Ω	length 7 mm width 6 mm	
L11	3 turns enamelled 1.5 mm copper wire	40 nH	length 6.8 mm int. dia. 5 mm leads 2 × 3 mm	
L13	1 turn enamelled 1.5 mm copper wire	3 nH	int. dia. 2.8 mm leads 2 × 1 mm	
L14	stripline (note 3)	36 Ω	length 15.5 mm width 5 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L15	stripline (note 3)	36 Ω	length 8 mm width 5 mm	
L16	2 turns enamelled 2.5 mm copper wire	28 nH	length 5.5 mm int. dia. 5 mm leads 2 × 3 mm	
L17	stripline (note 3)	36 Ω	length 12 mm width 5 mm	
L18, L19	stripline (note 3)	36 Ω	length 8.5 mm width 5 mm	
L20	grade 3B Ferroxcube RF choke			4312 020 36642
R1	0.4 W metal film resistor	16 Ω		
R2	10 turn potentiometer	50 kΩ		
R3	0.4 W metal film resistor	400 kΩ		
R4	0.4 W metal film resistor	100 kΩ		

Notes

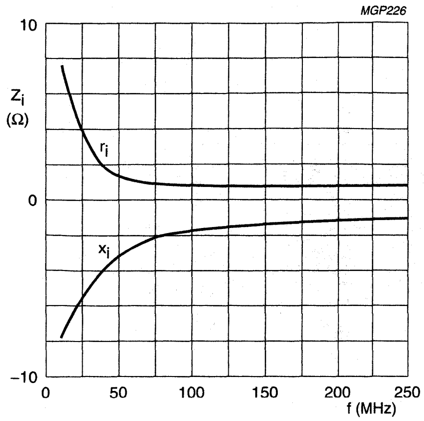
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. The striplines are mounted double copper-clad printed circuit board, with epoxy glass dielectric ($\varepsilon_r = 4.5$); thickness 1.6 mm.





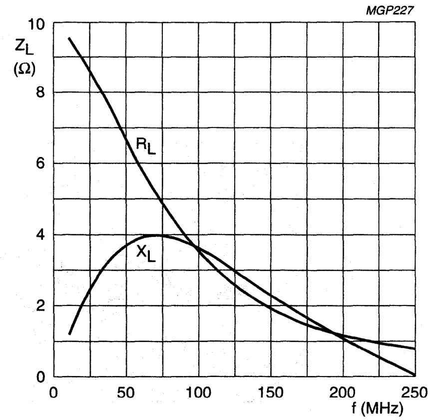
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
R_{GS} = 16 Ω; P_L = 150 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
R_{GS} = 16 Ω; P_L = 150 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

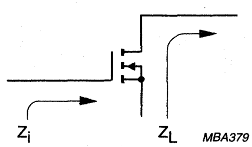
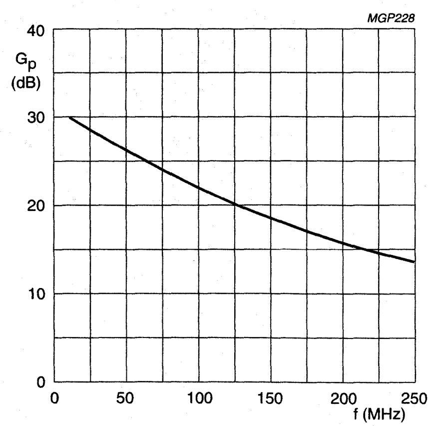


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
R_{GS} = 16 Ω; P_L = 150 W.

Fig.16 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor — BLF278

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Broadcast transmitters in the VHF frequency range.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT262A1 balanced flange package with two ceramic caps. The mounting flange provides the common source connection for the transistors.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT262A1

PIN	SYMBOL	DESCRIPTION
1	d_1	drain 1
2	d_2	drain 2
3	g_1	gate 1
4	g_2	gate 2
5	s	source

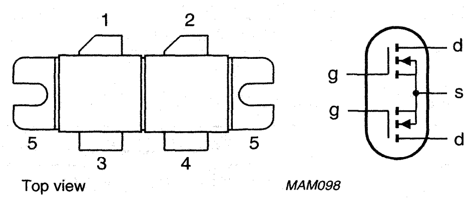


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	300	>20	>60
CW, class-C	108	50	300	typ. 18	typ. 80
CW, class-AB	225	50	250	>14 typ. 16	>50 typ. 55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

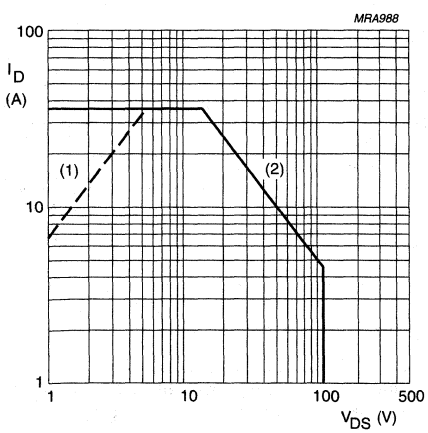
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section					
V_{DS}	drain-source voltage		–	110	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

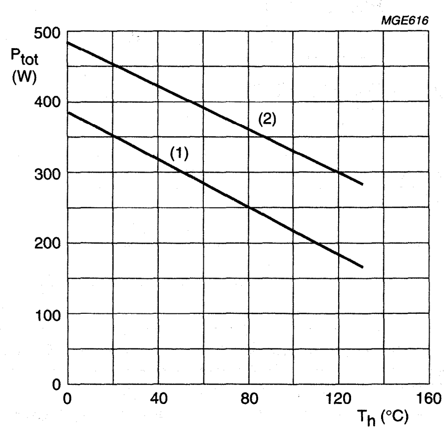
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	max. 0.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	max. 0.15	K/W



Total device; both sections equally loaded.
(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



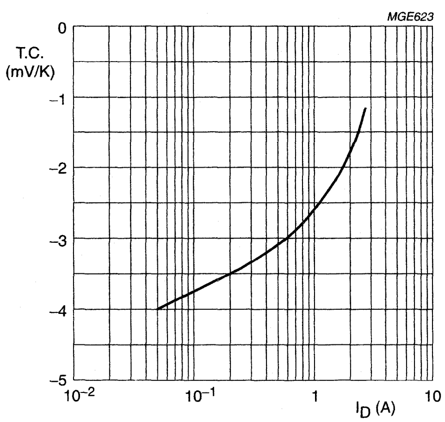
Total device; both sections equally loaded.
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

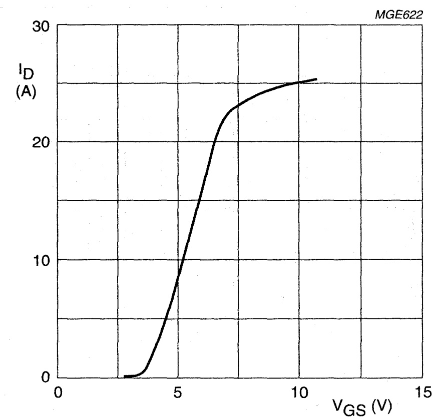
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 50 mA	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both sections	V_{DS} = 10 V; I_D = 50 mA	–	–	100	mV
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both sections	V_{DS} = 10 V; I_D = 5 A	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0.2	0.3	Ω
I_{DSX}	drain cut-off current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF
$C_{d\text{-}f}$	drain-flange capacitance		–	5.4	–	pF



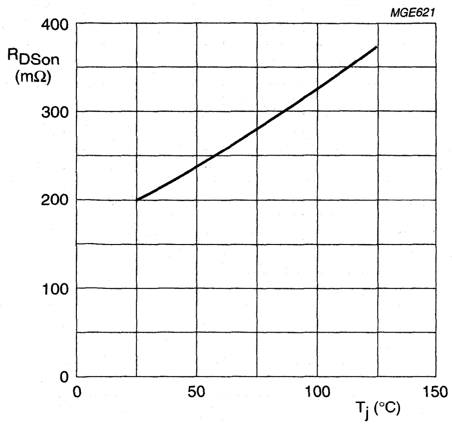
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



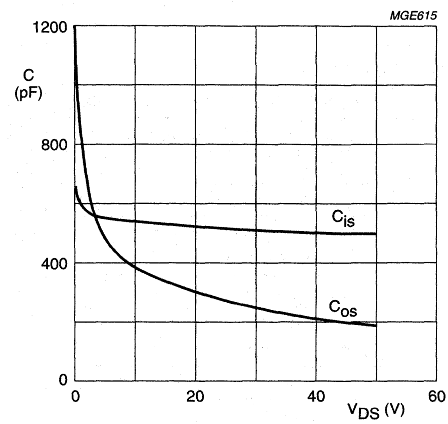
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



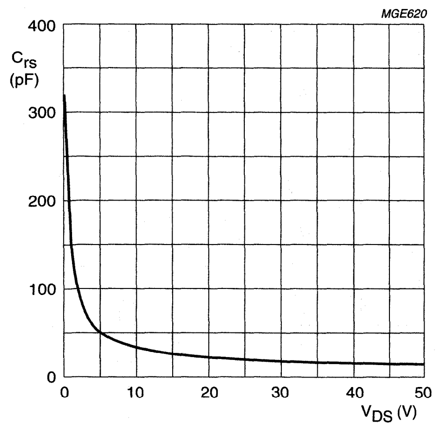
V_{GS} = 10 V; I_D = 5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION

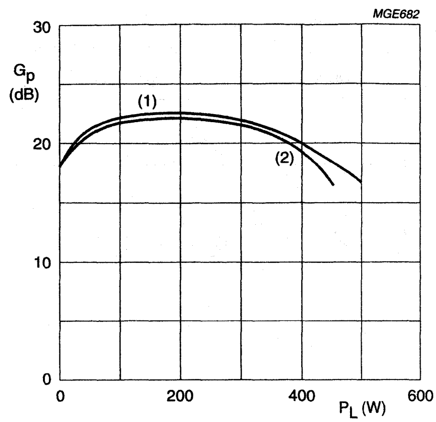
Class-B operation

RF performance in CW operation in a common source push-pull test circuit. $T_h = 25$ °C; $R_{th\ mb\text{-}h} = 0.15$ K/W unless otherwise specified. $R_{GS} = 4\ \Omega$ per section; optimum load impedance per section = 3.2 + j4.3 Ω ($V_{DS} = 50$ V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	2 × 0.1	300	>20 typ. 22	>60 typ. 70
CW, class-C	108	50	$V_{GS} = 0$	300	typ. 18	typ. 80

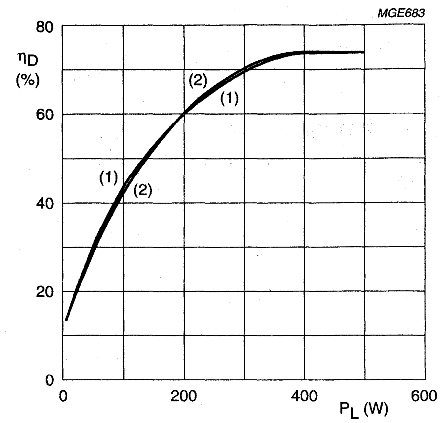
Ruggedness in class-B operation

The BLF278 is capable of withstanding a load mismatch corresponding to VSWR = 7 : 1 through all phases under the conditions: $V_{DS} = 50$ V; f = 108 MHz at rated load power.



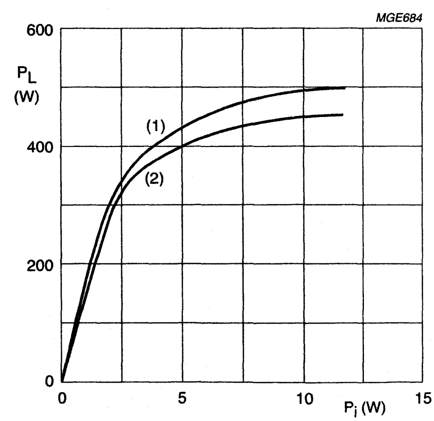
Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A; f = 108 MHz;
Z_L = 3.2 + j4.3 Ω (per section); R_{GS} = 4 Ω (per section).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A; f = 108 MHz;
Z_L = 3.2 + j4.3 Ω (per section); R_{GS} = 4 Ω (per section).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.10 Efficiency as a function of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A; f = 108 MHz;
Z_L = 3.2 + j4.3 Ω (per section); R_{GS} = 4 Ω (per section).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.11 Load power as a function of input power, typical values.

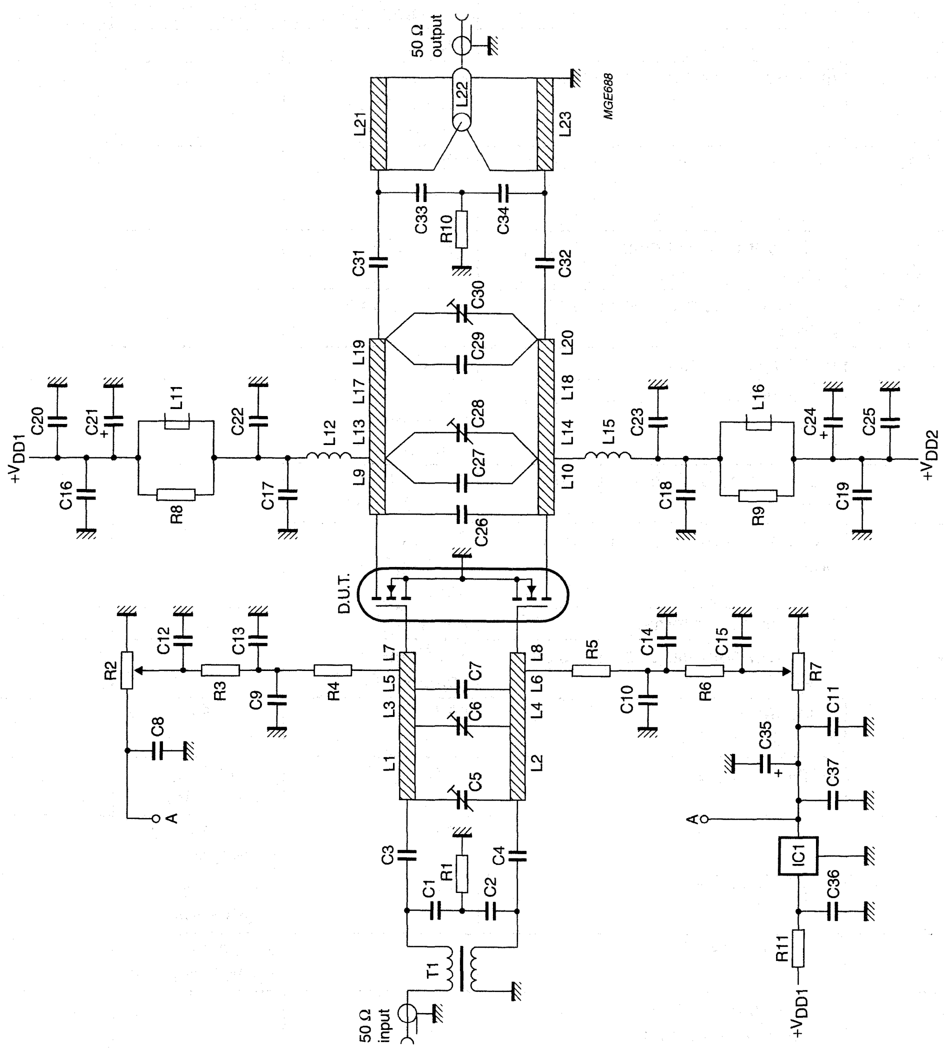


Fig.12 Class-B test circuit at f = 108 MHz.

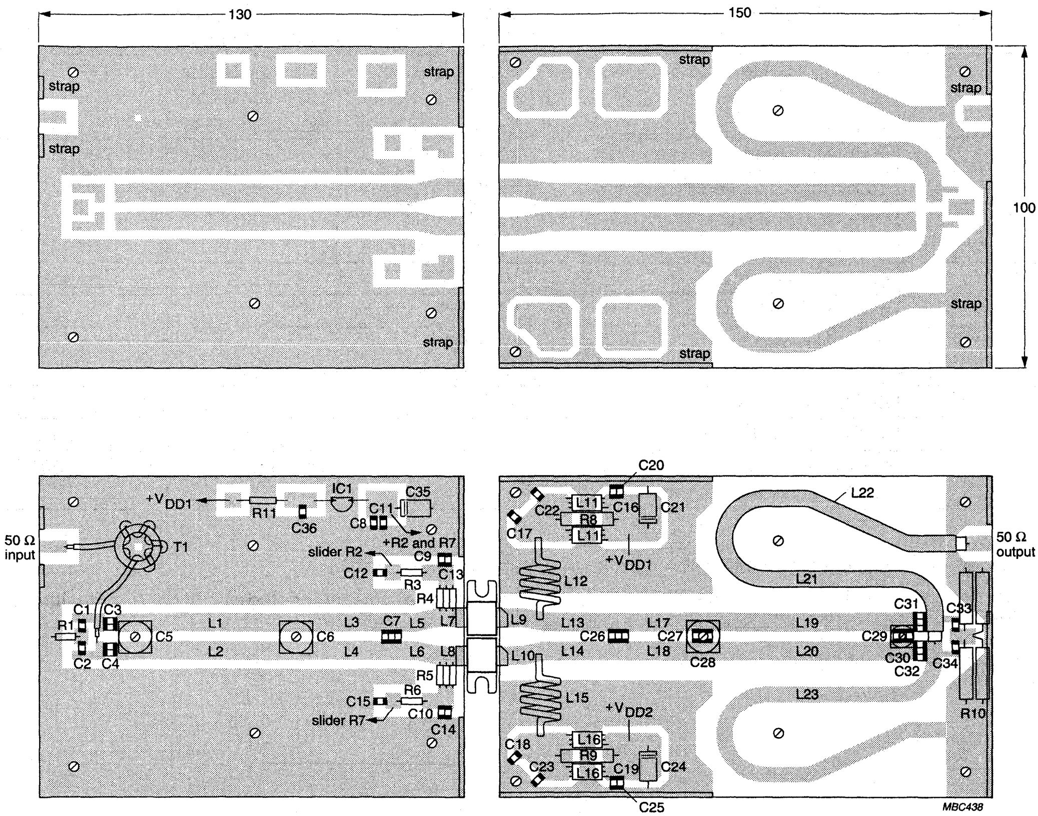
List of components (see Figs 12 and 13).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C33, C34	multilayer ceramic chip capacitor; note 1	22 pF, 500 V		
C3, C4	multilayer ceramic chip capacitor; note 1	100 pF + 68 pF in parallel, 500 V		
C5, C6, C28	film dielectric trimmer	5 to 60 pF		2222 809 08003
C7	multilayer ceramic chip capacitor; note 1	2 × 100 pF + 1 × 120 pF in parallel, 500 V		
C8, C11, C12, C15, C16, C19, C36	multilayer ceramic chip capacitor	100 nF, 500 V		2222 852 47104
C9, C10, C13, C14, C20, C25	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C17, C18, C22, C23	multilayer ceramic chip capacitor; note 1	470 pF, 500 V		
C21, C24, C35	electrolytic capacitor	10 μF, 63 V		
C26	multilayer ceramic chip capacitor; note 1	2 × 15 pF + 1 × 18 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor; note 1	3 × 15 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 18 pF + 1 × 15 pF in parallel, 500 V		
C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C31, C32	multilayer ceramic chip capacitor; note 1	3 × 43 pF in parallel, 500 V		
L1, L2	stripline; note 2	43 Ω	length 57.5 mm width 6 mm	
L3, L4	stripline; note 2	43 Ω	length 29.5 mm width 6 mm	
L5, L6	stripline; note 2	43 Ω	length 14 mm width 6 mm	
L7, L8	stripline; note 2	43 Ω	length 6 mm width 6 mm	
L9, L10	stripline; note 2	43 Ω	length 17.5 mm width 6 mm	
L11, L16	2 × grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L12, L15	4 turns enamelled 2 mm copper wire	85 nH	length 13.5 mm int. dia. 10 mm leads 2 × 7 mm	
L13, L14	stripline; note 2	43 Ω	length 19.5 mm width 6 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L17, L18	stripline; note 2	43 Ω	length 24.5 mm width 6 mm	
L19, L20	stripline; note 2	43 Ω	length 66 mm width 6 mm	
L21, L23	stripline; note 2	50 Ω	length 160 mm width 4.8 mm	
L22	semi-rigid cable; note 3	50 Ω	ext. dia. 3.6 mm outer conductor length 160 mm	
R1	metal film resistor	10 Ω, 0.4 W		
R2, R7	10 turn potentiometer	50 kΩ		
R3, R6	metal film resistor	3 × 12.1 Ω in parallel, 0.4 W		
R4, R5	metal film resistor	10 Ω; 0.4 W		
R8, R9	metal film resistor	10 Ω ±5%, 1 W		
R10	metal film resistor	4 × 10 Ω in parallel, 1 W		
R11	metal film resistor	5.11 kΩ, 1 W		
IC1	voltage regulator 78L05			
T1	1:1 Balun; 7 turns type 4C6 50 Ω coaxial cable wound around toroid		14 × 9 × 5 mm	4322 020 90770

Notes

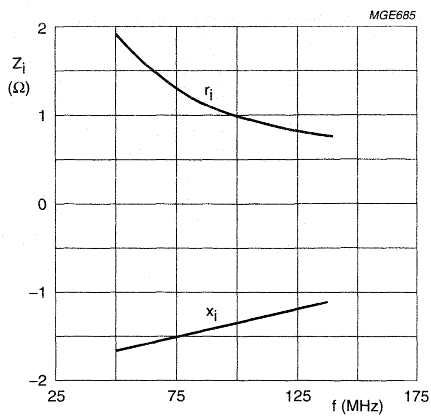
1. American Technical Ceramics capacitor, type 100B or capacitor of same quality.
2. L1 to L10, L13, L14, L17 to L21 and L23 are striplines on a double copper-clad printed-circuit board, with fibre-glass PTFE dielectric ($\varepsilon_r = 2.2$), thickness $^1/_{16}$ inch; thickness of copper sheet 2 × 35 μm.
3. L22 is soldered on to stripline L21.



Dimensions in mm.

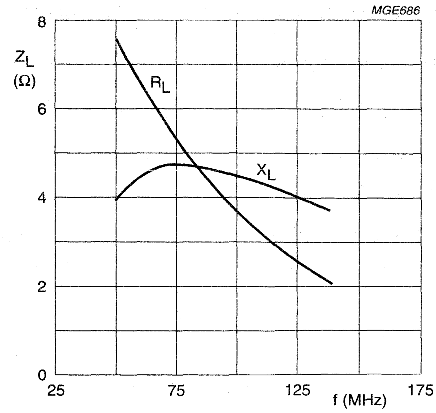
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.13 Printed-circuit board and component layout for 108 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A;
R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.14 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A;
R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.15 Load impedance as a function of frequency (series components), typical values per section.

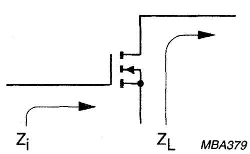
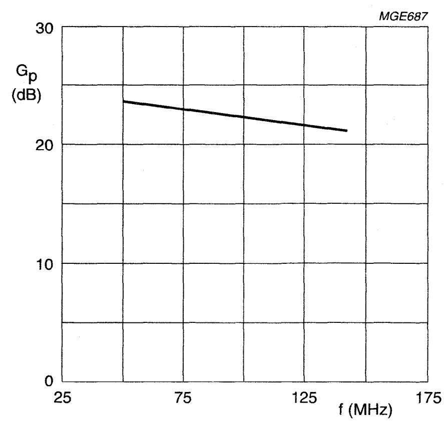


Fig.16 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A;
R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.17 Power gain as a function of frequency, typical values per section.

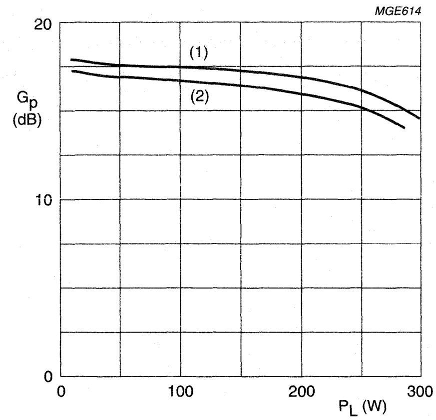
Class-AB operation

RF performance in CW operation in a common source push-pull test circuit. $T_h = 25\ °C$; $R_{th\ mb\text{-}h} = 0.15$ K/W unless otherwise specified. $R_{GS} = 2.8\ \Omega$ per section; optimum load impedance per section = 0.74 + j2 Ω; ($V_{DS} = 50$ V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	225	50	2 × 0.5	250	>14 typ. 16	>50 typ. 55

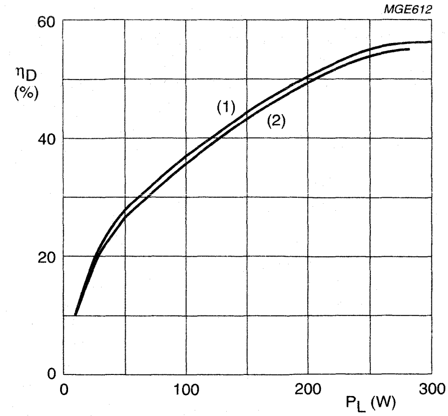
Ruggedness in class-AB operation

The BLF278 is capable of withstanding a load mismatch corresponding to VSWR = 7 : 1 through all phases under the conditions: $V_{DS} = 50$ V; f = 225 MHz at rated output power.



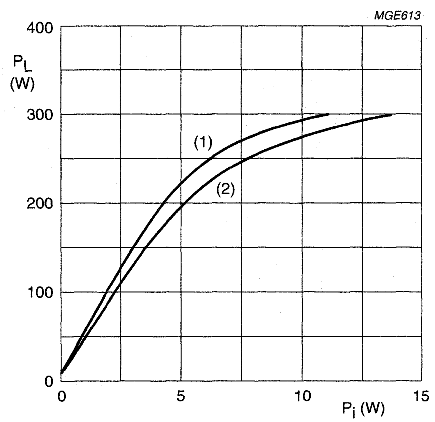
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.18 Power gain as a function of load power, typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.19 Efficiency as a function of load power, typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.20 Load power as a function of input power, typical values.

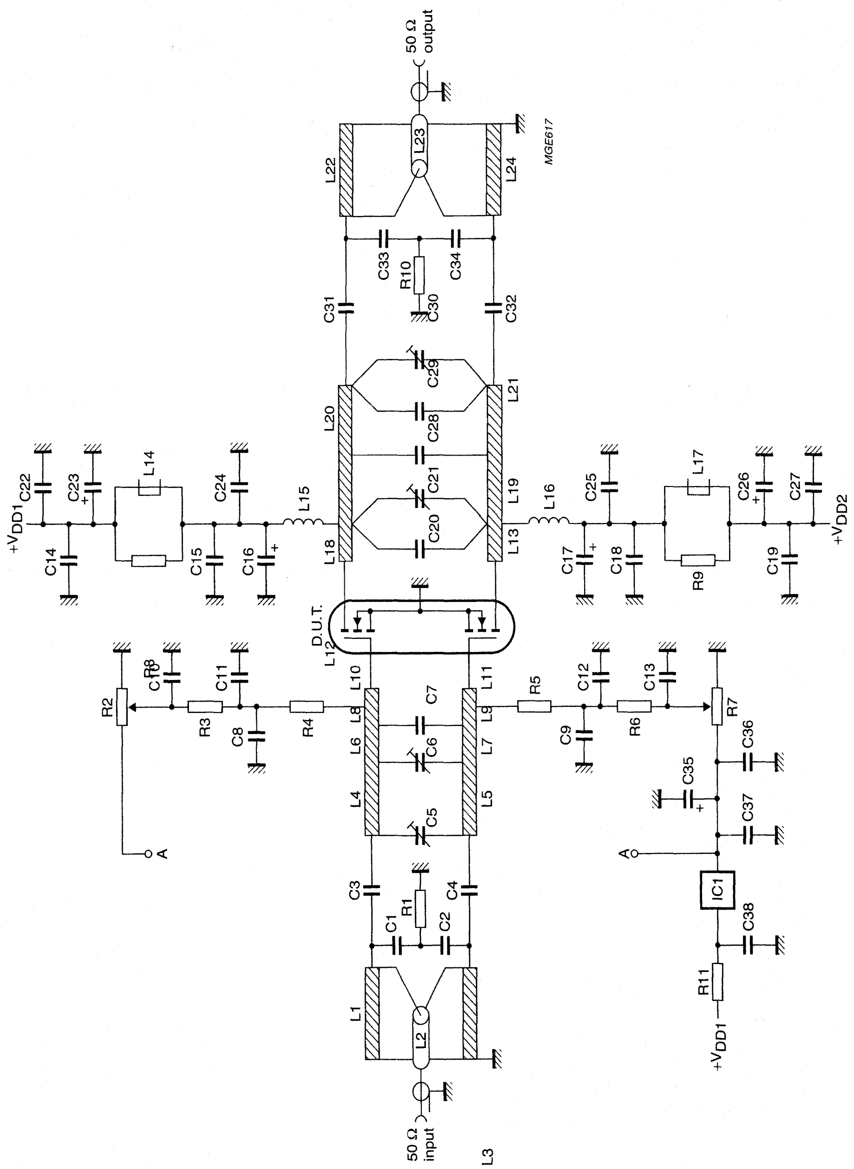


Fig.21 Class-AB test circuit at f = 225 MHz.

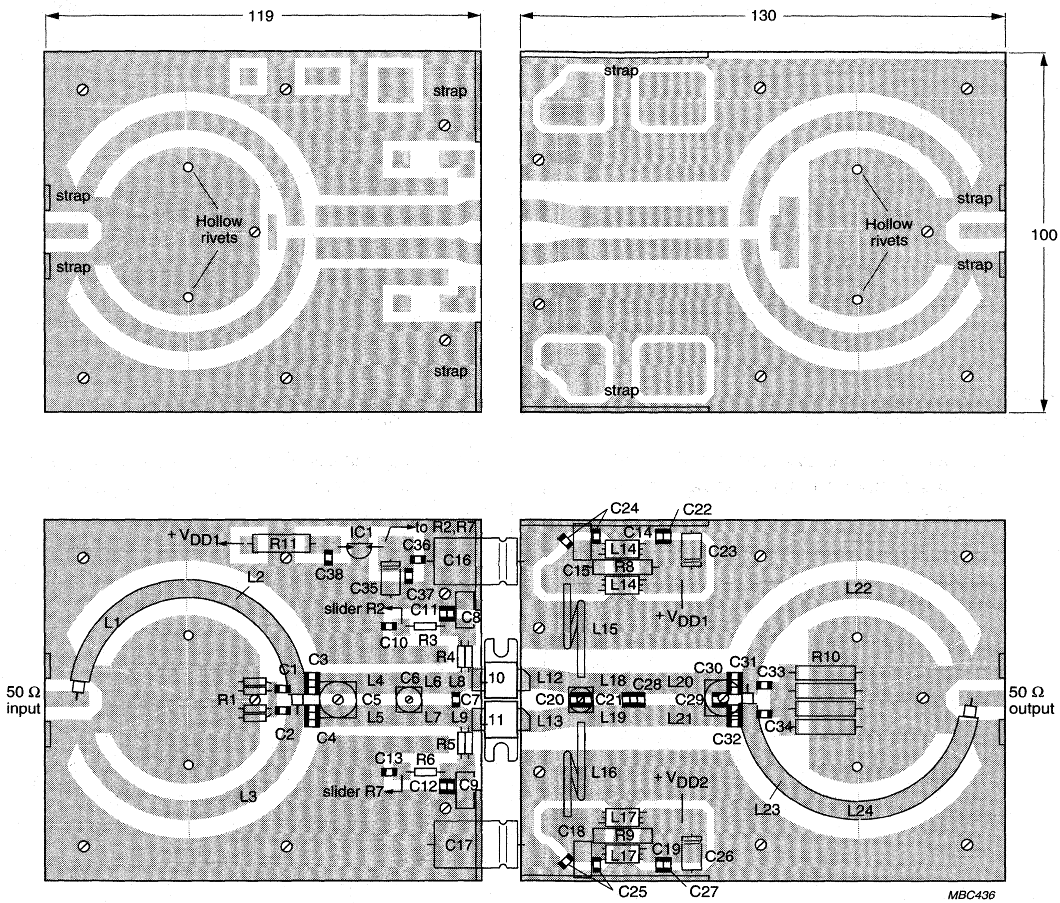
List of components (see Figs 21 and 22).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	27 pF, 500 V		
C3, C4, C31, C32	multilayer ceramic chip capacitor; note 1	3 × 18 pF in parallel, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7	multilayer ceramic chip capacitor; note 1	100 pF, 500 V		
C8, C9, C15, C18	MKT film capacitor	1 µF, 63 V		2222 371 11105
C10, C13, C14, C19, C36	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12	multilayer ceramic chip capacitor; note 1	2 × 1 nF in parallel, 500 V		
C16, C17	electrolytic capacitor	220 µF, 63 V		
C20	multilayer ceramic chip capacitor; note 1	3 × 33 pF in parallel, 500 V		
C21	film dielectric trimmer	2 to 9 pF		2222 809 09005
C22, C27, C37, C38	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C23, C26, C35	electrolytic capacitor	10 µF, 63 V		
C24, C25	multilayer ceramic chip capacitor; note 1	2 × 470 pF in parallel, 500 V		
C28	multilayer ceramic chip capacitor; note 1	2 × 10 pF + 1 × 18 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 5.6 pF in parallel, 500 V		
C33, C34	multilayer ceramic chip capacitor; note 1	5.6 pF, 500 V		
L1, L3, L22, L24	stripline; note 2	50 Ω	length 80 mm width 4.8 mm	
L2, L23	semi-rigid cable; note 3	50 Ω	ext. dia. 3.6 mm outer conductor length 80 mm	
L4, L5	stripline; note 2	43 Ω	length 24 mm width 6 mm	
L6, L7	stripline; note 2	43 Ω	length 14.5 mm width 6 mm	
L8, L9	stripline; note 2	43 Ω	length 4.4 mm width 6 mm	
L10, L11	stripline; note 2	43 Ω	length 3.2 mm width 6 mm	
L12, L13	stripline; note 2	43 Ω	length 15 mm width 6 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L14, L17	2 × grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L15, L16	1¾ turns enamelled 2 mm copper wire	40 nH	int. dia. 10 mm leads 2 × 7 mm space 1 mm	
L18, L19	stripline; note 2	43 Ω	length 13 mm width 6 mm	
L20, L21	stripline; note 2	43 Ω	length 29.5 mm width 6 mm	
R1	metal film resistor	10 Ω, 0.4 W		
R2, R7	10 turns potentiometer	50 kΩ		
R3, R6	metal film resistor	1 kΩ, 0.4 W		
R4, R5	metal film resistor	2 × 5.62 Ω, in parallel, 0.4 W		
R8, R9	metal film resistor	10 Ω ±5%, 1 W		
R10	metal film resistor	4 × 42.2 Ω in parallel, 1 W		
R11	metal film resistor	5.11 kΩ, 1 W		
IC1	voltage regulator 78L05			

Notes

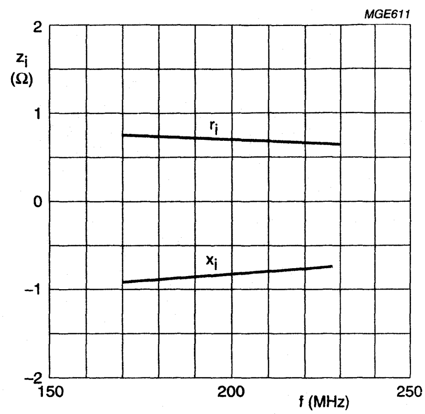
1. American Technical Ceramics capacitor, type 100B or other capacitor of the same quality.
2. L1, L3 to L13, L18 to L22 and L24 are microstriplines on a double copper-clad printed-circuit board, with fibre-glass reinforced PTFE dielectric ($\varepsilon_r = 2.2$), thickness $\frac{1}{16}$ inch; thickness of copper sheet 2 × 35 μm.
3. L2 and L23 are soldered on to striplines L1 and L24 respectively.



Dimensions in mm.

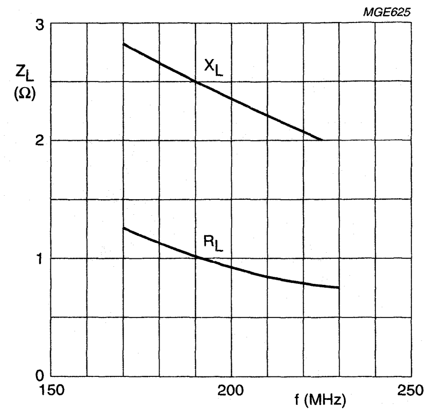
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.22 Printed-circuit board and component layout for 225 MHz class-AB test circuit.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.23 Input impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.24 Load impedance as a function of frequency (series components), typical values per section.

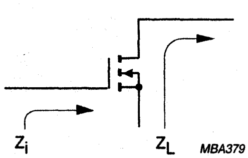
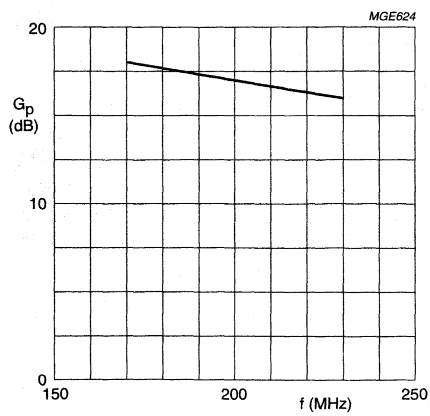


Fig.25 Definition of MOS impedance.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.26 Power gain as a function of frequency, typical values per section.

VHF power MOS transistor | BLF346

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Linear amplifier applications in Television transmitters and transposers.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 6-lead, SOT119 flange package, with a ceramic cap. All leads are isolated from the flange. A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the General Section of Data Handbook SC19a for further information.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING-SOT119

PIN	SYMBOL	DESCRIPTION
1	s	source
2	s	source
3	g	gate
4	d	drain
5	s	source
6	s	source

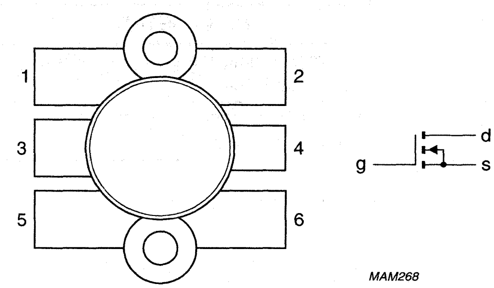


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance in a linear amplifier.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	P_L (W)	G_P (dB)	d_{im} (dB) (1)
Class-A	224.25	28	3	70	>24	>14	−52
				25	typ. 30	typ. 16.5	−52

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

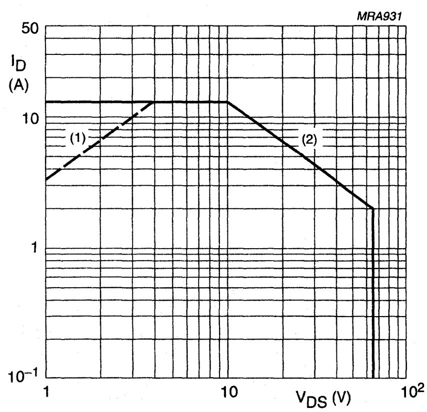
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
V_{GSS}	gate-source voltage		–	±20	V
I_D	DC drain current		–	13	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	130	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

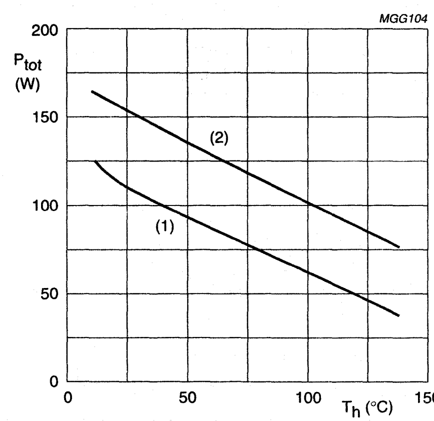
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 130 W	1.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 130 W	0.2	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

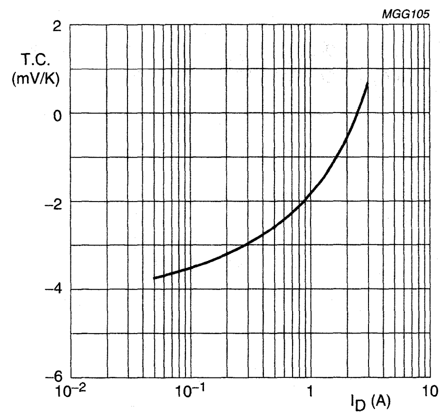
Fig.3 Power derating curves.

VHF power MOS transistor BLF346

CHARACTERISTICS

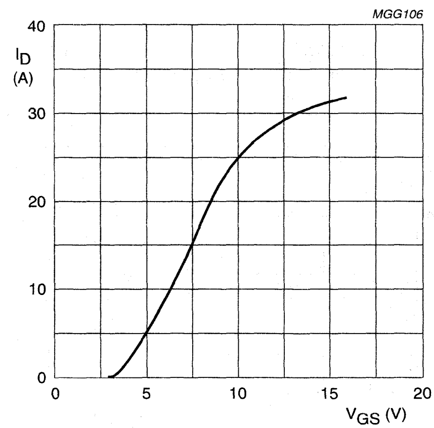
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 50 mA	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	V_{DS} = 10 V; I_D = 50 mA	–	–	100	mV
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	3	4.2	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	22	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	225	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	180	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF



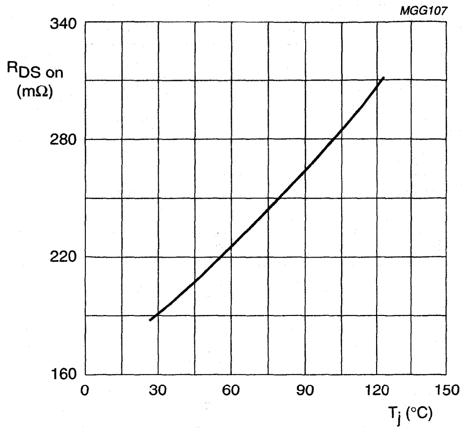
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



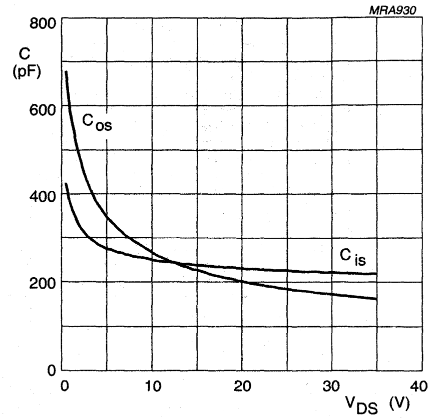
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values.



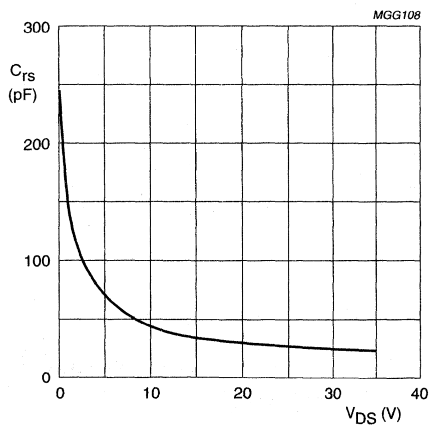
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

APPLICATION INFORMATION

RF performance in a linear amplifier (common source class-A circuit).
$R_{th\ mb-h}$ = 0.2 K/W; Z_L = 1.1 + j0.2 Ω unless otherwise specified.

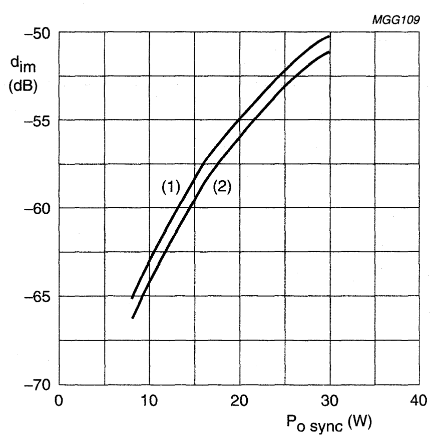
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	$P_{o\ sync}$ (W)	G_P (dB)	d_{im} (dB) (1)
Class-A	224.25	28	3	70	> 24	> 14	−52
				25	typ. 30	typ. 16.5	−52
				70	typ. 20	typ. 14.5	−55
				25	typ. 22	typ. 15	−55

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

Ruggedness in class-A operation

The BLF346 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 225 MHz at rated output power.



(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.9 Intermodulation distortion as a function of peak synchronized output power.

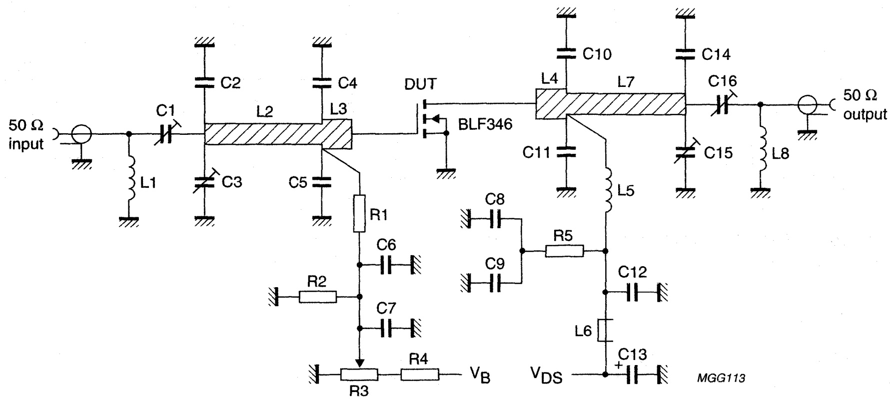


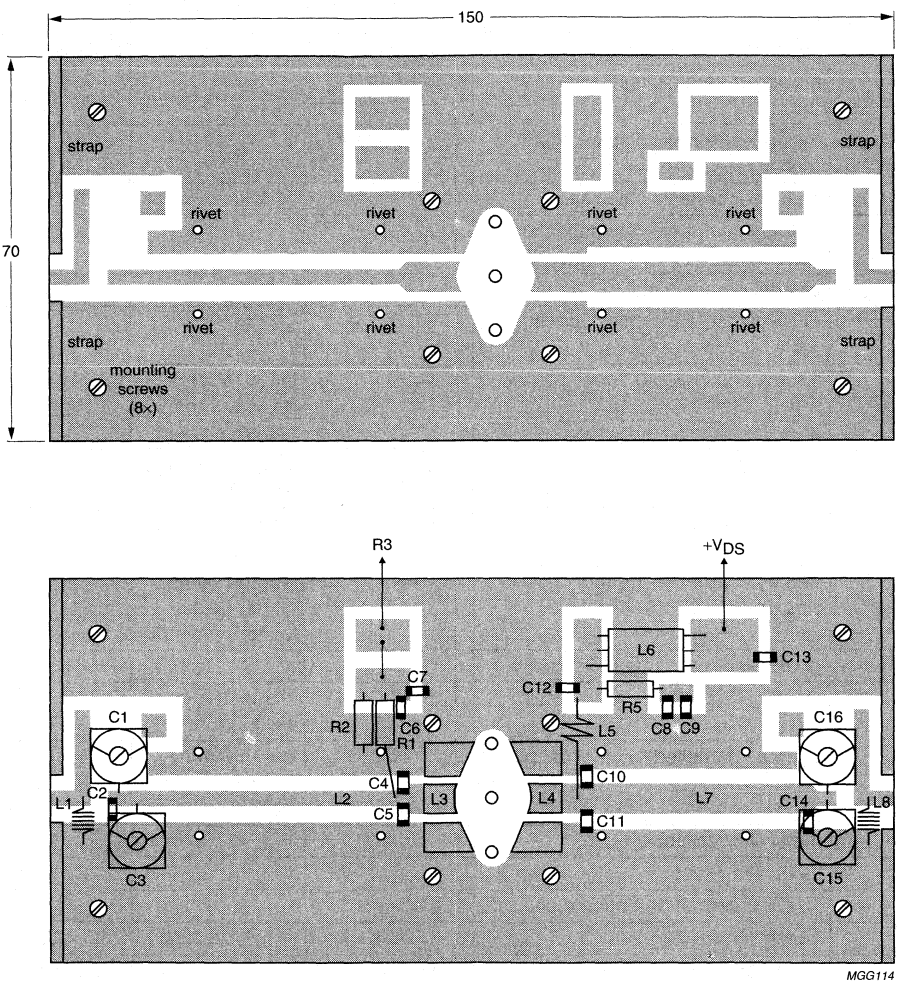
Fig.10 Test circuit for class-A operation at f = 225 MHz.

List of components (see Figs 10 and 11).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	2 to 18 pF		2222 809 09003
C2	multilayer ceramic chip capacitor (note 1)	10 pF, 500 V		
C3, C15, C16	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4, C5	multilayer ceramic chip capacitor (note 1)	56 pF, 500 V		
C6, C12	multilayer ceramic chip capacitor (note 1)	680 pF, 500 V		
C7, C8, C9	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C10, C11	multilayer ceramic chip capacitor (note 1)	43 pF, 500 V		
C13	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C14	multilayer ceramic chip capacitor (note 1)	27 pF, 500 V		
L1	4 turns enamelled 0.7 mm copper wire	42.4 nH	length 4 mm; int. dia. 3 mm; leads 2 × 5 mm	
L2	stripline (note 2)	50 Ω	length 49 mm; width 2.8 mm	
L3, L4	stripline (note 2)	31 Ω	length 11.5 mm; width 6 mm	
L5	2 turns enamelled 1.5 mm copper wire	18.7 nH	length 8 mm; int. dia. 4 mm; leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36642
L7	stripline (note 2)	31 Ω	length 40 mm; width 6 mm	
L8	3 turns enamelled 1.5 mm copper wire	28.8 nH	length 8 mm; int. dia. 4 mm; leads 2 × 5 mm	
R1	metal film resistor	1 kΩ, 0.4 W		2322 151 71002
R2	metal film resistor	100 kΩ, 0.4 W		2322 151 71004
R3	10 turns cermet potentiometer	100 Ω		
R4	metal film resistor	316 kΩ, 0.4 W		2322 153 53161
R5	metal film resistor	10 Ω, 0.4 W		2322 153 51009

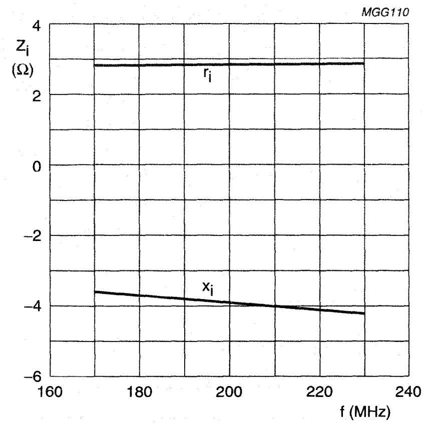
Notes

1. American Technical Ceramics capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board with epoxy fibre-glass dielectric (ε_r = 4.5); thickness $^1/_{16}$ inch.



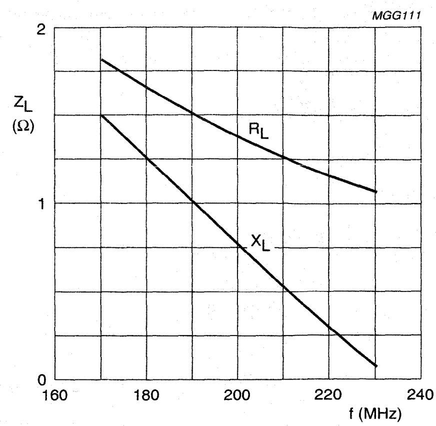
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

Fig.11 Component layout for 225 MHz class-A test circuit.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.12 Input impedance as a function of frequency (series components); typical values.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.13 Load impedance as a function of frequency (series components); typical values.

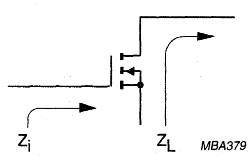
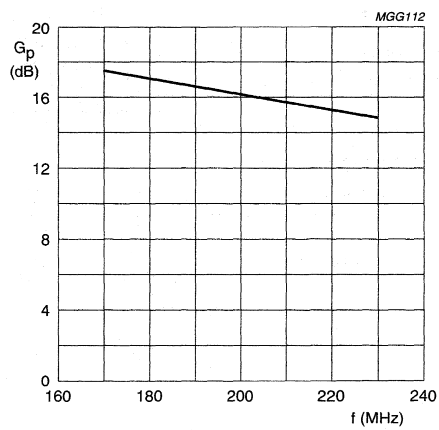


Fig.14 Definition of MOS impedance.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.15 Power gain as a function of frequency; typical values.

VHF linear push-pull power MOS transistor | BLF348

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262 A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

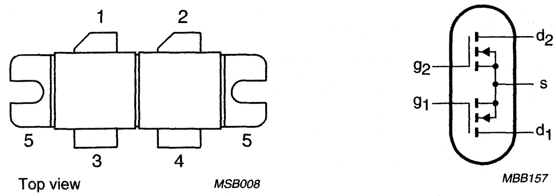


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environment safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance in a push-pull common source test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	d_{im} (dB) (note 1)	$P_{o\ sync}$ (W)	G_p (dB)
class-A	224.25	28	2 × 4.6	70	−52	> 67	> 11
	224.25	28	2 × 4.6	25	−52	typ. 75	typ. 13

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

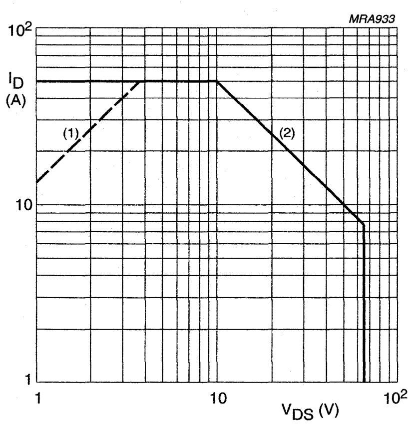
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

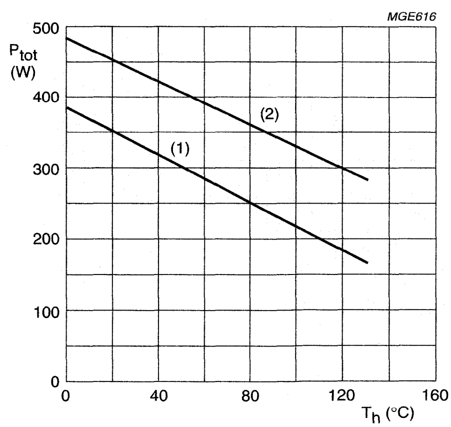
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



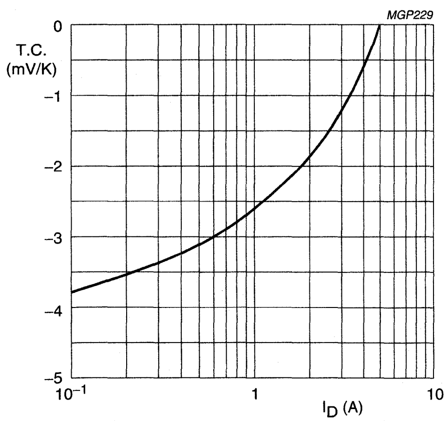
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

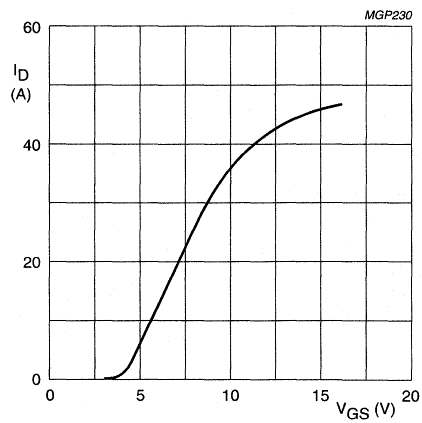
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.1 A	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.1 A; V_{DS} = 10 V	2	–	4.5	V
$\Delta V_{GS(th)}$	gate-source voltage difference of both transistor sections	I_D = 0.1 A; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	I_D = 8 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	495	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	340	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF



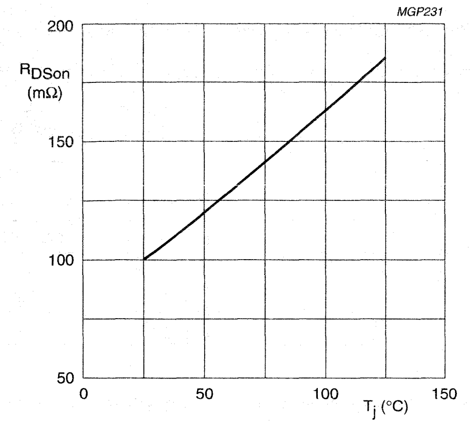
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



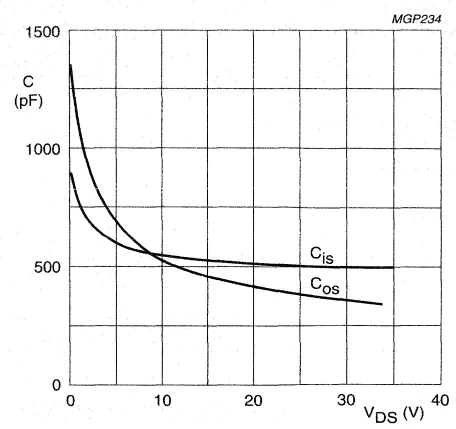
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



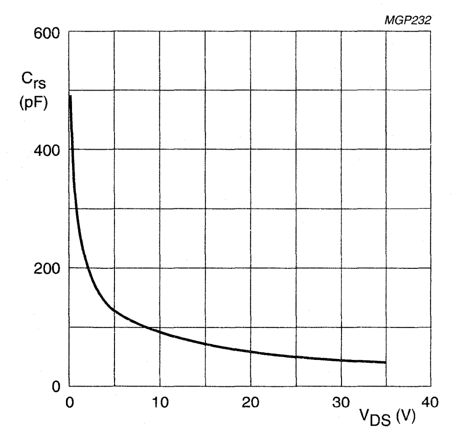
I_D = 8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

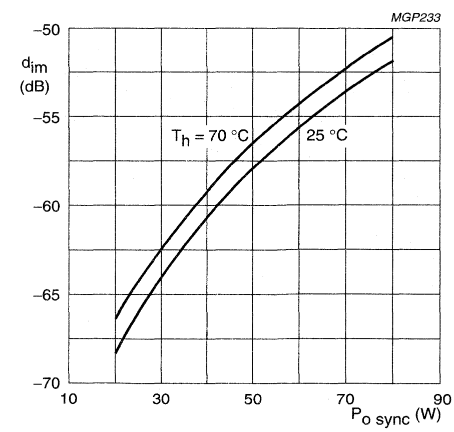


Fig.9 Intermodulation distortion as a function of peak synchronized output power.

APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 70 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W unless otherwise specified.
RF performance in a linear amplifier (common source circuit class-A circuit).
R_{GS} = 82 Ω per section; optimum load impedance per section = 0.14 + j0.14 Ω.

MODE OF OPERATION	f_{vision} (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	d_{im} (dB) (note 1)	$P_{o\ sync}$ (W)	G_p (dB)
class-A	224.25	28	2 × 4.6	70	−52	> 67 typ. 70	> 11 typ. 12.5
	224.25	28	2 × 4.6	25	−52	typ. 75	typ. 13
	224.25	28	2 × 4.6	70	−55	> 54 typ. 57	> 11 typ.12.5
	224.25	28	2 × 4.6	25	−55	typ. 62	typ. 13

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

Ruggedness in class-A operation

The BLF348 is capable of withstanding a load mismatch corresponding to VSWR = 20 through all phases under the following conditions:

V_{DS} = 28 V; f = 224.25 MHz at rated output power.

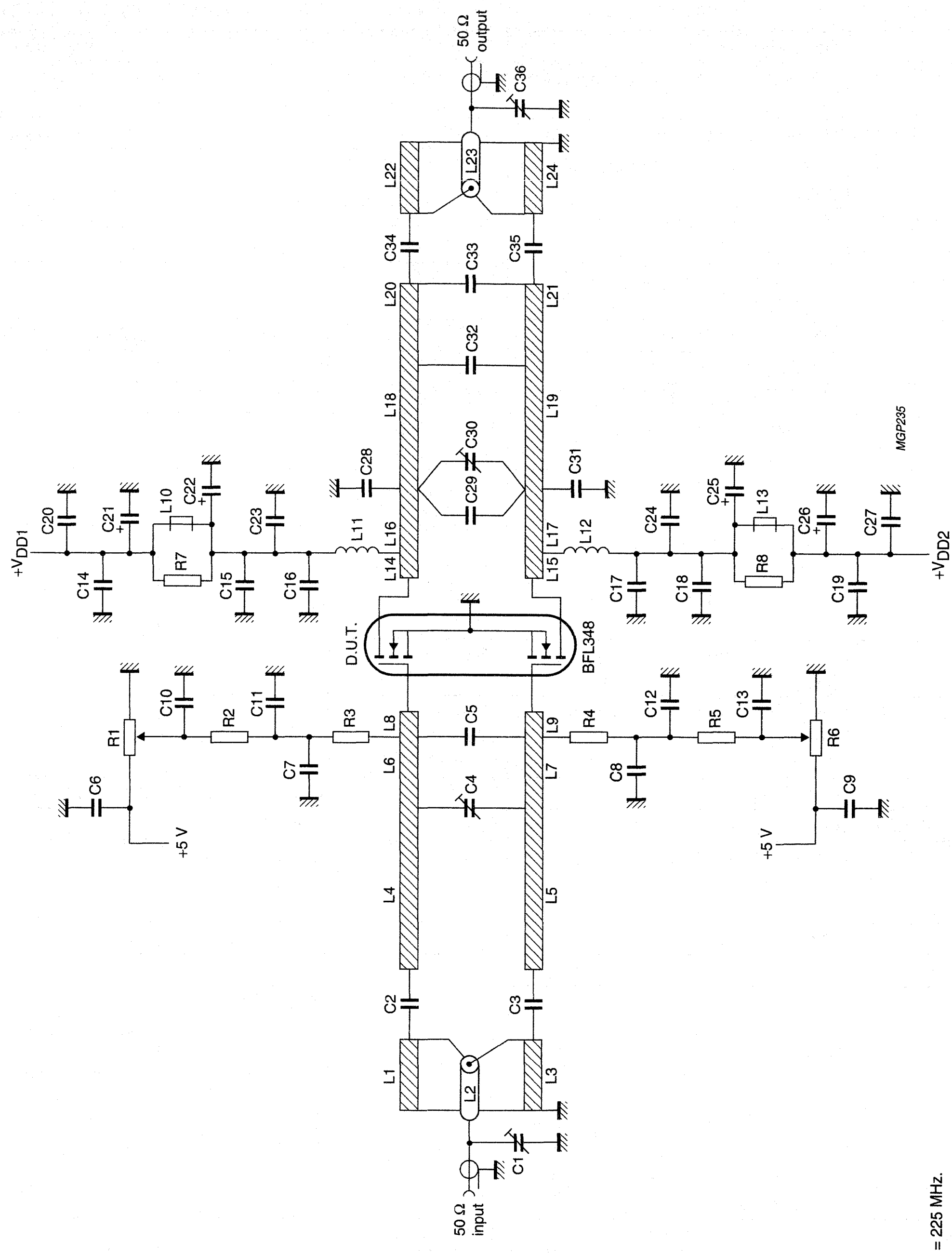


Fig.10 Test circuit for class-A operation.

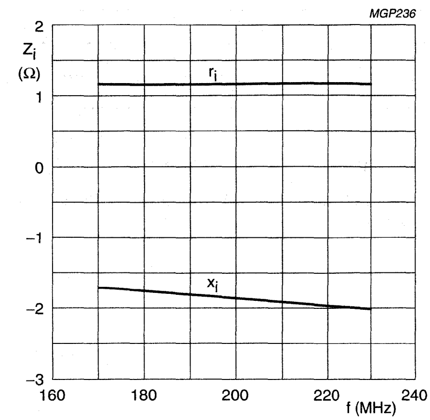
List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	2 to 9 pF		2222 809 09006
C2, C3	multilayer ceramic chip capacitor (note 1)	2 × 10 pF in parallel + 22 pF		
C4, C30	film dielectric trimmer	5 to 60 pF		2222 809 08003
C5	multilayer ceramic chip capacitor (note 1)	82 pF, 500 V		
C6, C9, C10, C13, C14, C19	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12, C20, C27	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C7, C8, C16, C17	MKT film capacitor	1 µF		2222 371 11105
C21, C26	electrolytic capacitor	10 µF, 63 V		
C22, C25	electrolytic capacitor	220 µF, 63 V		
C15, C18, C23, C24	multilayer ceramic chip capacitor (note 1)	510 pF, 500 V		
C28, C31	multilayer ceramic chip capacitor (note 1)	2 × 8.2 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor (note 1)	3 × 39 pF in parallel, 500 V		
C32	multilayer ceramic chip capacitor (note 1)	33 pF, 500 V		
C33	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C34, C35	multilayer ceramic chip capacitor (note 1)	10 pF + 18 pF + 62 pF (3 in parallel), 500 V		
C36	film dielectric trimmer	2 to 18 pF		2222 809 09003
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8 × 80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline (note 2)	43 Ω	6 × 32 mm	
L6, L7	stripline (note 2)	43 Ω	6 × 7 mm	
L8, L9	stripline (note 2)	43 Ω	6 × 7 mm	
L10, L13	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642
L11, L12	3/4 turn enamelled 2 mm copper wire	40 nH	space 1 mm int. dia. 10 mm leads 2 × 7 mm	
L14, L15	stripline (notes 2 and 4)	43 Ω	6 × 6 mm	
L16, L17	stripline (notes 2 and 4)	43 Ω	6 × 9.5 mm	
L18, L19	stripline (notes 2 and 4)	43 Ω	6 × 27.5 mm	
L20, L21	stripline (notes 2 and 4)	43 Ω	6 × 13 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
R1, R6	10 turns Bourns potentiometer	50 kΩ		
R2, R5	0.4 W metal film resistor	1 kΩ		
R3, R4	0.4 W metal film resistor	82 Ω		
R7, R8	1 W, ±5% metal film resistor	10 Ω		

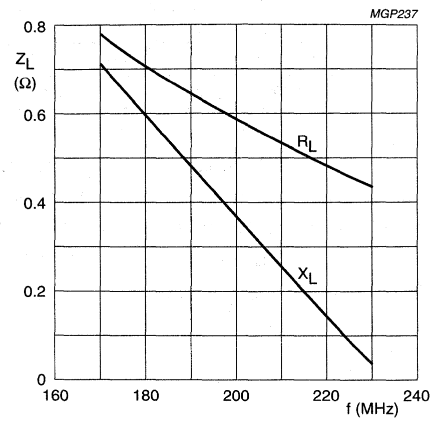
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 - L9, L14 - L22 and L24 are on a double copper-clad printed circuit board with glass microfibre PTFE dielectric ($\varepsilon_r = 2.2$); thickness $^1\!/_{16}$ inch; thickness of copper sheet 2 x 35 μm.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.
4. A copper strap, thickness 0.8 mm, is soldered on to striplines L14 - L21.



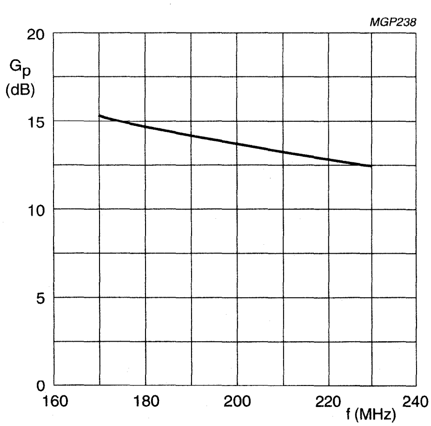
Class-A operation; V_{DS} = 28 V; I_{DQ} = 2 × 4.6 A;
R_{GS} = 82 Ω (per section); T_h = 70 °C.

Fig.11 Input impedance as a function of frequency (series components), typical values.



Class-A operation; V_{DS} = 28 V; I_{DQ} = 2 × 4.6 A;
R_{GS} = 82 Ω (per section); T_h = 70 °C.

Fig.12 Load impedance as a function of frequency (series components), typical values.



Class-A operation; V_{DS} = 28 V; I_{DQ} = 2 × 4.6 A;
R_{GS} = 82 Ω (per section); T_h = 70 °C.

Fig.13 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor BLF368

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262A1 balanced flange package, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

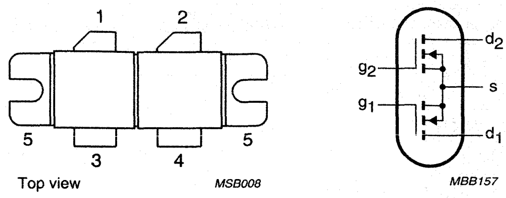


Fig.1 Simplified outline and symbol.

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	32	300	>12 typ. 13.5	>1 typ. 0.4	>55 typ. 62

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

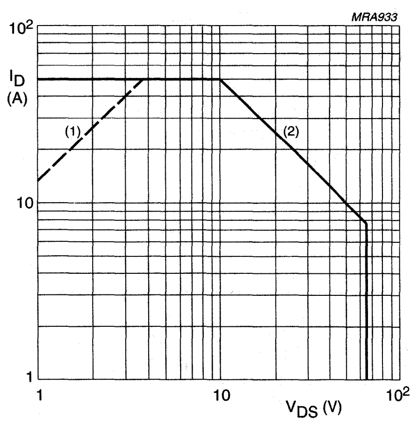
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V_{DSS}	drain-source voltage		–	65	V
V_{GSS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	25	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

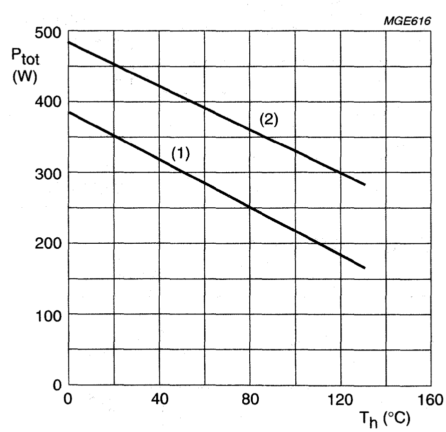
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15	K/W



(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



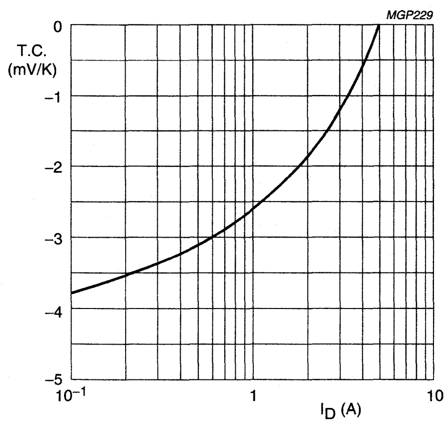
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

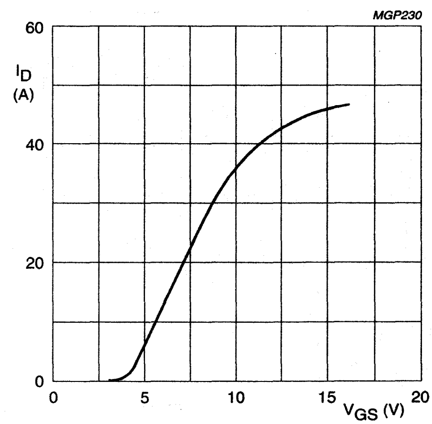
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 100 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 32 V	–	–	5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 100 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	I_D = 100 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	I_D = 8 A; V_{DS} = 10 V	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	I_D = 8 A; V_{DS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz	–	495	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz	–	340	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz	–	40	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



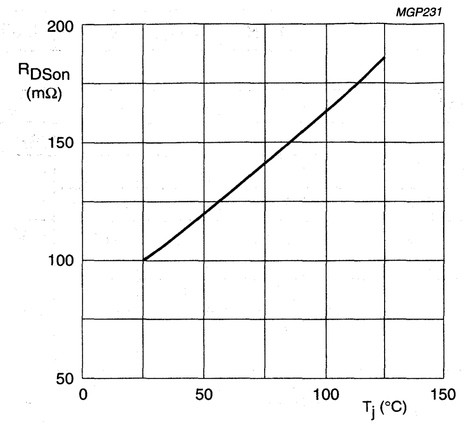
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



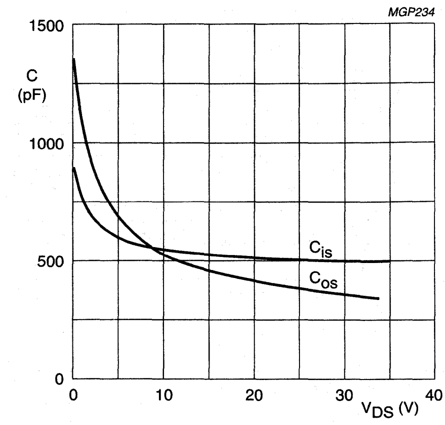
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



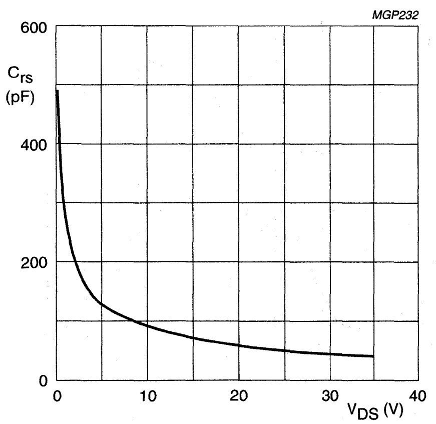
V_{GS} = 10 V; I_D = 8 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.15 K/W unless otherwise specified. RF performance in CW operation in a common source class-AB circuit. R_{GS} = 536 Ω per section; optimum load impedance per section = 1.34 + j0.34 Ω; V_{DS} = 32 V.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	32	2 × 250	300	>12 typ. 13.5	>1 typ. 0.4	>55 typ. 62
	225	28	2 × 250	300	typ. 13	typ. 0.7	typ. 68
	225	35	2 × 250	300	typ. 14	typ. 0.2	typ. 60
	175	28	2 × 250	300	typ. 15	typ. 0.5	typ. 70

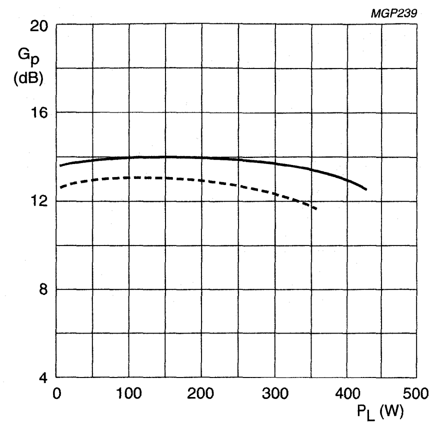
Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

Ruggedness in class-AB operation

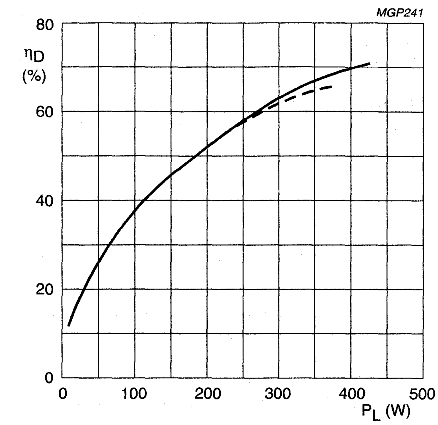
The BLF368 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 32 V; f = 225 MHz at rated output power.



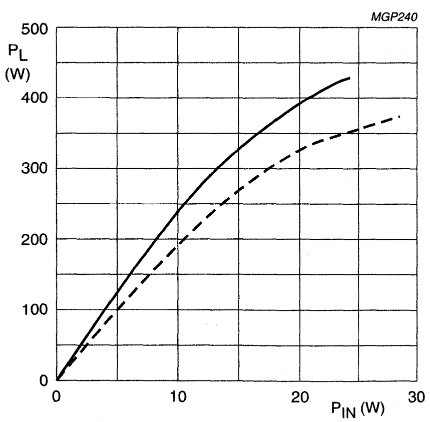
Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 × 250 mA;
Z_L = 1.34 + j0.34 Ω (per section); R_{GS} = 536 Ω (per section);
f = 225 MHz.
solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power; typical values per section.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 × 250 mA;
Z_L = 1.34 + j0.34 Ω (per section); R_{GS} = 536 Ω (per section);
f = 225 MHz.
solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

Fig.10 Efficiency as a function of load power; typical values per section.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 × 250 mA;
Z_L = 1.34 + j0.34 Ω (per section); R_{GS} = 536 Ω (per section);
f = 225 MHz.
solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

Fig.11 Load power as a function of input power; typical values per section.

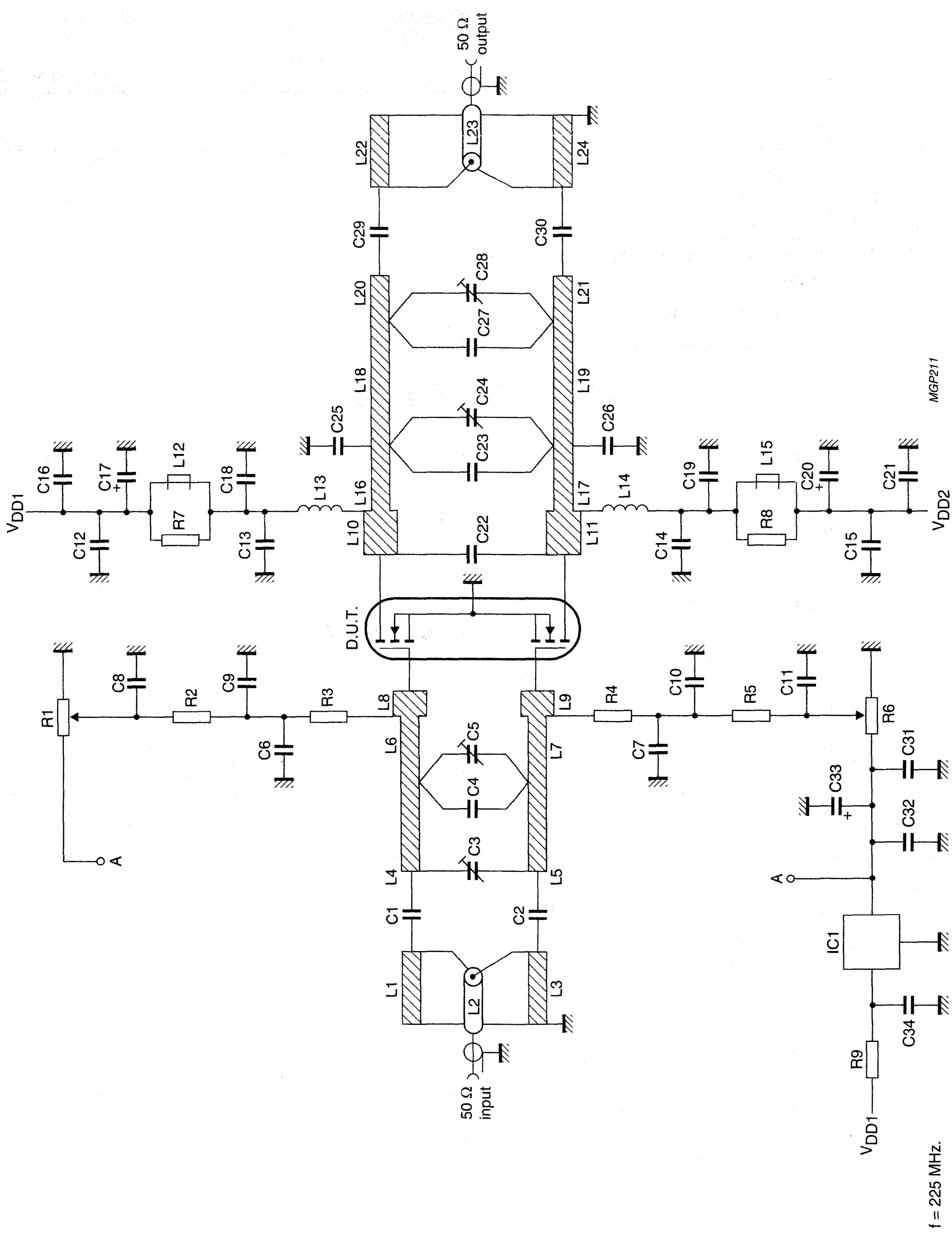


Fig.12 Test circuit for class-AB operation.

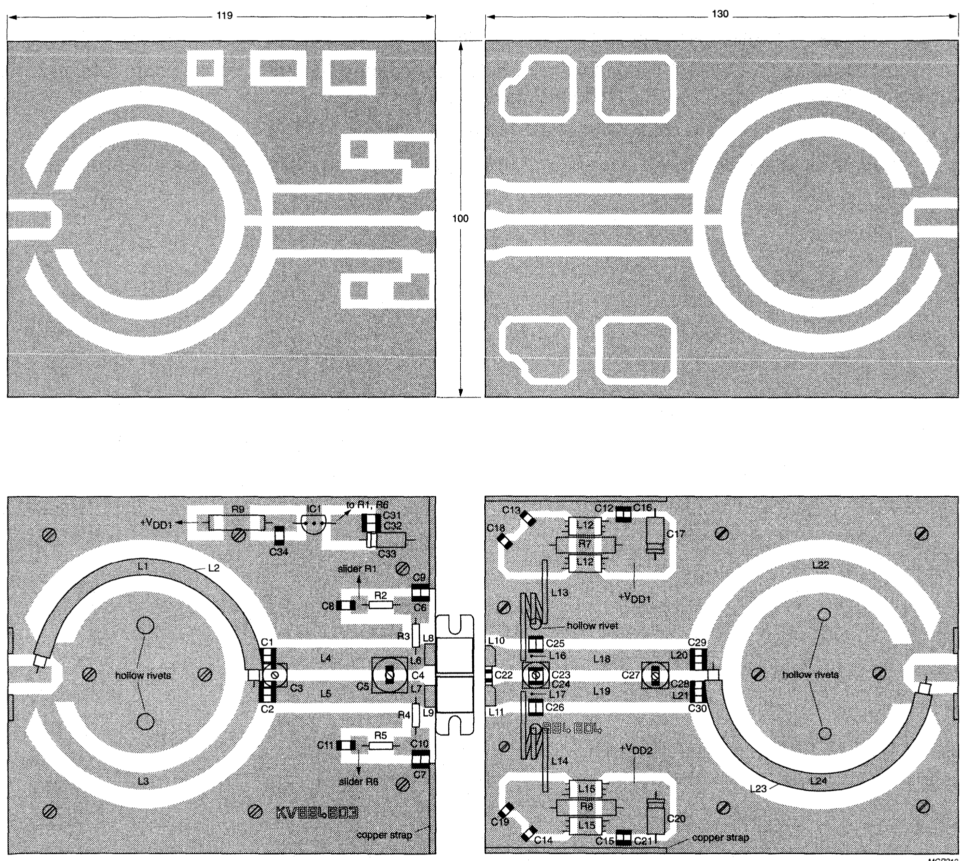
List of components class-AB test circuit (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor (note 1)	2×56 pF in parallel + 18 pF, 500 V		
C3	film dielectric trimmer	2 to 9 pF		2222 809 09005
C4	multilayer ceramic chip capacitor (note 1)	47 pF, 500 V		
C5	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6, C7, C9, C10, C12, C15, C31, C34	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		2222 852 47104
C8, C11, C16, C21, C32	multilayer ceramic chip capacitor (note 1)	100 nF, 50 V		
C17, C20, C33	electrolytic capacitor	10 μF, 63 V		
C22	multilayer ceramic chip capacitor (note 1)	82 pF, 500 V		
C23	multilayer ceramic chip capacitor (note 1)	10 pF + 30 pF in parallel, 500 V		
C24, C28	film dielectric trimmer	2 to 18 pF		2222 809 09006
C25, C26	multilayer ceramic chip capacitor (note 1)	39 pF + 47 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C29, C30	multilayer ceramic chip capacitor (note 1)	3×100 pF in parallel, 500 V		
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8×80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline (note 2)	43 Ω	6×32.5 mm	
L6, L7	stripline (note 2)	43 Ω	6×10.5 mm	
L8, L9	stripline (note 2)	43 Ω	6×3 mm	
L10, L11	stripline (note 2)	43 Ω	6×10.5 mm	
L12, L15	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642
L13, L14	2 turns enamelled 1.6 mm copper wire	25 nH	space 2.5 mm int. dia. 5 mm leads 2×7 mm	
L16, L17	stripline (notes 2 and 4)	43 Ω	6×3 mm	
L18, L19	stripline (notes 2 and 4)	43 Ω	6×35 mm	
L20, L21	stripline (notes 2 and 4)	43 Ω	6×9 mm	
R1, R6	10 turns potentiometer	50 kΩ		
R2, R5	metal film resistor	0.4 W, 1 kΩ		
R3, R4	metal film resistor	0.4 W, 536 Ω		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
R7, R8	metal film resistor	1 W, ±5%, 10 Ω		
R9	metal film resistor	1 W, 3.16 kΩ		
IC1	voltage regulator 78L05			

Notes

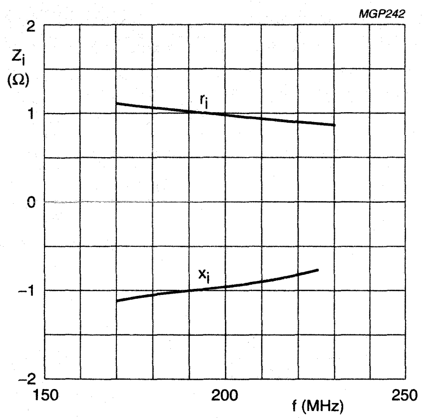
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 - L11, L16 - L22 and L24 are on a double copper-clad printed circuit board with glass microfibre PTFE dielectric ($\varepsilon_r = 2.2$); thickness $^1/_{16}$ inch; thickness of copper sheet 2×35 µm.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.
4. A copper strap, thickness 0.8 mm, is soldered over the complete striplines L16 - L21 to avoid overheating by large RF currents.



The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

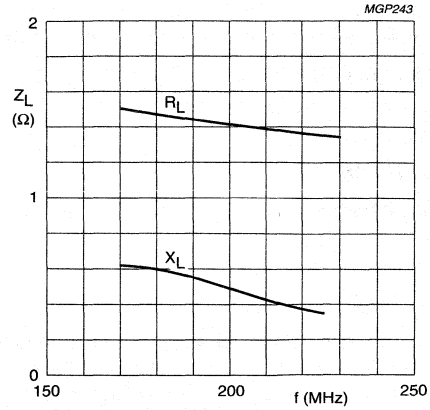
Dimensions in mm.

Fig.13 Component layout for 225 MHz class-AB test circuit.



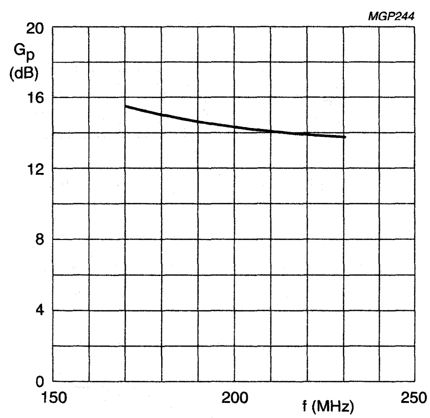
Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 × 250 mA;
R_{GS} = 536 Ω (per section); P_L = 300 W.

Fig.14 Input impedance as a function of frequency (series components); typical values per section.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 × 250 mA;
R_{GS} = 536 Ω (per section); P_L = 300 W.

Fig.15 Load impedance as a function of frequency (series components); typical values per section.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 × 250 mA;
R_{GS} = 536 Ω (per section); P_L = 300 W.

Fig.16 Power gain as a function of frequency; typical values per section.

VHF push-pull power MOS transistor BLF378

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Broadcast transmitter applications in the VHF frequency range.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT262A1 balanced flange package with two ceramic caps. The mounting flange provides the common source connection for the transistors.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

PINNING - SOT262A1

PIN	SYMBOL	DESCRIPTION
1	d_1	drain 1
2	d_2	drain 2
3	g_1	gate 1
4	g_2	gate 2
5	s	source

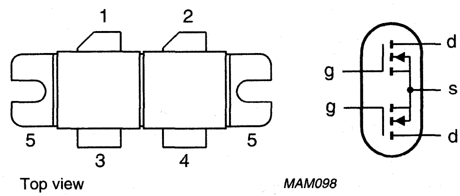


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	ΔG_p (dB)(1)	η_D (%)
CW, class-AB				>14	<1	>50
	225	50	250	typ. 16	typ. 0.6	typ. 55

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input / 25% synchronized output compression in television service (negative modulation, CCIR system).

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

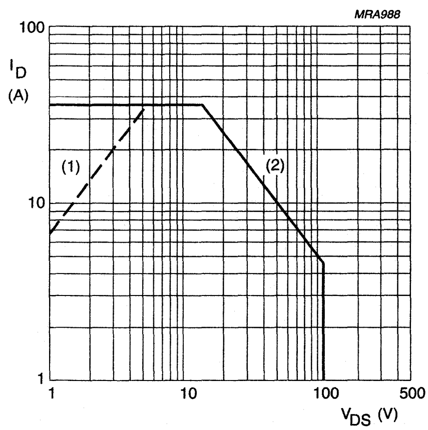
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V_{DSS}	drain-source voltage		–	110	V
V_{GSS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

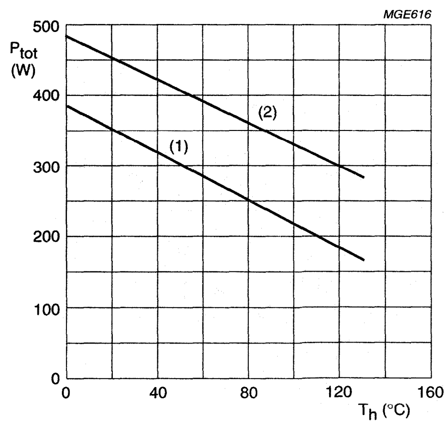
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15	K/W



Total device; both sections equally loaded.
(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



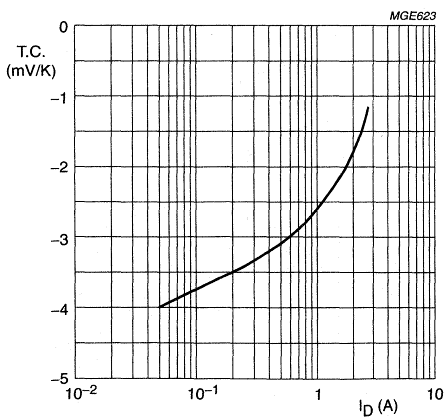
Total device; both sections equally loaded.
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

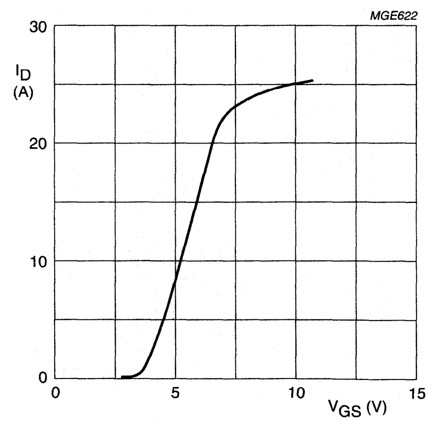
$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 50$ mA	110	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 50$ V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm20$ V; $V_{DS} = 0$	–	–	1	μA
V_{GSth}	gate-source threshold voltage	$I_D = 50$ mA; $V_{DS} = 10$ V	2.0	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	$I_D = 50$ mA; $V_{DS} = 10$ V	–	–	100	mV
g_{fs}	forward transconductance	$I_D = 5$ A; $V_{DS} = 10$ V	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	$I_D = 5$ A; $V_{DS} = 10$ V	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	$I_D = 5$ A; $V_{GS} = 10$ V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	$V_{GS} = 10$ V; $V_{DS} = 10$ V	–	25	–	A
C_{is}	input capacitance	$V_{GS} = 0$; $V_{DS} = 50$ V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	$V_{GS} = 0$; $V_{DS} = 50$ V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 50$ V; f = 1 MHz	–	14	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



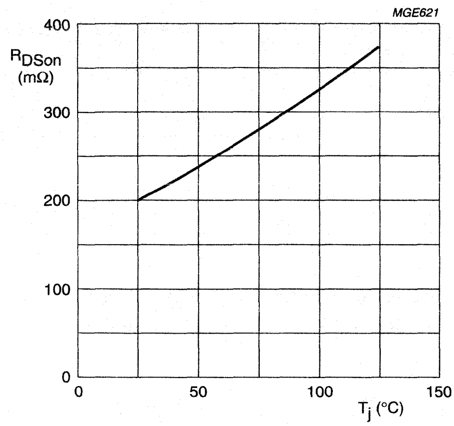
$V_{DS} = 10$ V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



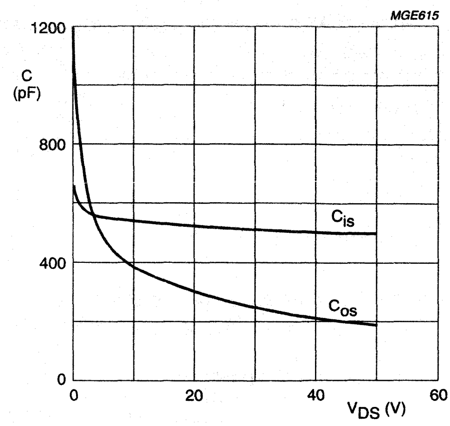
$V_{DS} = 10$ V; $T_j = 25$ °C.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



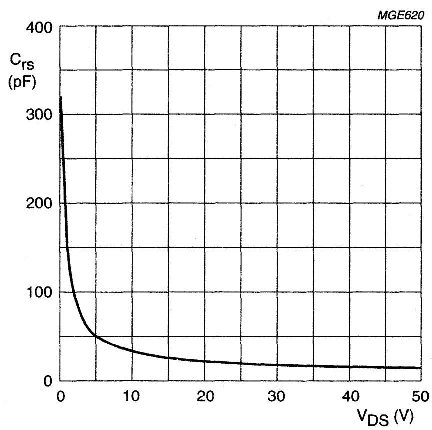
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION

Class-AB operation

RF performance in CW operation in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W unless otherwise specified. R_{GS} = 2.8 Ω per section; optimum load impedance per section = 0.74 + j2 Ω (V_{DS} = 50 V).

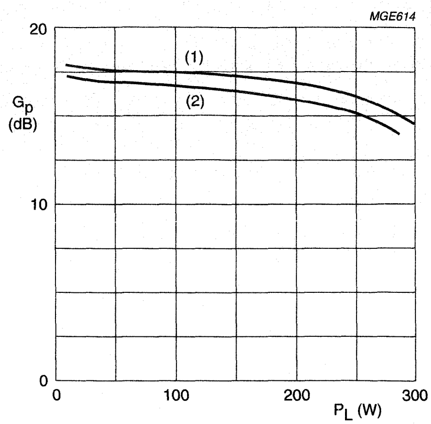
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	ΔG_p (dB)(1)	η_D (%)
CW, class-AB	225	50	2 × 0.5	250	>14 typ. 16	<1 typ. 0.6	>50 typ. 55
	225	45	2 × 0.5	250	typ. 15	typ. 1	typ. 60

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input / 25% synchronized output compression in television service (negative modulation, CCIR system).

Ruggedness in class-AB operation

The BLF378 is capable of withstanding a load mismatch corresponding to VSWR = 7 : 1 through all phases under the conditions: V_{DS} = 50 V; f = 225 MHz at rated output power.

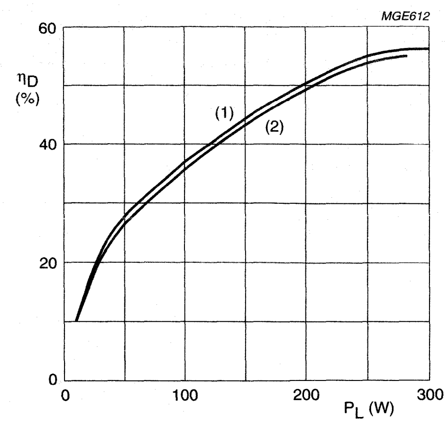


Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz;
Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.9 Power gain as a function of load power; typical values per section.

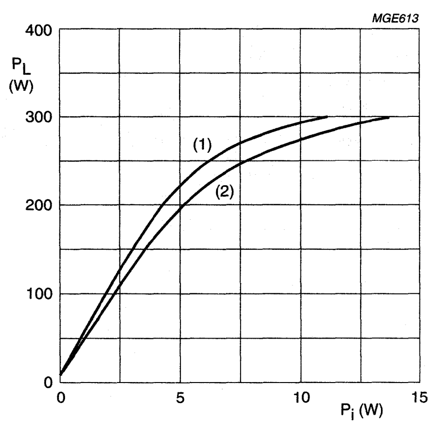


Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz;
Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.10 Efficiency as a function of load power; typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz;
Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.11 Load power as a function of input power; typical values per section.

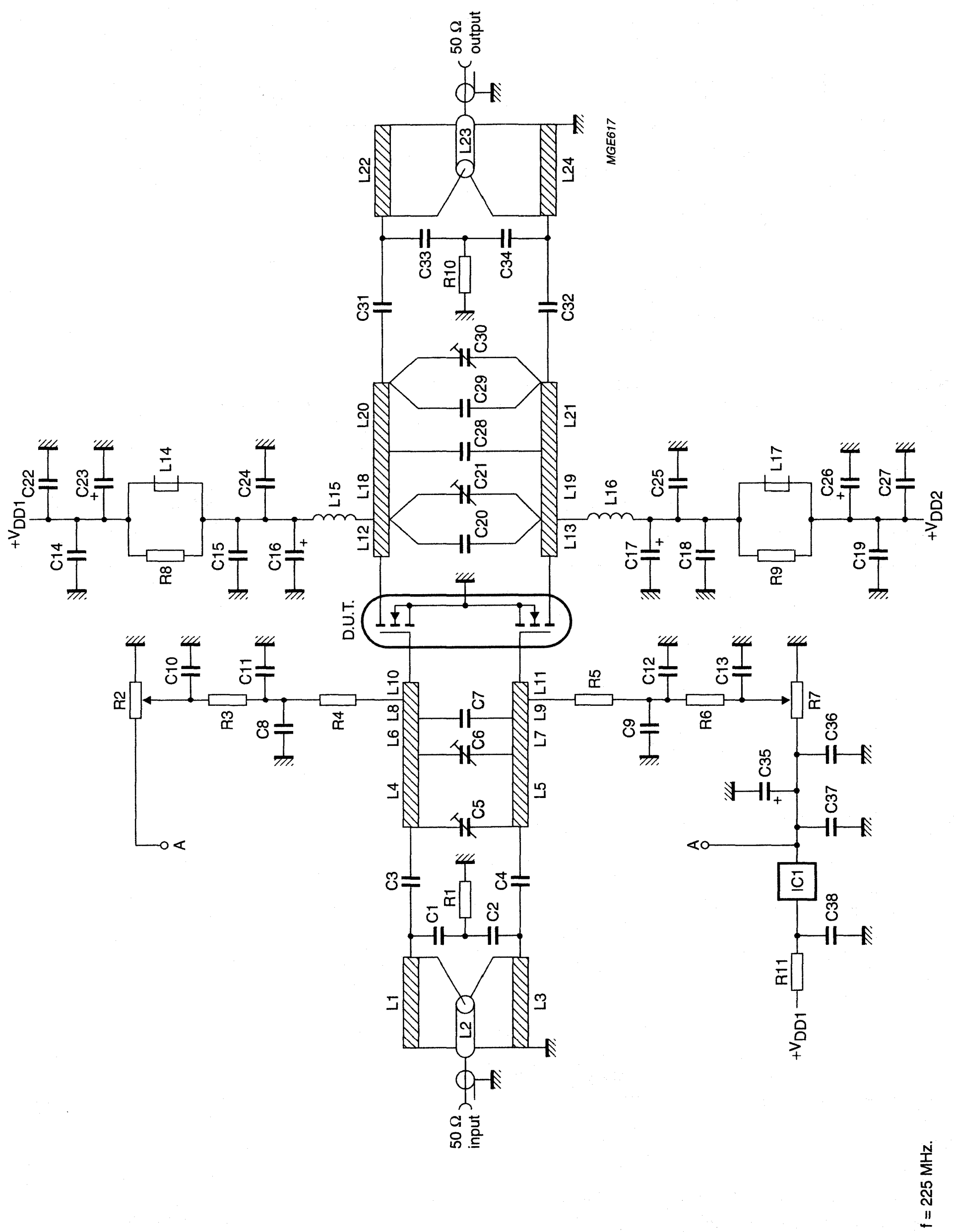


Fig.12 Test circuit for class-AB operation.

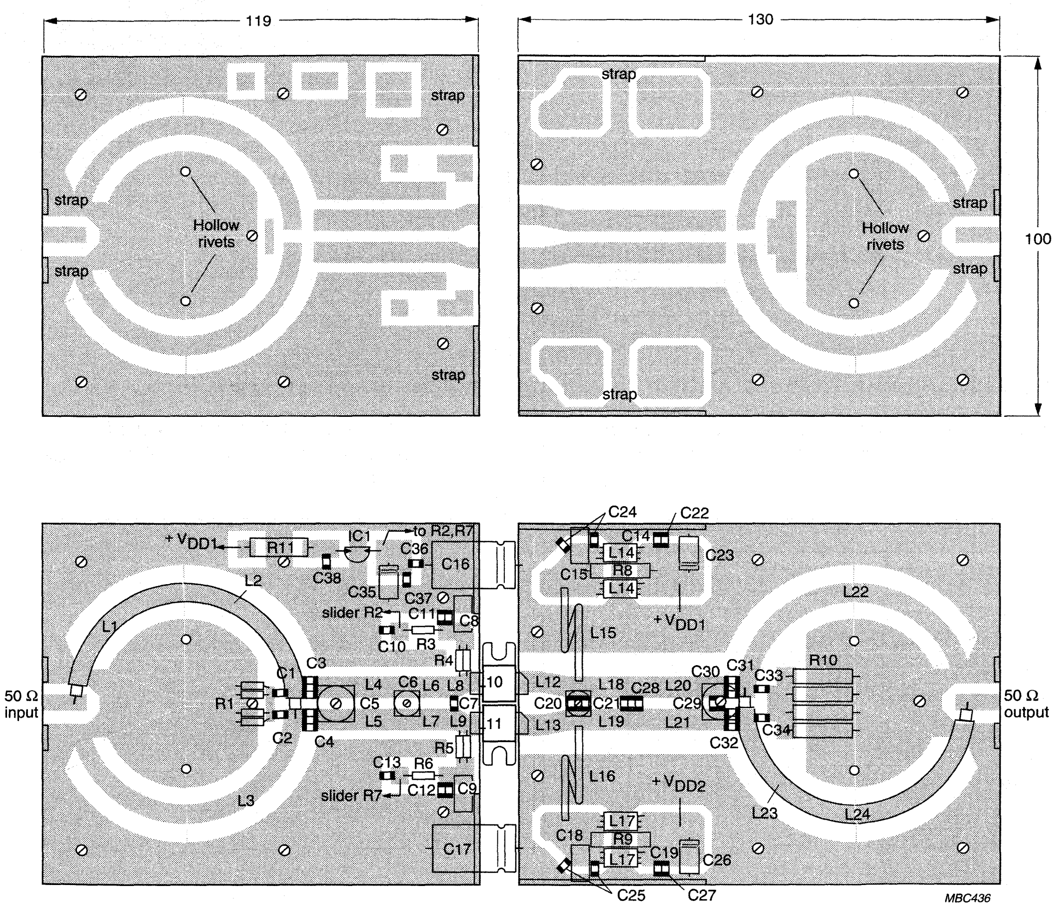
List of components class-AB test circuit (see Figs 12 and 13).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor; note 1	27 pF, 500 V		
C3, C4, C31, C32	multilayer ceramic chip capacitor; note 1	3 × 18 pF in parallel, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7	multilayer ceramic chip capacitor; note 1	100 pF, 500 V		
C8, C9, C15, C18	MKT film capacitor	1 μF, 63 V		2222 371 11105
C10, C13, C14, C19, C36	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12	multilayer ceramic chip capacitor; note 1	2 × 1 nF in parallel, 500 V		
C16, C17	electrolytic capacitor	220 μF, 63 V		
C20	multilayer ceramic chip capacitor; note 1	3 × 33 pF in parallel, 500 V		
C21	film dielectric trimmer	2 to 9 pF		2222 809 09005
C22, C27, C37, C38	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C23, C26, C35	electrolytic capacitor	10 μF, 63 V		
C24, C25	multilayer ceramic chip capacitor; note 1	2 × 470 pF in parallel, 500 V		
C28	multilayer ceramic chip capacitor; note 1	2 × 10 pF in parallel + 18 pF, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 5.6 pF in parallel, 500 V		
C33, C34	multilayer ceramic chip capacitor; note 1	5.6 pF, 500 V		
L1, L3, L22, L24	stripline; note 2	50 Ω	4.8 × 80 mm	
L2, L23	semi-rigid cable; note 3	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline; note 2	43 Ω	6 × 24 mm	
L6, L7	stripline; note 2	43 Ω	6 × 14.5 mm	
L8, L9	stripline; note 2	43 Ω	6 × 4.4 mm	
L10, L11	stripline; note 2	43 Ω	6 × 3.2 mm	
L12, L13	stripline; note 2	43 Ω	6 × 15 mm	
L14, L17	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642
L15, L16	$1\frac{3}{4}$ turns enamelled 2 mm copper wire	40 nH	space 1 mm int. dia. 10 mm leads 2 × 7 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
L18, L19	stripline; note 2	43 Ω	6 × 13 mm	
L20, L21	stripline; note 2	43 Ω	6 × 29.5 mm	
R1	metal film resistor	4 × 0.4 W, 10 Ω		
R2, R7	10 turns potentiometer	50 kΩ		
R3, R6	metal film resistor	0.4 W, 1 kΩ		
R4, R5	metal film resistor	2 × 0.4 W, 5.62 Ω in parallel		
R8, R9	metal film resistor	1 W, 10 Ω, ±5%		
R10	metal film resistor	4 × 1 W, 10 Ω in parallel		
R11	metal film resistor	1 W, 5.11 kΩ		
IC1	voltage regulator 78L05			

Notes

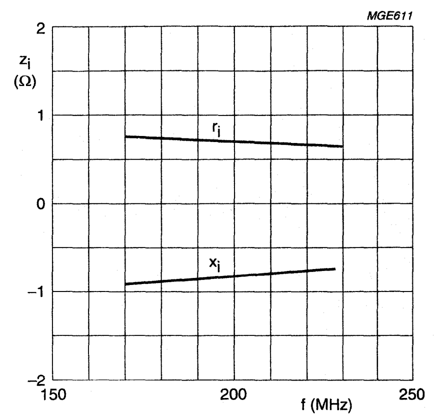
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 to L13, L18 to L22 and L24 are on a double copper-clad printed-circuit board with glass microfibre PTFE dielectric ($\varepsilon_r = 2.2$); thickness $^1\!/_{16}$ inch; thickness of copper sheet 2 × 35 μm.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.



Dimensions in mm.

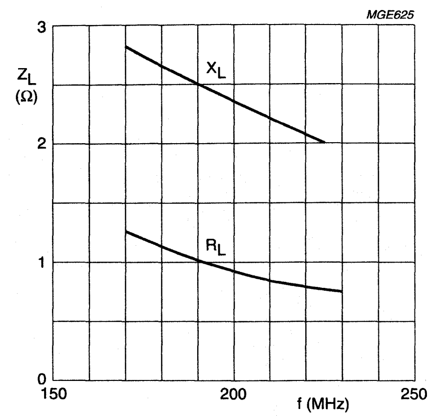
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.13 Printed-circuit board and component layout for 225 MHz class-AB test circuit.



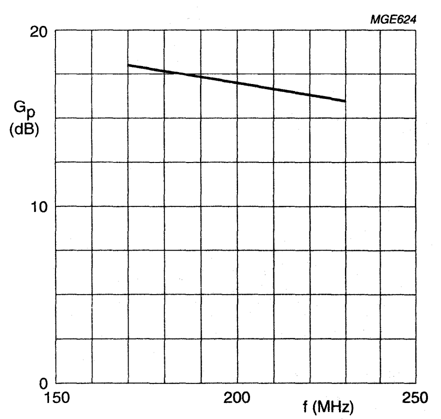
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.14 Input impedance as a function of frequency (series components); typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.15 Load impedance as a function of frequency (series components); typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.16 Power gain as a function of frequency; typical values per section.

UHF power MOS transistor BLF404

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch
- Designed for broadband operation.

APPLICATIONS

- Communication transmitters in the VHF/UHF range with a nominal supply voltage of 12.5 V.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS power transistor in an 8-lead SOT409A SMD package with a ceramic cap.

PINNING

PIN	DESCRIPTION
1, 8	source
2, 3	gate
4, 5	source
6, 7	drain

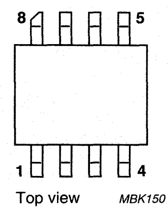


Fig.1 Simplified outline SOT409A.

QUICK REFERENCE DATA

RF performance at $T_{mb} \leq 60$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW class-AB	500	12.5	4	≥10	≥50

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

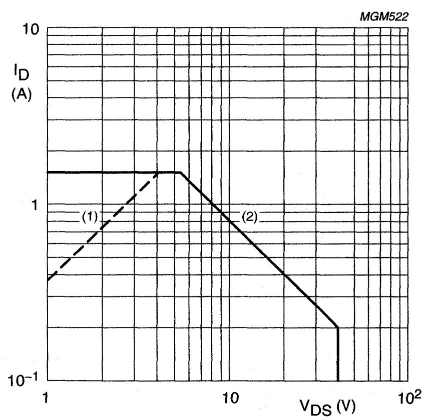
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
V_{GS}	gate-source voltage		–	±20	V
I_D	DC drain current		–	1.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 85$ °C	–	8.3	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_{mb} \leq 85$ °C, $P_{tot} = 8.3$ W	12.1	K/W



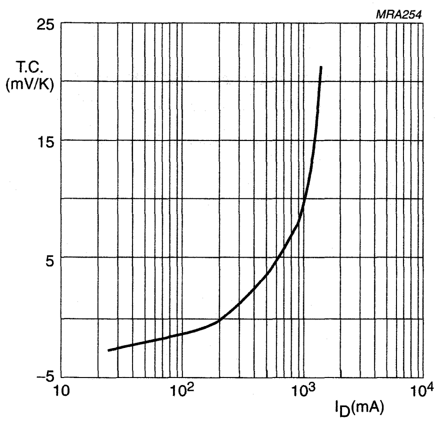
(1) Current in this area may be limited by R_{DSon}.
(2) $T_{mb} = 85$ °C.

Fig.2 DC SOAR.

CHARACTERISTICS

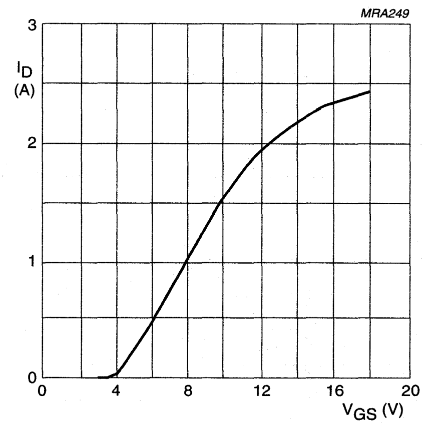
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	40	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	1	μA
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	2.3	–	A
R_{DSon}	drain-source on-state resistance	I_D = 0.7 A; V_{GS} = 15 V	–	1.8	2.7	Ω
g_{fs}	forward transconductance	I_D = 0.7 A; V_{DS} = 10 V	200	270	–	mS
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	14	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	17	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	3	–	pF



V_{DS} = 10 V.

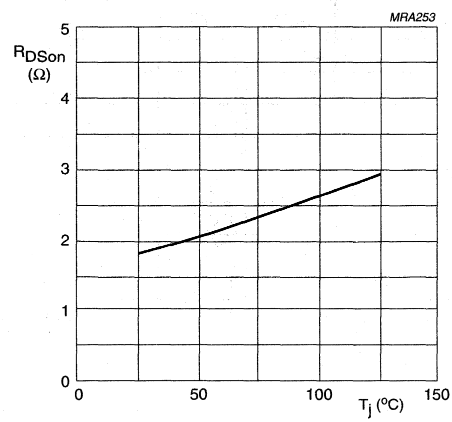
Fig.3 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



V_{DS} = 10 V; T_j = 25 °C.

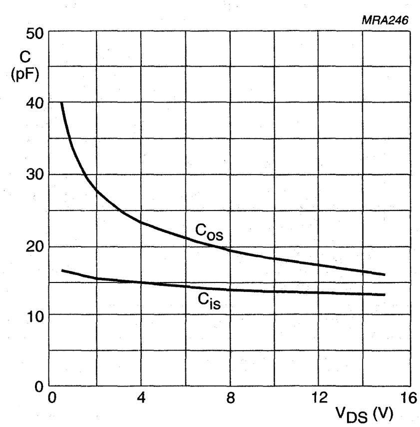
Fig.4 Drain current as a function of gate-source voltage; typical values.

UHF power MOS transistor BLF404



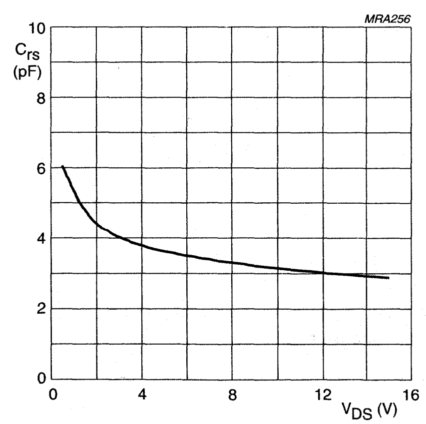
I_D = 0.7 A; V_{GS} = 15 V.

Fig.5 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.6 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.7 Feedback capacitance as a function of drain-source voltage; typical values.

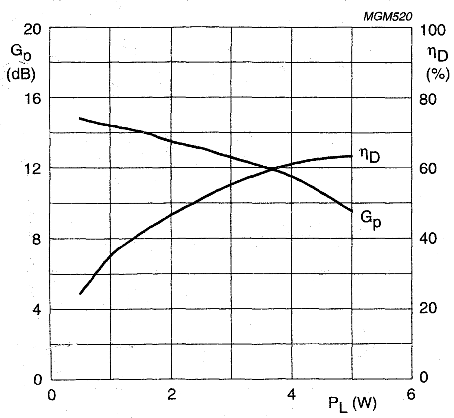
APPLICATION INFORMATION

RF performance at $T_{mb} \leq 60$ °C in a common source test circuit with the device soldered on a printed-circuit board with through metallized holes.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	500	12.5	50	4	≥10 typ. 11.5	≥50 typ. 55

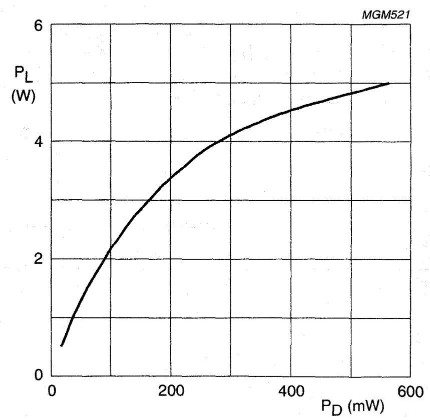
Ruggedness in class-AB operation

The BLF404 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: f = 500 MHz; V_{DS} = 12.5 V; P_L = 4 W; $T_{mb} \leq 60$ °C.



CW, class-AB operation; f = 500 MHz; V_{DS} = 12.5 V; I_{DQ} = 50 mA; $T_{mb} \leq 60$ °C.

Fig.8 Power gain and drain efficiency as functions of load power; typical values.



CW, class-AB operation; f = 500 MHz; V_{DS} = 12.5 V; I_{DQ} = 50 mA; $T_{mb} \leq 60$ °C.

Fig.9 Load power as a function of drive power; typical values.

Test circuit information

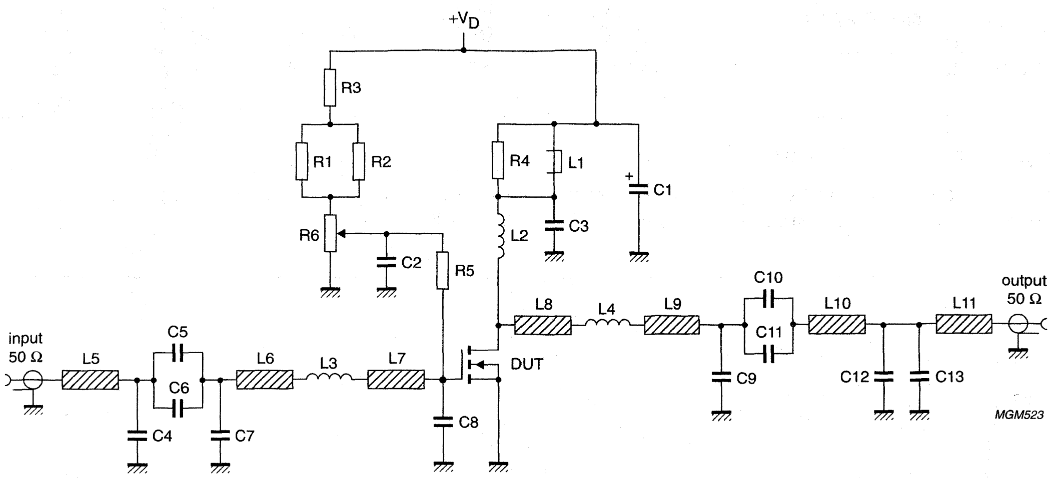


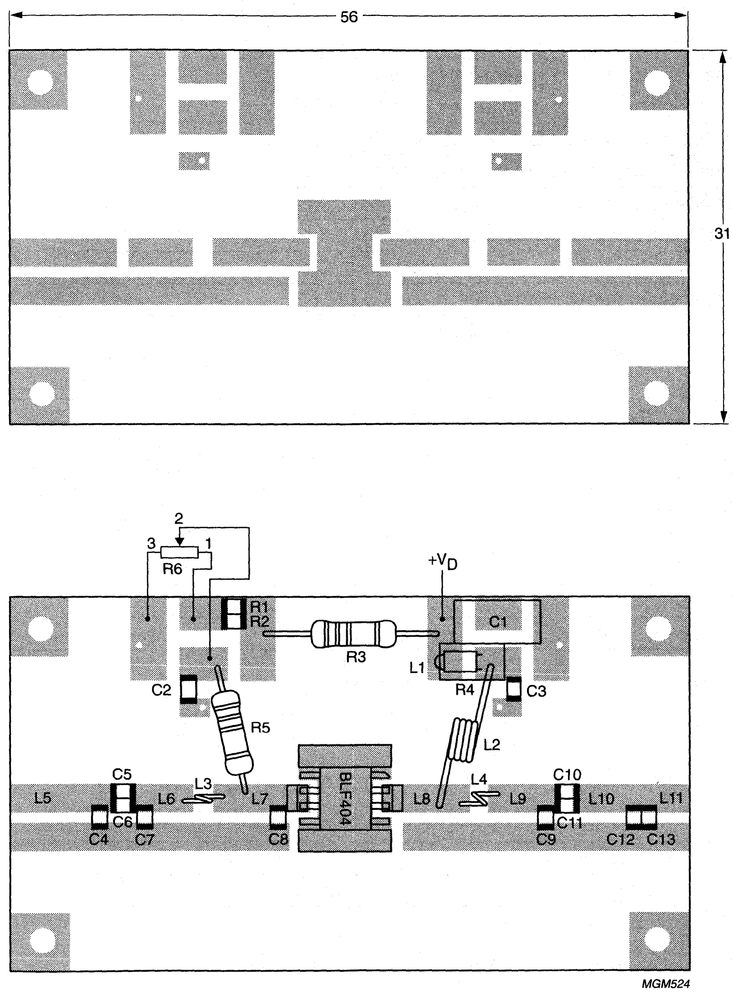
Fig.10 Class-AB common source test circuit at f = 500 MHz.

List of components used in test circuit (see Figs 10 and 11).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1	electrolytic capacitor	4.7 μF, 10 V		
C2, C3	multilayer ceramic chip capacitor	47 nF		
C4	multilayer ceramic chip capacitor; note 1	18 pF		
C5, C10	multilayer ceramic chip capacitor; note 1	180 pF		
C6, C11	multilayer ceramic chip capacitor; note 1	270 pF		
C7	multilayer ceramic chip capacitor; note 1	22 pF		
C8	multilayer ceramic chip capacitor; note 1	8.2 pF		
C9	multilayer ceramic chip capacitor; note 1	2.7 pF		
C12	multilayer ceramic chip capacitor; note 1	1.2 pF		
C13	multilayer ceramic chip capacitor; note 1	12 pF		
L1	2 turns 1 mm enamelled copper wire on a grade 4B1 Ferroxcube core		ext. dia. = 4.2 mm int. dia. = 2 mm length = 6 mm	
L2	3 turns 1 mm enamelled copper wire		int. dia. = 4.6 mm leads = 2 x 5 mm	
L3	bifilar coil		lead dia. = 0.8 mm	
L4	bifilar coil		lead dia. = 1 mm	
L5	stripline; note 2	50 Ω	8.8 × 2.38 mm	
L6	stripline; note 2	50 Ω	5.8 × 2.38 mm	
L7	stripline; note 2	50 Ω	6.8 × 2.38 mm	
L8	stripline; note 2	50 Ω	3.76 × 2.38 mm	
L9	stripline; note 2	50 Ω	5.8 × 2.38 mm	
L10	stripline; note 2	50 Ω	4.48 × 2.38 mm	
L11	stripline; note 2	50 Ω	3.13 × 2.38 mm	
R1, R2	SMD resistor	3.9 kΩ		
R3	metal film resistor	1 kΩ, 0.25 W		
R4	metal film resistor	22 Ω, 0.25 W		
R5	metal film resistor	10 kΩ, 0.25 W		
R6	potentiometer	10 kΩ		

Notes

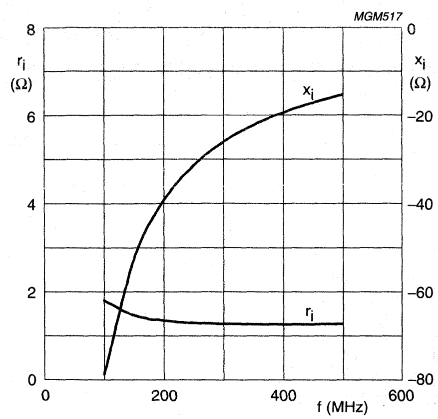
1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad printed circuit board, with DUROID dielectric (ε_r = 2.2); thickness 0.79 mm, thickness of the copper sheet 2 x 35 μm.



Dimensions in mm.

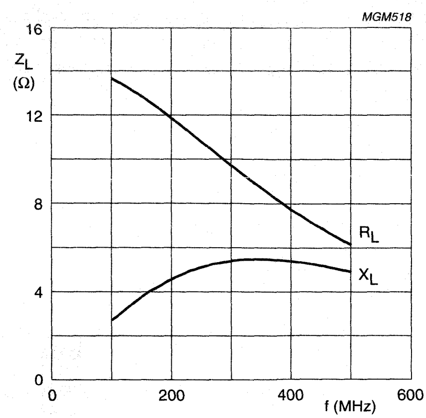
The components are situated on one side of the copper-clad printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.11 Printed-circuit board and component layout for 500 MHz class-AB test circuit in Fig.10.



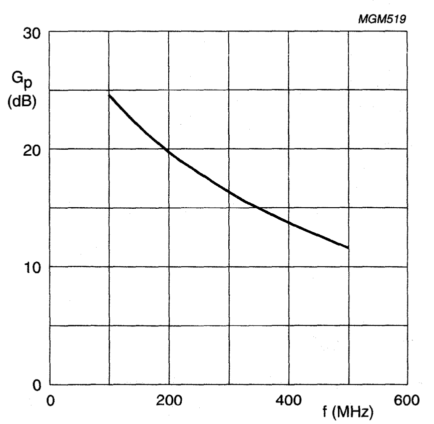
CW, class-AB operation; V_{DS} = 12.5 V; I_D = 50 mA;
P_L = 4 W; T_{mb} ≤ 60 °C.

Fig.12 Input impedance as a function of frequency (series components); typical values.



CW, class-AB operation; V_{DS} = 12.5 V; I_D = 50 mA;
P_L = 4 W; T_{mb} ≤ 60 °C.

Fig.13 Load impedance as a function of frequency (series components); typical values.

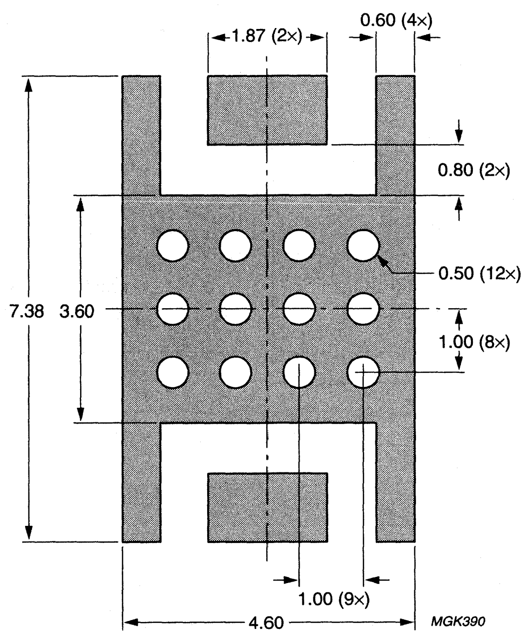


CW, class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA;
P_L = 4 W; T_{mb} ≤ 60 °C.

Fig.14 Power gain as a function of frequency (series components); typical values.

MOUNTING RECOMMENDATIONS

Both the metallized groundplate and leads contribute to the heatflow. It is recommended that the transistor is mounted on a grounded metallized area of a maximum thickness of 0.8 mm on the printed-circuit board, equipped with at least 12 (0.5 mm diameter) through metallized holes filled with solder.
A thermal resistance $R_{th(mb-h)}$ of 5 K/W can be achieved if heatsink compound is applied when the transistor is mounted on the printed-circuit board.



Dimensions in mm.

Fig.15 Reflow soldering footprint for SOT409A.

UHF power MOS transistor | BLF521

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT172D studless envelope, with a ceramic cap. All leads are isolated from the mounting base.

PINNING - SOT172D

PIN	DESCRIPTION
1	source
2	gate
3	drain
4	source

PIN CONFIGURATION

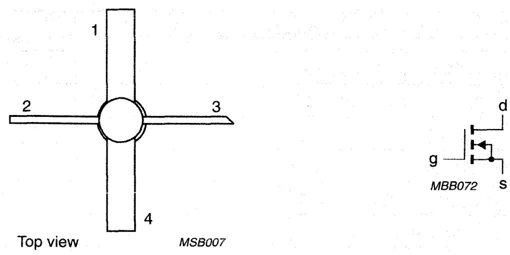


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_{amb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	12.5	2	> 10	> 50

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

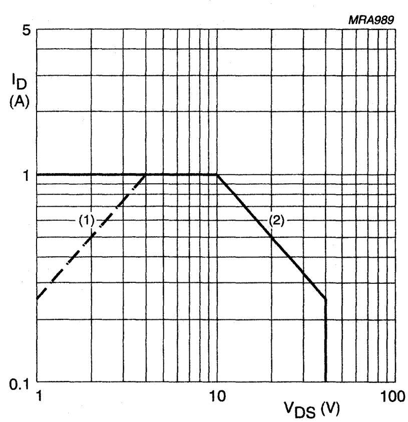
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	10	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	17.5 K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient (note 1)	75 K/W

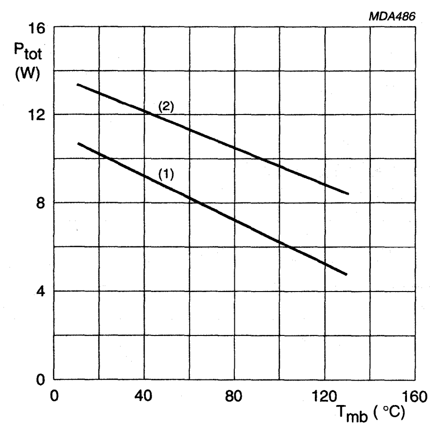
Note

1. Mounted on printed circuit board, see Fig.12.



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



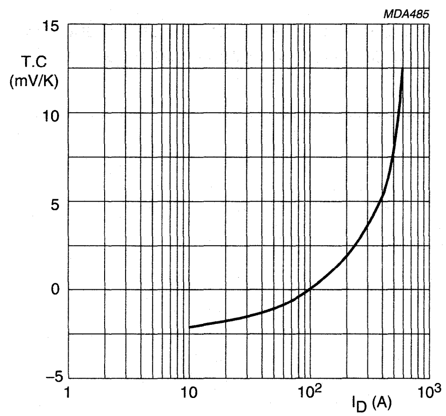
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

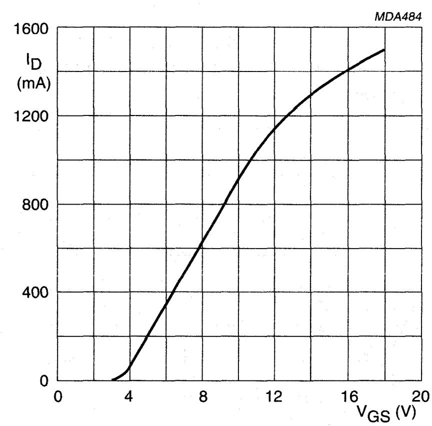
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	40	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	80	135	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.5	4	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	1.3	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	5.3	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	7.8	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	1.8	–	pF



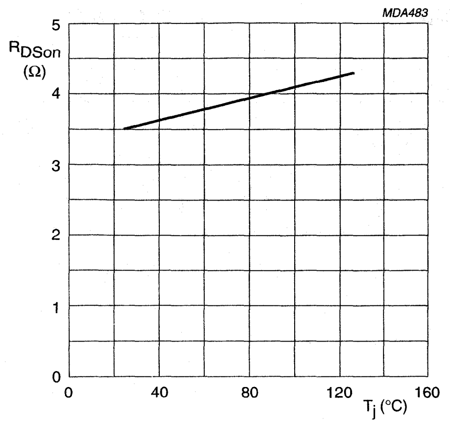
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



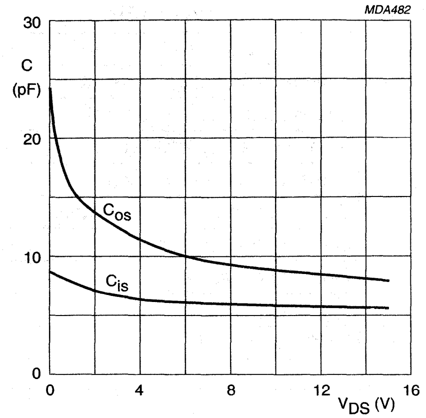
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



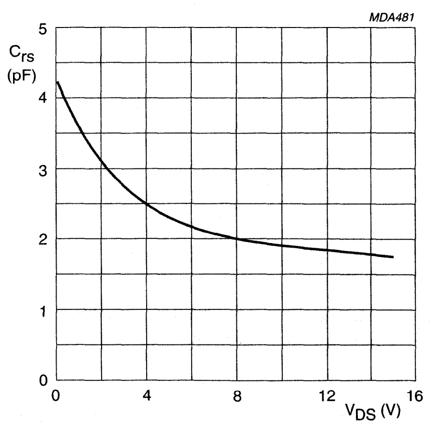
I_D = 0.3 A; V_{GS} = 15 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

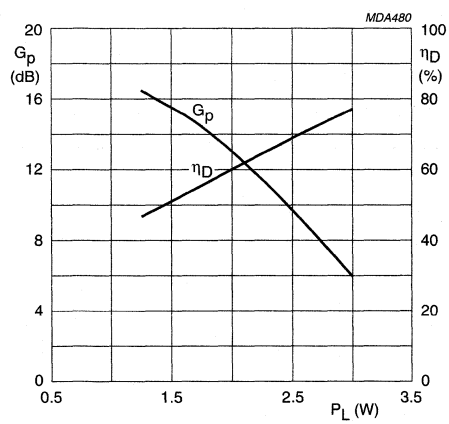
T_{amb} = 25 °C; R_{GS} = 274 Ω, unless otherwise specified.
RF performance in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	500	12.5	10	2	> 10 typ. 13	> 50 typ. 60

Ruggedness in class-B operation

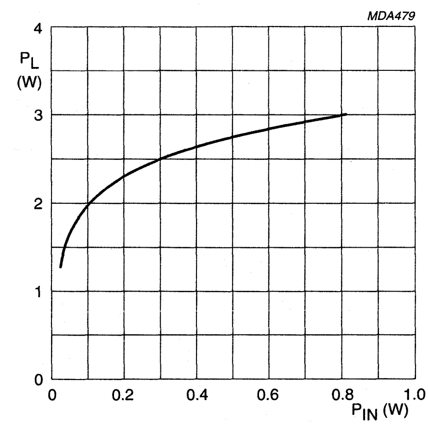
The BLF521 is capable of withstanding a load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{DS} = 15.5 V; f = 500 MHz at rated output power.



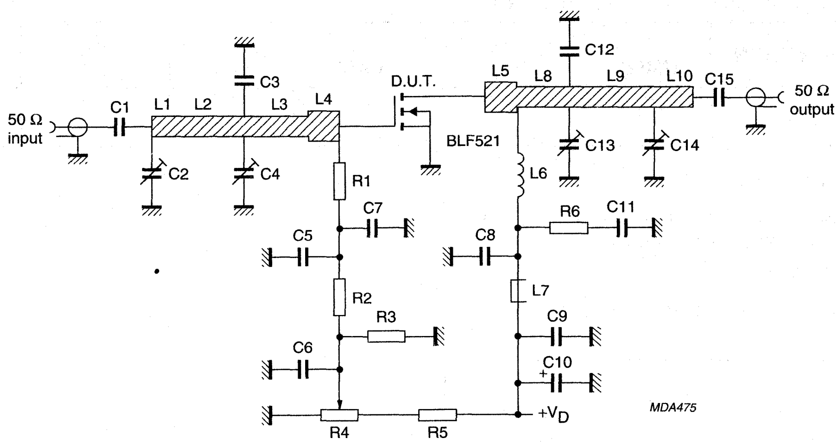
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA;
Z_L = 9.5 + j12.8; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA;
Z_L = 9.5 + j12.8; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

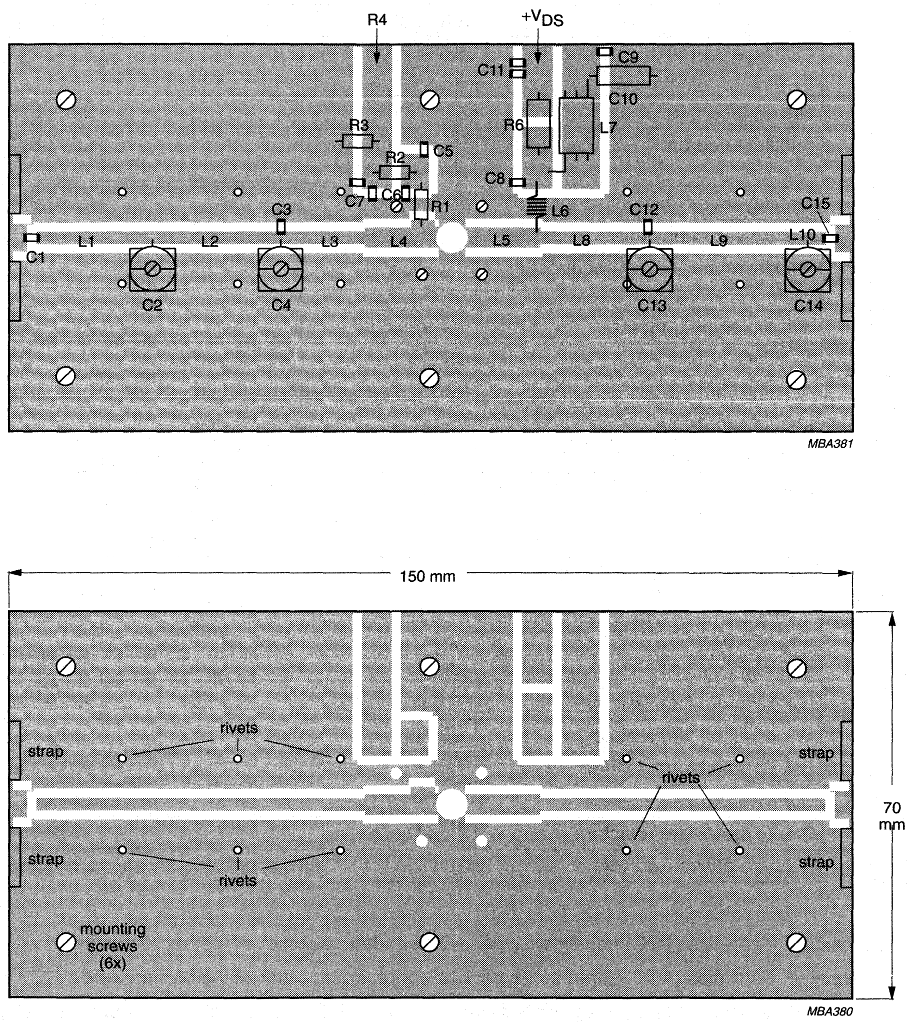
Fig.11 Test circuit for class-B operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C5, C8, C15	multilayer ceramic chip capacitor (note 1)	390 pF, 500 V		
C2, C13	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3	multilayer ceramic chip capacitor (note 2)	5.6 pF, 500 V		
C4	film dielectric trimmer	2 to 18 pF		2222 809 09003
C6, C11	multilayer ceramic chip capacitor	2 × 100 nF in parallel, 50 V		2222 852 47104
C7, C9	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C10	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C12	multilayer ceramic chip capacitor (note 2)	9.1 pF, 50 V		
C14	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
L1	stripline (note 3)	83 Ω	20 × 2 mm	
L2	stripline (note 3)	83 Ω	21 × 2 mm	
L3	stripline (note 3)	83 Ω	19 × 2 mm	
L4, L5	stripline (note 3)	67 Ω	12 × 3 mm	
L6	5 turns enamelled 0.5 mm copper wire	62 nH	length 3.75 mm int. dia. 3 mm leads 2 × 4 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L8	stripline (note 3)	83 Ω	18.6 × 2 mm	
L9	stripline (note 3)	83 Ω	31.6 × 2 mm	
L10	stripline (note 3)	83 Ω	2 × 2 mm	
R1	0.4 W metal film resistor	274 Ω		2322 151 72741
R2	0.4 W metal film resistor	1.96 kΩ		2322 151 71962
R3	0.4 W metal film resistor	1 MΩ		2322 151 71005
R4	cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

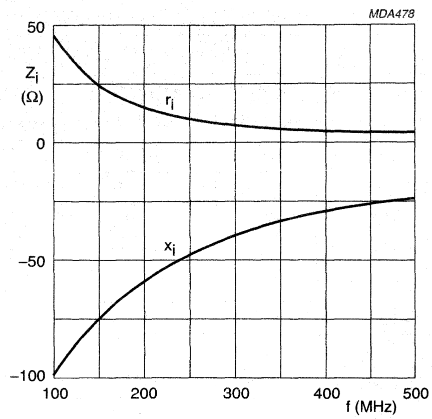
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm.



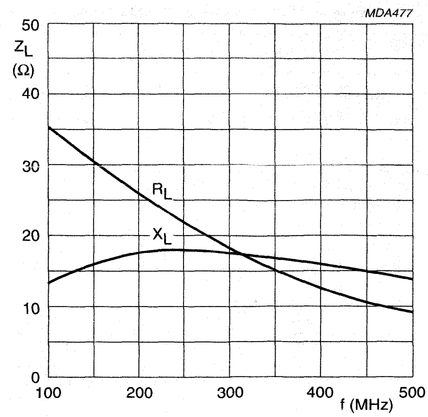
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz test circuit.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA;
R_{GS} = 274 Ω; P_L = 2 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA;
R_{GS} = 274 Ω; P_L = 2 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

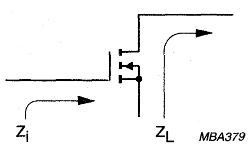
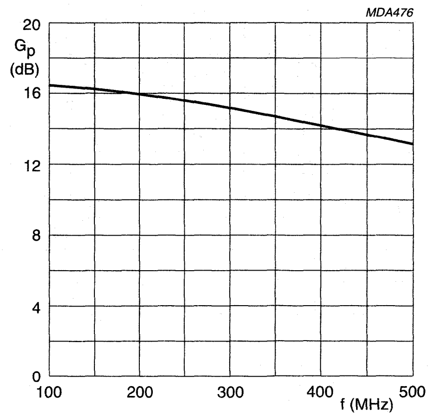


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA;
R_{GS} = 274 Ω; P_L = 2 W.

Fig.16 Power gain as a function of frequency, typical values.

Common emitter S-parameters

Measured at V_{DS} = 12.5 V and I_D = 100 mA.

f (MHz)	S_{11} MAGNITUDE (ratio)	S_{11} ANGLE (deg)	S_{21} MAGNITUDE (ratio)	S_{21} ANGLE (deg)	S_{12} MAGNITUDE (ratio)	S_{12} ANGLE (deg)	S_{22} MAGNITUDE (ratio)	S_{22} ANGLE (deg)
40	0.968	–24.0	10.749	161.5	0.044	72.6	0.900	–27.4
100	0.864	–55.4	9.105	138.3	0.094	51.7	0.828	–62.4
200	0.701	–91.0	6.353	112.7	0.130	29.7	0.735	–100.8
300	0.626	–112.4	4.693	97.0	0.140	17.2	0.693	–122.7
400	0.587	–127.0	3.622	85.6	0.141	9.4	0.678	–136.3
500	0.580	–137.1	2.959	76.5	0.139	4.0	0.675	–145.4
600	0.580	–144.6	2.498	68.8	0.135	0.0	0.675	–152.1
700	0.581	–151.7	2.131	61.4	0.130	–2.5	0.677	–157.5
800	0.588	–157.6	1.874	54.7	0.123	–4.3	0.677	–162.3
900	0.596	–163.5	1.656	48.8	0.115	–4.8	0.683	–166.9
1000	0.605	–168.8	1.473	43.0	0.107	–4.4	0.689	–171.2

Measured at V_{DS} = 12.5 V and I_D = 150 mA.

f (MHz)	S_{11} MAGNITUDE (ratio)	S_{11} ANGLE (deg)	S_{21} MAGNITUDE (ratio)	S_{21} ANGLE (deg)	S_{12} MAGNITUDE (ratio)	S_{12} ANGLE (deg)	S_{22} MAGNITUDE (ratio)	S_{22} ANGLE (deg)
40	0.965	–25.9	11.435	160.6	0.044	72.0	0.876	–29.2
100	0.857	–58.7	9.534	136.8	0.092	50.1	0.804	–65.7
200	0.691	–95.1	6.529	111.3	0.125	28.6	0.715	–104.3
300	0.622	–116.7	4.783	96.0	0.134	16.7	0.678	–125.8
400	0.588	–130.3	3.663	84.8	0.135	9.2	0.666	–138.8
500	0.580	–140.8	2.988	75.9	0.133	4.3	0.665	–147.5
600	0.582	–147.8	2.515	68.4	0.128	0.7	0.666	–154.0
700	0.586	–154.9	2.154	61.2	0.123	–1.3	0.668	–159.1
800	0.588	–160.5	1.897	54.6	0.117	–2.6	0.669	–163.8
900	0.599	–166.3	1.673	48.8	0.111	–2.6	0.675	–168.1
1000	0.609	–171.7	1.493	43.0	0.103	–1.7	0.681	–172.3

Measured at V_{DS} = 12.5 V and I_D = 200 mA.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.965	−26.7	11.660	160.1	0.044	71.4	0.854	−30.4
100	0.851	−60.7	9.625	135.9	0.091	49.4	0.783	−67.7
200	0.688	−97.5	6.524	110.5	0.123	27.9	0.699	−106.5
300	0.623	−118.8	4.751	95.2	0.131	16.4	0.666	−127.6
400	0.590	−132.7	3.644	84.3	0.132	9.2	0.657	−140.3
500	0.585	−142.4	2.968	75.3	0.130	4.3	0.658	−148.7
600	0.583	−150.0	2.495	67.8	0.126	1.0	0.659	−155.0
700	0.589	−156.7	2.137	60.7	0.120	−0.8	0.662	−160.0
800	0.593	−162.2	1.877	54.3	0.114	−1.9	0.664	−164.6
900	0.602	−167.8	1.656	48.4	0.108	−1.7	0.670	−168.9
1000	0.612	−173.0	1.476	42.8	0.100	−0.5	0.677	−173.0

Measured at V_{DS} = 12.5 V and I_D = 250 mA.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.963	−27.3	11.640	159.7	0.045	70.8	0.832	−31.3
100	0.848	−62.0	9.567	135.2	0.092	48.9	0.766	−69.2
200	0.686	−99.3	6.434	109.8	0.123	27.4	0.688	−108.2
300	0.624	−120.3	4.674	94.6	0.130	16.0	0.657	−128.9
400	0.594	−134.2	3.582	83.8	0.130	8.9	0.651	−141.3
500	0.585	−143.9	2.914	74.7	0.128	4.2	0.651	−149.6
600	0.590	−150.8	2.447	67.4	0.124	0.9	0.654	−155.8
700	0.595	−157.6	2.097	60.3	0.119	−0.6	0.658	−160.7
800	0.601	−163.1	1.840	53.8	0.113	−1.7	0.660	−165.2
900	0.607	−168.8	1.625	48.0	0.106	−1.3	0.667	−169.4
1000	0.613	−174.1	1.447	42.2	0.099	−0.1	0.673	−173.3

UHF power MOS transistor BLF542

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the UHF frequency range.

The transistor is encapsulated in a 6-lead, SOT171 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT171

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

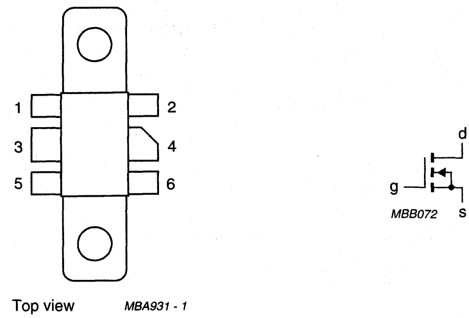


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	500	28	5	> 13	> 50

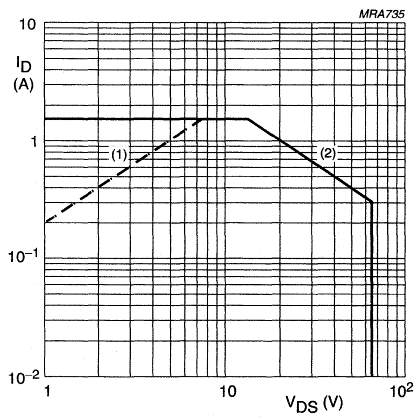
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1.5	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	20	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

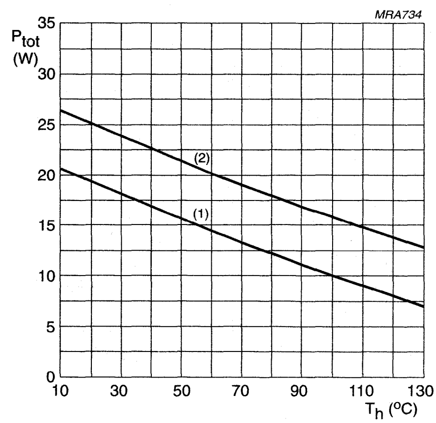
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	8.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



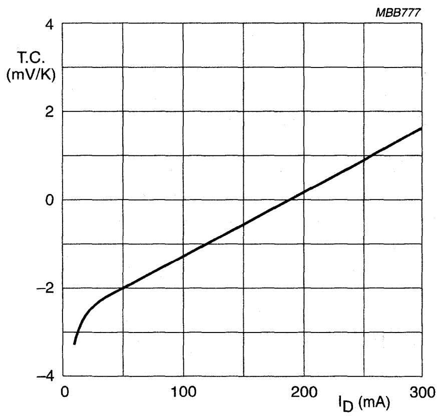
(1) Continuous operation.
(2) Short time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

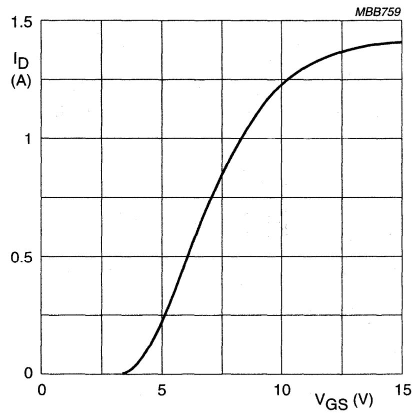
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.1 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	160	240	–	mS
$R_{DS(on)}$	drain-source on-resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.3	5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	1.4	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	14	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	9.4	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	1.7	–	pF



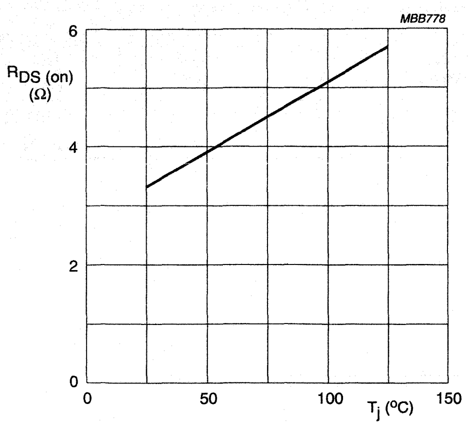
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



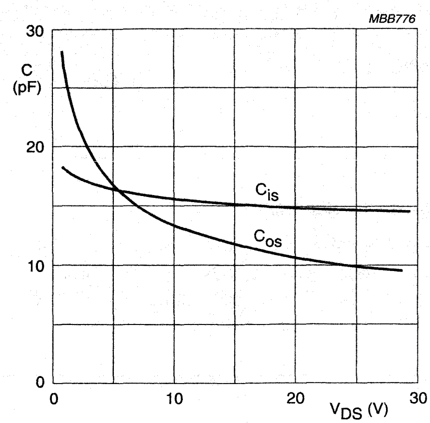
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



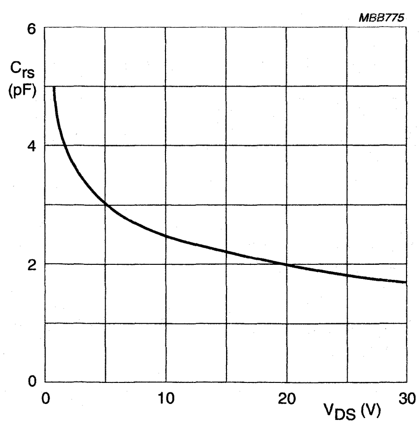
I_D = 0.3 A; V_{GS} = 15 V

Fig.6 Drain-source on-resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

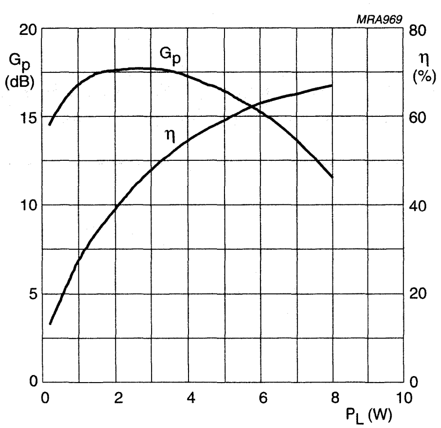
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_{mb} = 25 °C unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	500	28	50	5	> 13 typ. 16.5	> 50 typ. 59

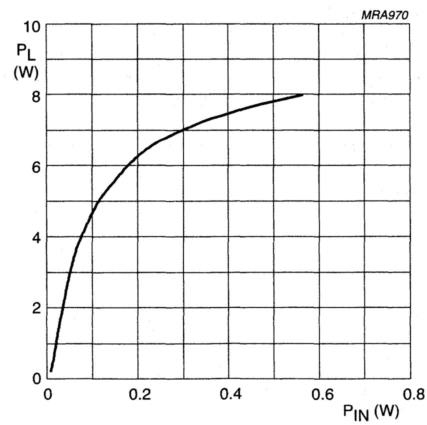
Ruggedness in class-B operation

The BLF542 is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions: V_{DS} = 28 V; f = 500 MHz at rated output power.



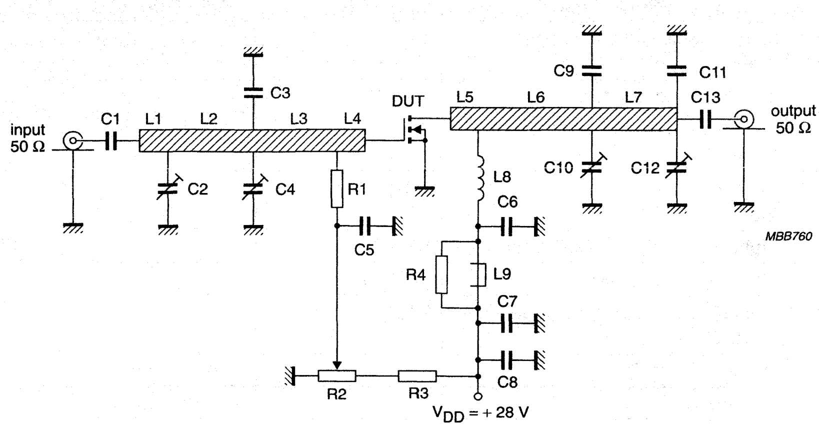
Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA;
Z_L = 9.7 + j24.5 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA;
Z_L = 9.7 + j24.5 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

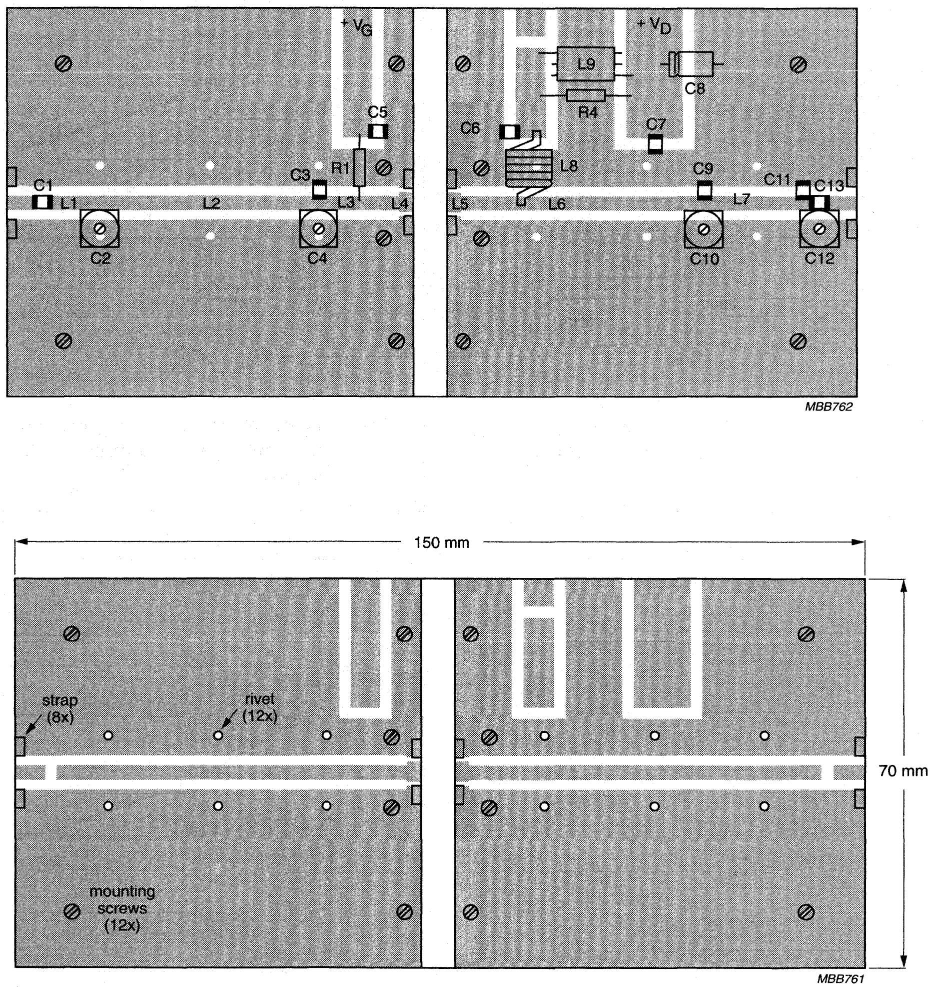
Fig.11 Test circuit for class-B operation.

List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C5, C13	multilayer ceramic chip capacitor (note 1)	390 pF		
C2, C4, C10, C12	film dielectric trimmer	2 to 18 pF		222 809 05217
C3, C9	multilayer ceramic chip capacitor (note 1)	39 pF		
C6	multilayer ceramic chip capacitor (note 2)	220 pF		
C7	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C8	electrolytic capacitor	63 V, 10 μF		2222 030 28109
C11	multilayer ceramic chip capacitor (note 1)	10 pF		
L1	stripline (note 3)	50 Ω	11 mm × 2.5 mm	
L2	stripline (note 3)	50 Ω	37 mm × 2.5 mm	
L3	stripline (note 3)	50 Ω	13 mm × 2.5 mm	
L4, L5	stripline (note 3)	42 Ω	3 mm × 3 mm	
L6	stripline (note 3)	50 Ω	39 mm × 2.5 mm	
L7	stripline (note 3)	50 Ω	22 mm × 2.5 mm	
L8	8 turns 0.8 mm enamelled copper wire	250 nH	length 9 mm int. dia. 6 mm leads 2 × 5 mm	
L9	grade 3B Ferroxcube wideband RF choke			4312 020 36640
R1	metal film resistor	10 kΩ, 0.4 W		2322 151 71003
R2	10 turn potentiometer	50 kΩ		
R3	metal film resistor	205 kΩ, 0.4 W		2322 151 72054
R4	metal film resistor	10 Ω, 0.4 W		2322 151 71009

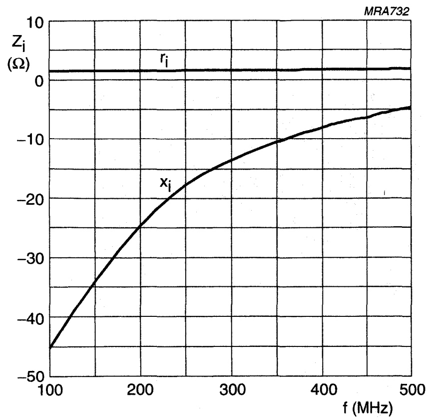
Notes

1. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board with PTFE fibre-glass dielectric (ε_r = 2.2); thickness $^1\!/_{32}$ inch.



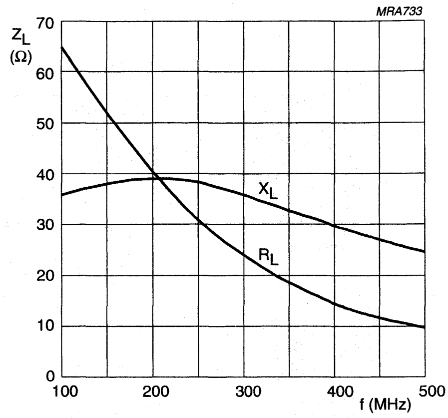
The components are mounted on one side of a copper-clad printed circuit board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by means of fixing screws, hollow rivets and copper foil straps, as shown.

Fig.12 Component layout for 500 MHz test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA;
P_L = 5 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA;
P_L = 5 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

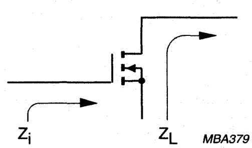
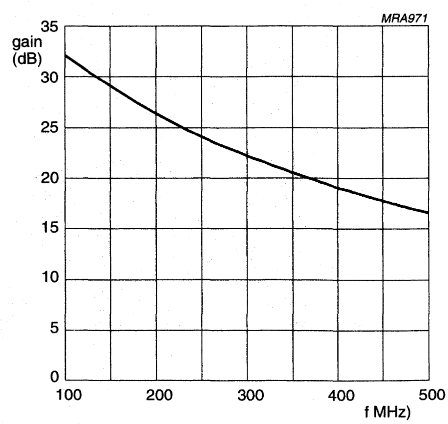


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA;
P_L = 5 W.

Fig.16 Power gain as a function of frequency, typical values.

UHF power MOS transistor BLF543

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 6-lead, SOT171 flange envelope, with a ceramic cap. All leads are isolated from the flange.

The devices are marked with a V_{GS} indication intended for matched pair applications.

PINNING - SOT171

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

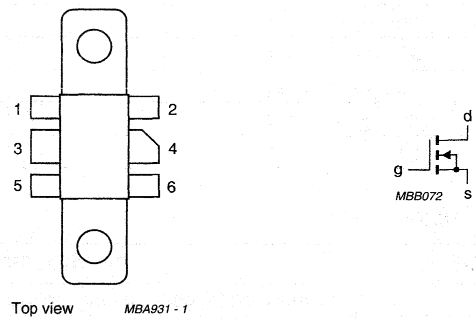


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	10	> 12	> 50
CW, class-B	960	28	10	typ. 8	typ. 50

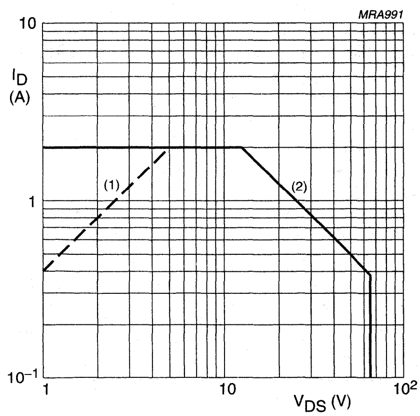
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	2	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	25	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

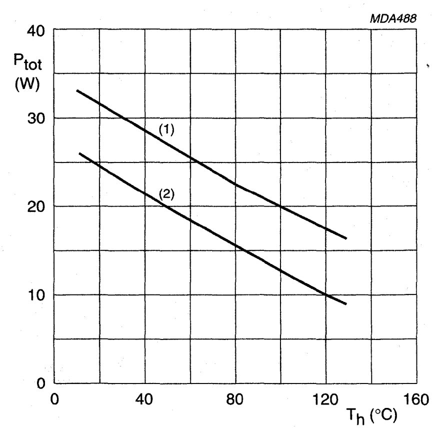
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	7 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



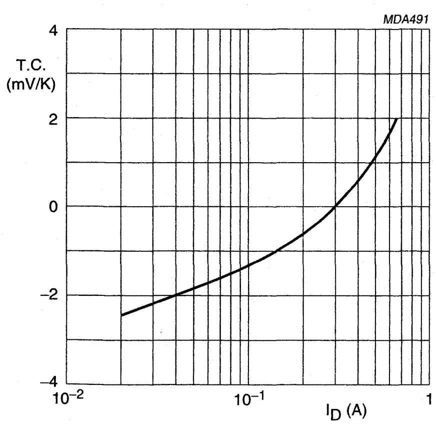
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

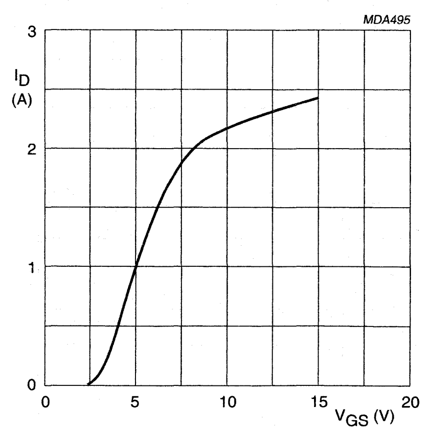
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 20 mA; V_{DS} = 10 V	1	–	4	V
$\Delta V_{GS(th)}$	gate-source voltage difference of matched pairs	I_D = 20 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 0.6 A; V_{DS} = 10 V	300	450	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.6 A; V_{GS} = 10 V	–	1.7	2.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	2.4	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	16	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	12	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	3.2	–	pF



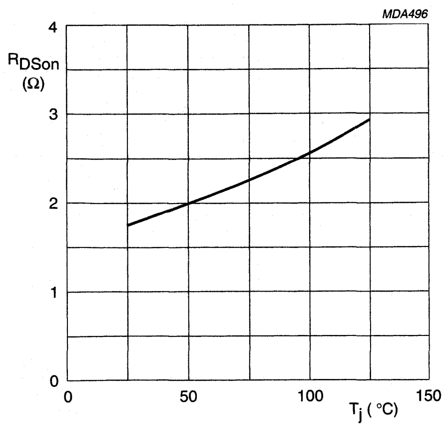
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



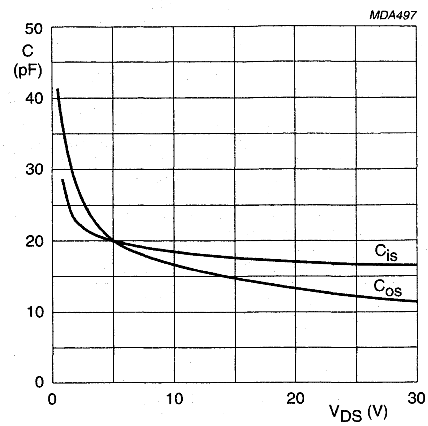
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



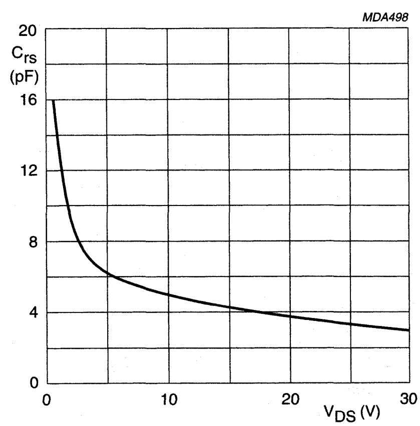
I_D = 0.6 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

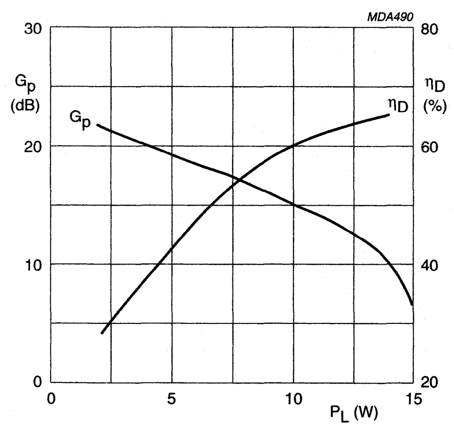
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W, unless otherwise specified.
RF performance in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW class-B	500	28	20	10	> 12 typ. 15	> 50 typ. 60
CW class-B	960	28	20	10	typ. 8	typ. 50
CW class-B	960	24	20	7.5	typ. 8	typ. 50

Ruggedness in class-B operation

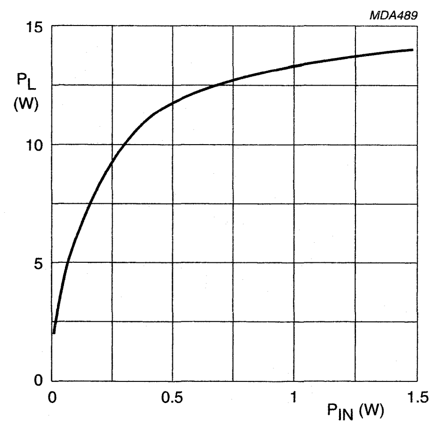
The BLF543 is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA;
Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA;
Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.

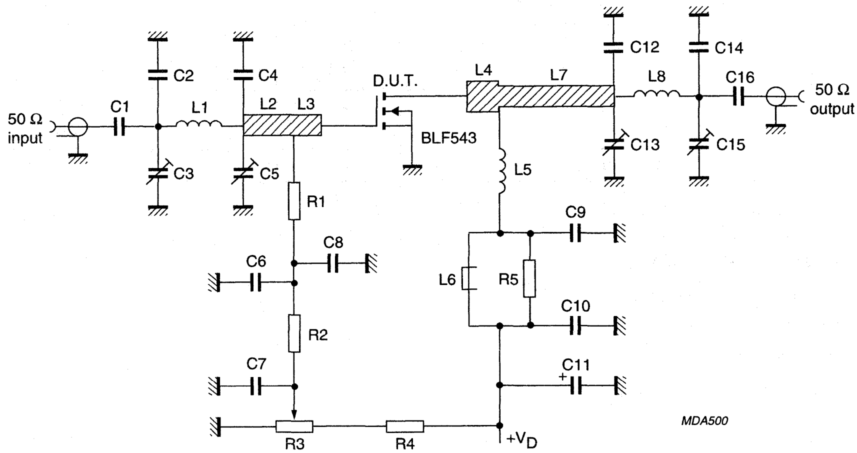


Fig.11 Test circuit for class-B operation at 500 MHz.

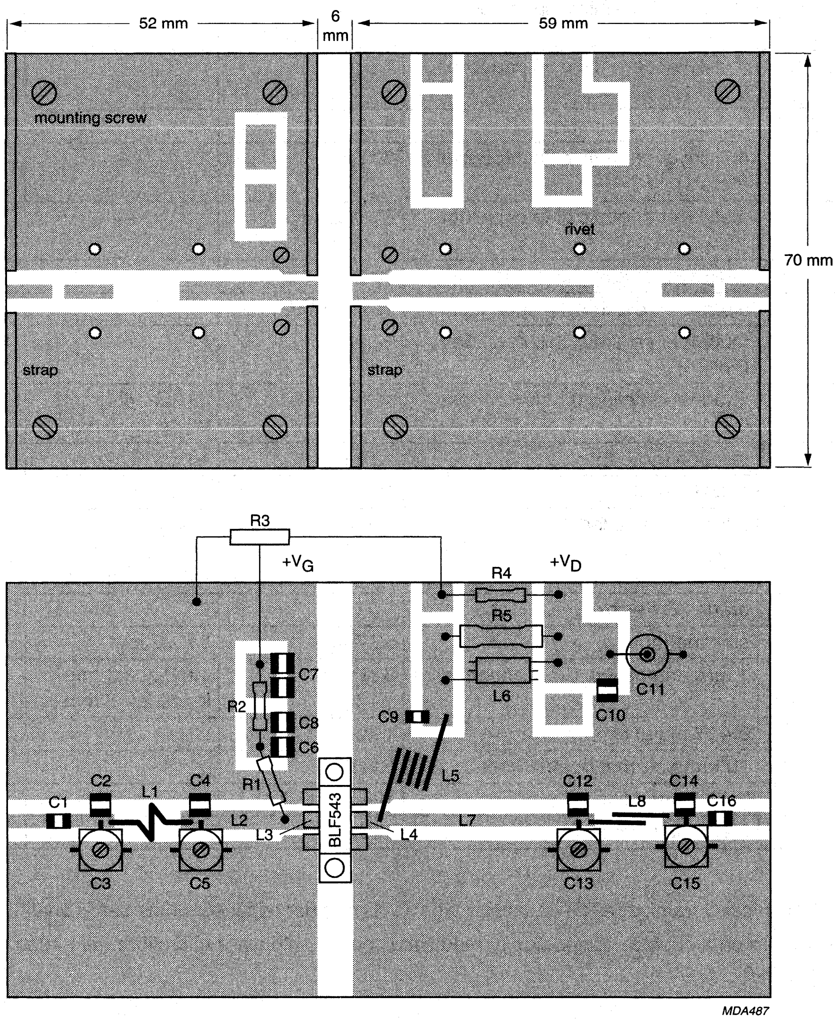
List of components (class-B test circuit at 500 MHz)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C9, C16	multilayer ceramic chip capacitor (note 1)	390 pF		
C2, C14	multilayer ceramic chip capacitor (note 1)	7.5 pF		
C3, C5, C13, C15	film dielectric trimmer	9 pF		2222 809 09002
C4	multilayer ceramic chip capacitor (note 1)	20 pF		
C7	multilayer ceramic chip capacitor	2 × 100 nF in parallel, 50 V		2222 852 47104
C8, C10	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
C12	multilayer ceramic chip capacitor (note 1)	22 pF		
L1	1 turn enamelled 0.8 mm copper wire	11 nH	int. dia. 4.7 mm leads 2 × 5 mm	
L2	stripline (note 2)	42.5 Ω	14.5 × 3 mm	
L3, L4	stripline (note 2)	42.5 Ω	6 × 3 mm	
L5	7 turns enamelled 1 mm copper wire	124 nH	length 7.8 mm int. dia. 4 mm leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
L7	stripline (note 2)	55.7 Ω	31 × 2 mm	
L8	1 turn enamelled 1 mm copper wire	8 nH	int. dia. 3.2 mm leads 2 × 5 mm	
R1, R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	10 turns cermet potentiometer	5 kΩ		
R4	0.4 W metal film resistor	19.6 kΩ		2322 151 71963
R5	1 W metal film resistor	10 Ω		2322 153 51009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness $\frac{1}{32}$ inch.

UHF power MOS transistor BLF543



The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.

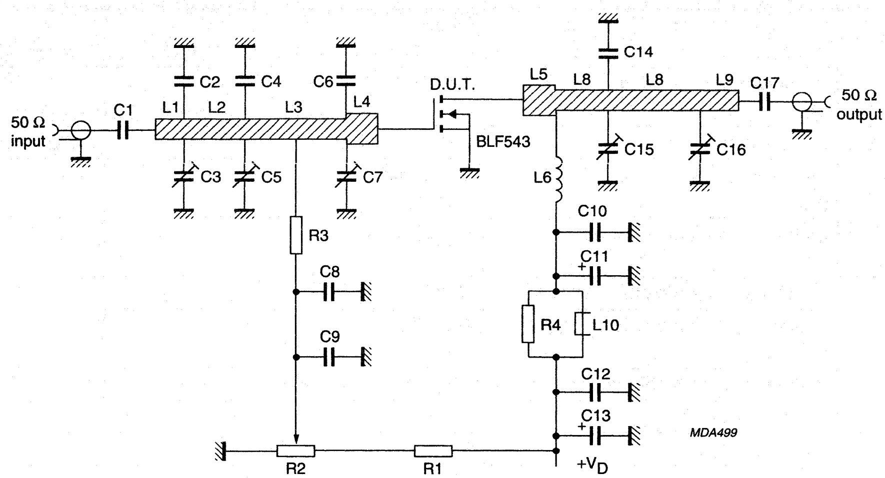


Fig.13 Test circuit for class-B operation at 960 MHz.

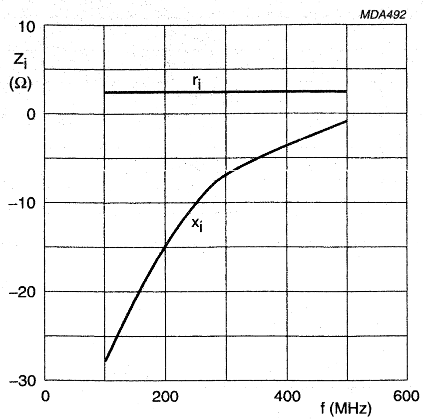
List of components (class-B test circuit at 960 MHz)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C10, C17	multilayer ceramic chip capacitor (note 1)	68 pF		
C2	multilayer ceramic chip capacitor (note 2)	4.7 pF		
C3, C5, C15, C16	film dielectric trimmer	1.2 to 5.5 pF		2222 808 00004
C4	multilayer ceramic chip capacitor (note 2)	2 × 5.6 pF in parallel		
C6, C7	multilayer ceramic chip capacitor (note 2)	7.5 pF		
C9, C12	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C14	multilayer ceramic chip capacitor (note 2)	2 × 4.7 pF in parallel		
C11, C13	aluminum electrolytic capacitor	10 μF, 63 V		2222 030 28109
L1	stripline (note 3)	50 Ω	12.5 × 2.5 mm	
L2	stripline (note 3)	50 Ω	19 × 2.5 mm	
L3	stripline (note 3)	50 Ω	29.5 × 2.5 mm	
L4, L5	stripline (note 3)	42.5 Ω	3 × 3 mm	
L6	3 turns enamelled 0.8 mm copper wire	35 nH	length 4.6 mm int. dia. 4 mm leads 2 × 5 mm	
L7	stripline (note 3)	50 Ω	12.5 × 2.5 mm	
L8	stripline (note 3)	50 Ω	28.5 × 2.5 mm	
L9	stripline (note 3)	50 Ω	20.5 × 2.5 mm	
L10	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.4 W metal film resistor	205 kΩ		2322 151 72054
R2	10 turns potentiometer	50 kΩ		
R3	0.4 W metal film resistor	10 kΩ		2322 151 71003
R4	0.4 W metal film resistor	10 Ω		2322 153 51009

Notes

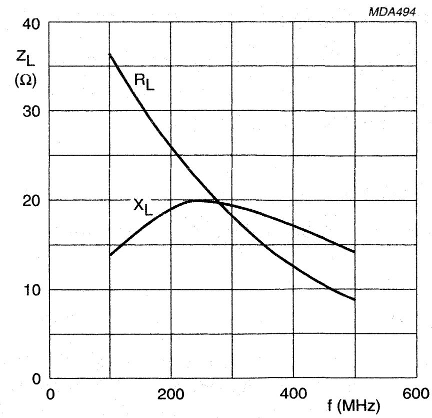
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness $1/32$ inch.

UHF power MOS transistor BLF543



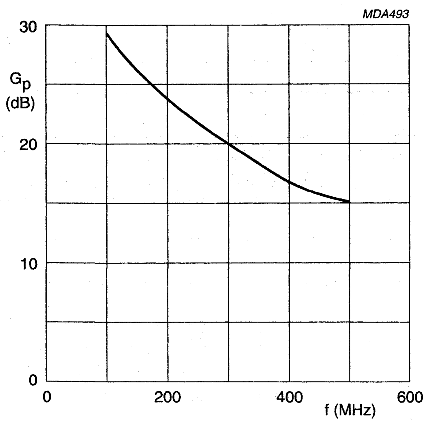
Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA;
P_L = 10 W.

Fig.14 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA;
P_L = 10 W.

Fig.15 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA;
P_L = 10 W.

Fig.16 Power gain as a function of frequency, typical values.

Optimum input and load impedances

Optimum input impedance: 2.3 + j9.5 Ω.
Optimum load impedance: 4.3 + j8.6 Ω.
Conditions: class-B operation; V_{DS} = 24 V;
I_{DQ} = 20 mA; f = 960 MHz; P_L = 7.5 W; typical values.

UHF power MOS transistor BLF544

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

APPLICATIONS

- Communication transmitters in the UHF frequency range.

DESCRIPTION

N-channel enhancement mode vertical D-MOS power transistor encapsulated in a 6-lead, SOT171A flange package with a ceramic cap. All leads are isolated from the flange.
A marking code showing gate-source voltage (V_{GS}) information is provided for matched pair applications.

PINNING - SOT171A

PIN	SYMBOL	DESCRIPTION
1	s	source
2	s	source
3	g	gate
4	d	drain
5	s	source
6	s	source

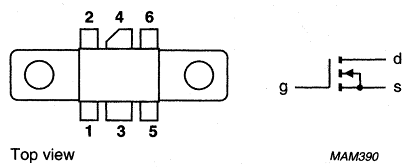


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	20	>11	>50
CW, class-B	960	28	20	typ. 7	typ. 50

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

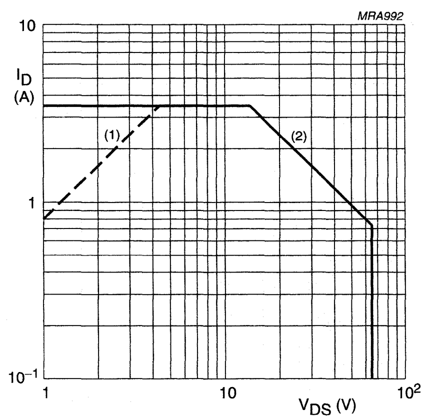
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	3.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	48	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

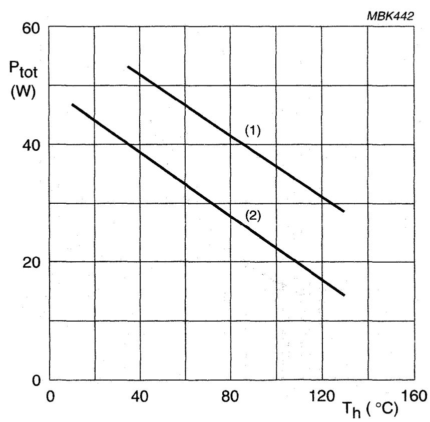
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	3.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



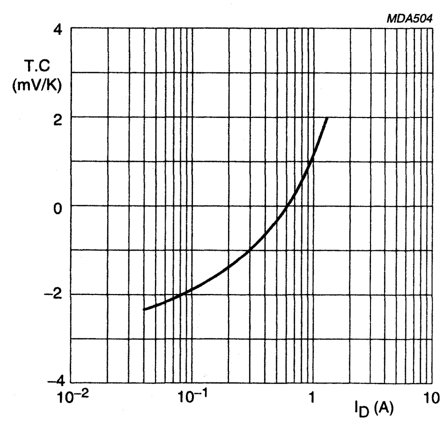
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

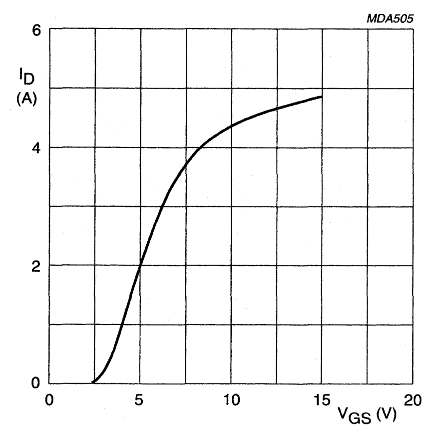
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
ΔV_{GSth}	gate-source voltage difference of matched pairs	I_D = 40 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
R_{DSon}	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF



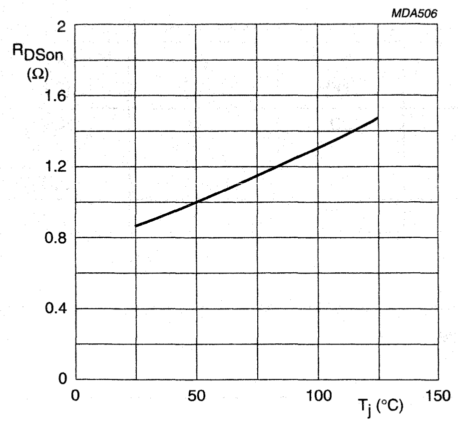
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



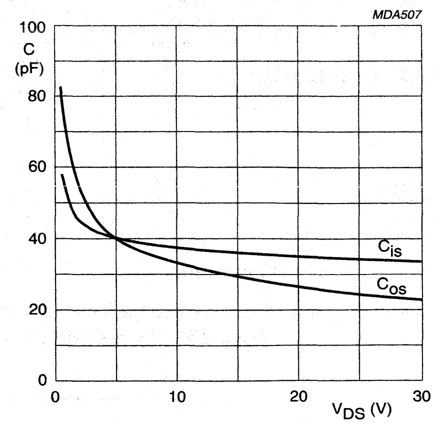
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values.



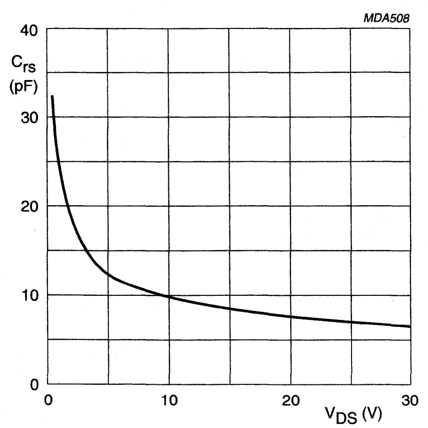
I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

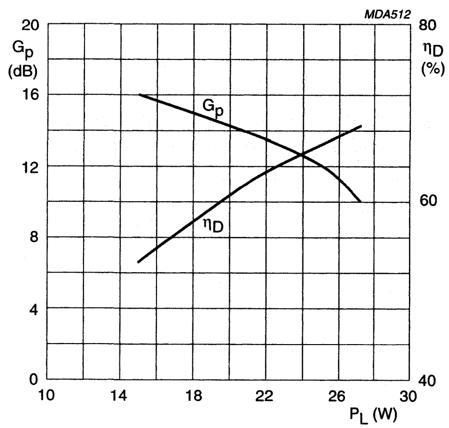
APPLICATION INFORMATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W unless otherwise specified.
RF performance in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	40	20	>11 typ. 14	>50 typ. 60
CW, class-B	960	28	40	20	typ. 7	typ. 50
CW, class-B	960	24	40	15	typ. 7	typ. 50

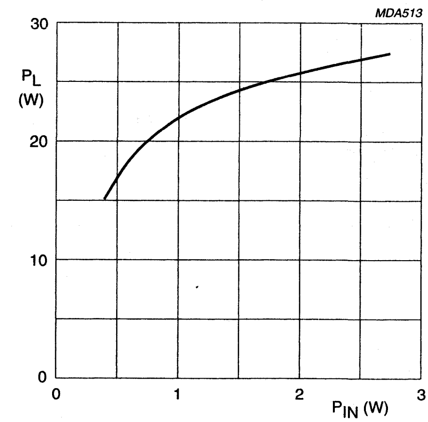
Ruggedness in class-B operation

The BLF544 is capable of withstanding a full load mismatch corresponding to VSWR = 50 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 500 MHz at rated output power.



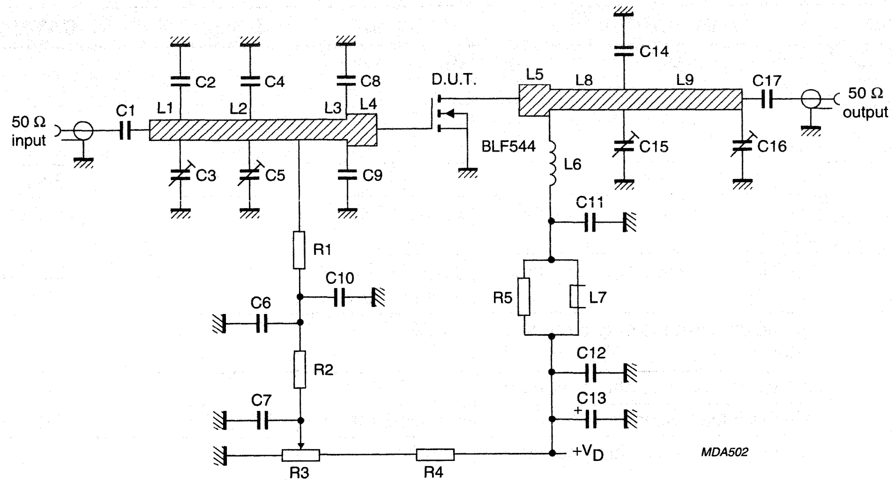
Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
Z_L = 4.3 + j6.3 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power; typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
Z_L = 4.3 + j6.3 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power; typical values.



f = 500 MHz

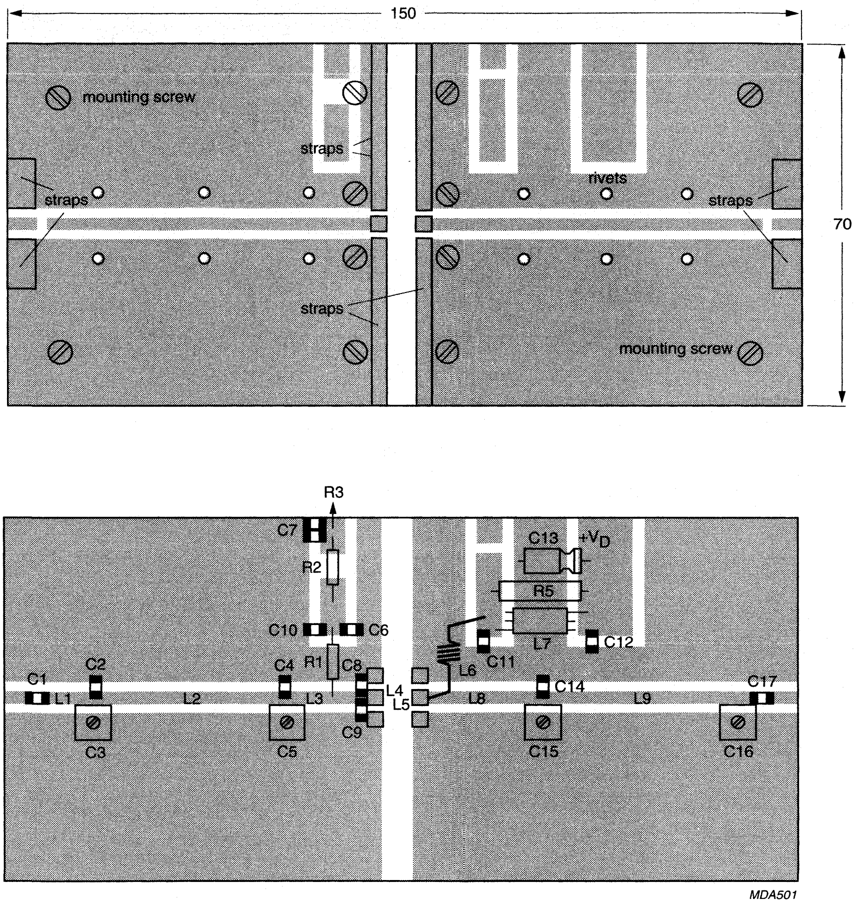
Fig.11 Test circuit for class-B operation.

List of components (see Figs 11 and 12).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C11, C17	multilayer ceramic chip capacitor; note 1	390 pF; 500 V		
C2	multilayer ceramic chip capacitor; note 2	16 pF; 50 V		
C3, C5	film dielectric trimmer	2 to 9 pF		2222 809 09002
C4	multilayer ceramic chip capacitor; note 2	27 pF; 50 V		
C7	multilayer ceramic chip capacitor	2 × 100 nF in parallel; 50 V		2222 852 47104
C8, C9	multilayer ceramic chip capacitor; note 2	39 pF		
C10, C12	multilayer ceramic chip capacitor	100 nF; 50 V		2222 852 47104
C13	electrolytic capacitor	4.7 µF; 63 V		2222 030 38478
C14	multilayer ceramic chip capacitor; note 1	20 pF; 500 V		
C15, C16	film dielectric trimmer	2 to 18 pF		2222 809 09003
L1	stripline note 3	50 Ω	9.5 × 2.5 mm	
L2	stripline note 3	50 Ω	34.5 × 2.5 mm	
L3	stripline note 3	50 Ω	17.5 × 2.5 mm	
L4, L5	stripline note 3	42 Ω	3 × 3 mm	
L6	4 turns enamelled 0.8 mm copper wire	31 nH	length 7.5 mm int. dia. 3 mm leads 2 × 5 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L8	stripline note 3	50 Ω	22 × 2.5 mm	
L9	stripline note 3	50 Ω	39.5 × 2.5 mm	
R1, R2	0.4 W metal film resistor	1 kΩ		2322 151 11002
R3	10 turns cermet potentiometer	50 kΩ		
R4	0.4 W metal film resistor	140 kΩ		2322 151 11404
R5	1 W metal film resistor	10 Ω		2322 153 51009

Notes

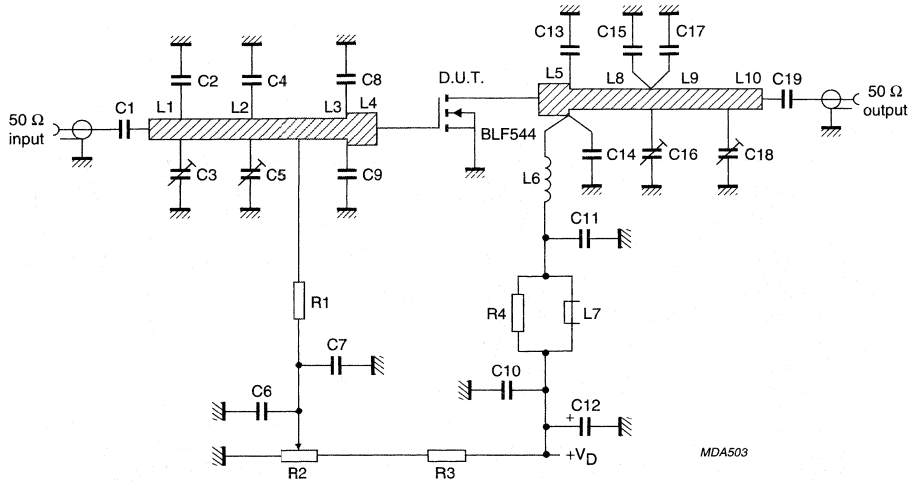
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness $1/32$ inch.



Dimensions in mm.

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



f = 960 MHz.

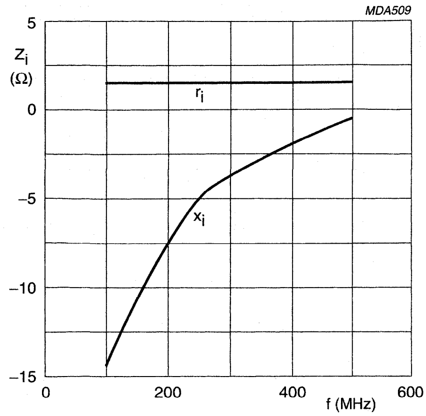
Fig.13 Test circuit for class-B operation.

List of components (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor; note 1	68 pF; 500 V		
C2	multilayer ceramic chip capacitor; note 2	1.6 pF; 50 V		
C3, C5, C16, C18	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C4	multilayer ceramic chip capacitor; note 2	1 pF; 50 V		
C6	multilayer ceramic chip capacitor	10 nF; 50 V		2222 852 47103
C7, C11	multilayer ceramic chip capacitor; note 1	56 μF; 500 V		
C8, C9, C15, C17	multilayer ceramic chip capacitor note 2	6.8 μF; 50 V		
C10	multilayer ceramic chip capacitor	100 nF; 50 V		2222 852 47104
C12	electrolytic capacitor	4.7 μF; 63 V		2222 030 38478
C13	multilayer ceramic chip capacitor; note 2	16 pF; 50 V		
C14	multilayer ceramic chip capacitor; note 2	18 pF; 50 V		
C19	multilayer ceramic chip capacitor; note 1	62 pF; 500 V		
L1, L8	stripline; note 3	50 Ω	6 × 2.5 mm	
L2	stripline; note 3	50 Ω	38 × 2.5 mm	
L3	stripline; note 3	50 Ω	17.5 × 2.5 mm	
L4, L5	stripline; note 3	42 Ω	3 × 3 mm	
L6	2 turns enamelled 1 mm copper wire	16 nH	length 3.4 mm int. dia. 3 mm leads 2 × 5 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L9	stripline; note 3	50 Ω	21 × 2.5 mm	
L10	stripline; note 3	50 Ω	34.5 × 2.5 mm	
R1	0.4 W metal film resistor	15 kΩ		2322 151 11473
R2	10 turns potentiometer	50 kΩ		
R3	0.4 W metal film resistor	140 kΩ		2322 151 11404
R4	0.4 W metal film resistor	10 Ω		2322 153 51009

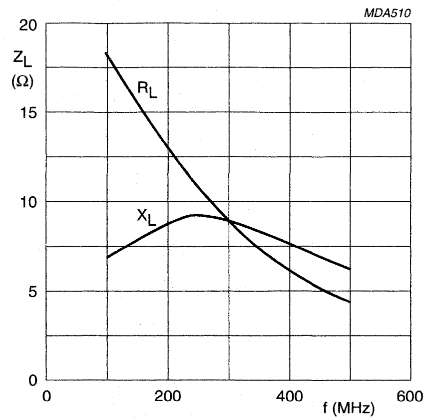
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed-circuit board with glass microfibre reinforced PTFE (ε_r = 2.2); thickness $^1/_{32}$ inch.



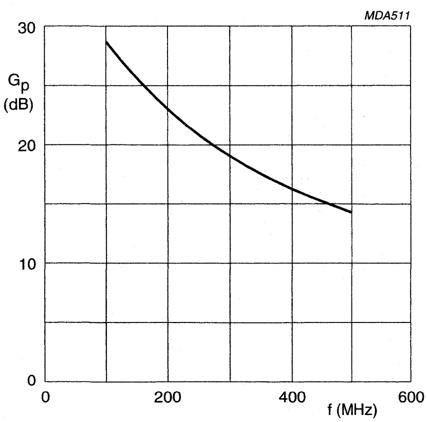
Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA; P_L = 20 W.

Fig.14 Input impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA; P_L = 20 W.

Fig.15 Load impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA; P_L = 20 W.

Fig.16 Power gain as a function of frequency; typical values.

Optimum input and load impedances

Optimum input impedance: 1.2 + j4.8 Ω.
Optimum load impedance: 2.6 − j3.1 Ω.
Conditions: class-B operation; V_{DS} = 24 V;
I_{DQ} = 40 mA; f = 960 MHz; P_L = 15 W; typical values.

UHF push-pull power MOS transistor BLF545

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT268

PIN	DESCRIPTION
1	drain 1
2	gate 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION

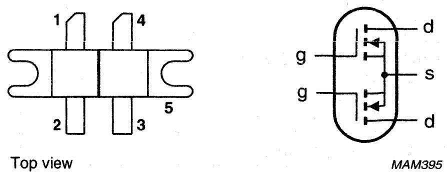


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a push-pull common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	500	28	40	> 11	> 50

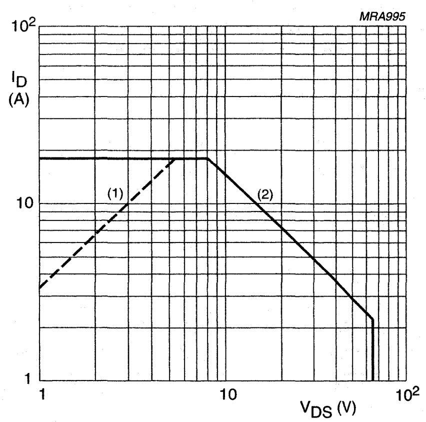
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	3.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	92	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

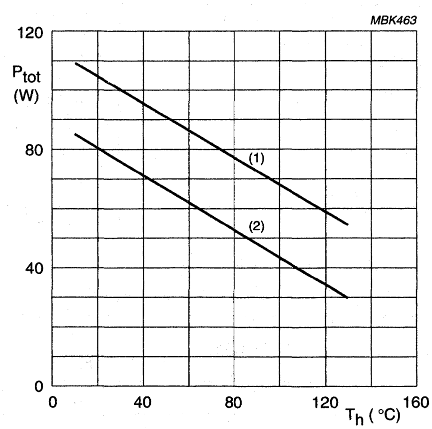
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.9 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



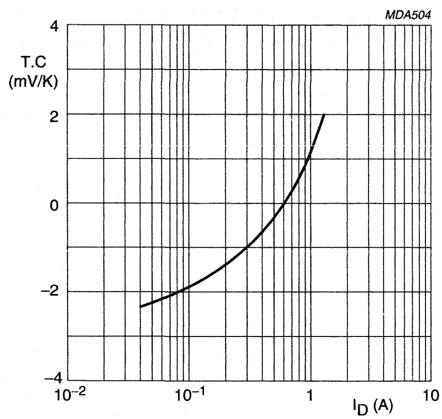
(1) Short-time operation during mismatch.
(2) Continuous operation.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

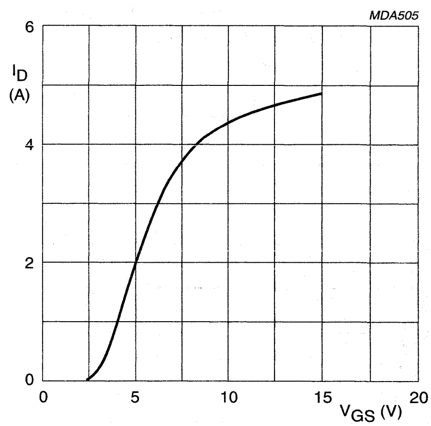
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF



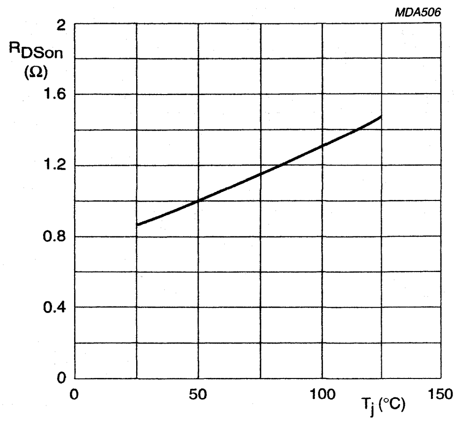
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



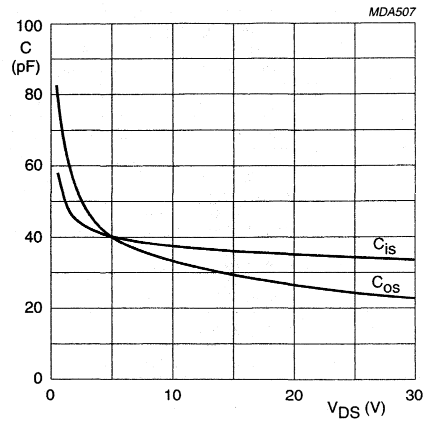
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



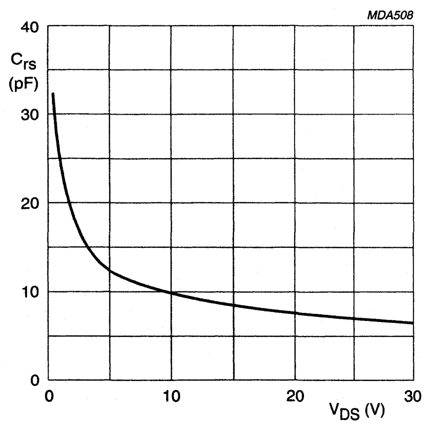
I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

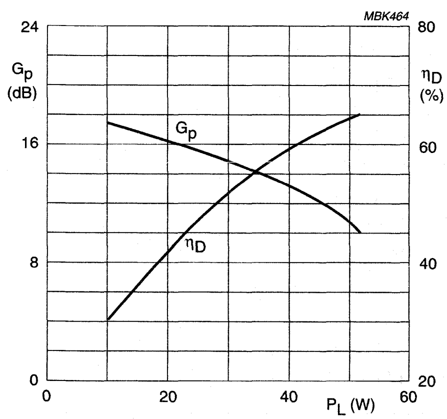
T_h = 25 °C; $R_{th\ mb-h}$ = 0.25 K/W, unless otherwise specified.
RF performance in a common source, class-B, push-pull circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	500	28	2 × 40	40	> 11 typ. 13	> 50 typ. 60

Ruggedness in class-B operation

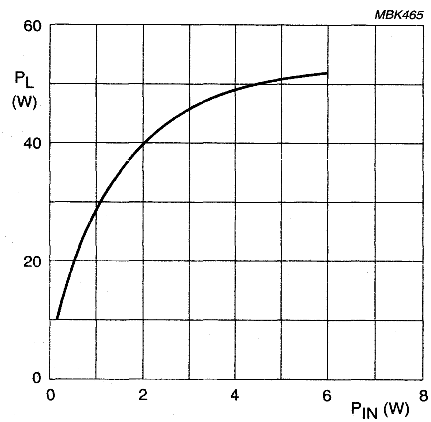
The BLF545 is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



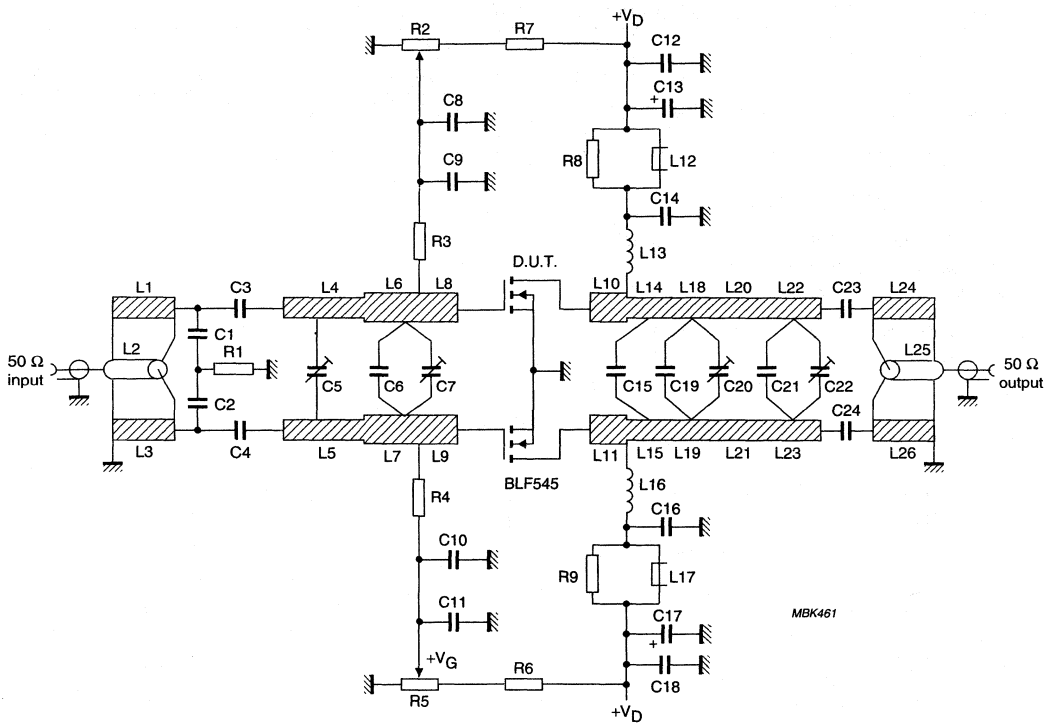
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 40 mA;
Z_L = 4.2 + j6.2 Ω (per section); f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 40 mA;
Z_L = 4.2 + j6.2 Ω (per section); f = 500 MHz.

Fig.10 Load power as a function of input power, typical values per section.



f = 500 MHz.

Fig.11 Test circuit for class-B operation.

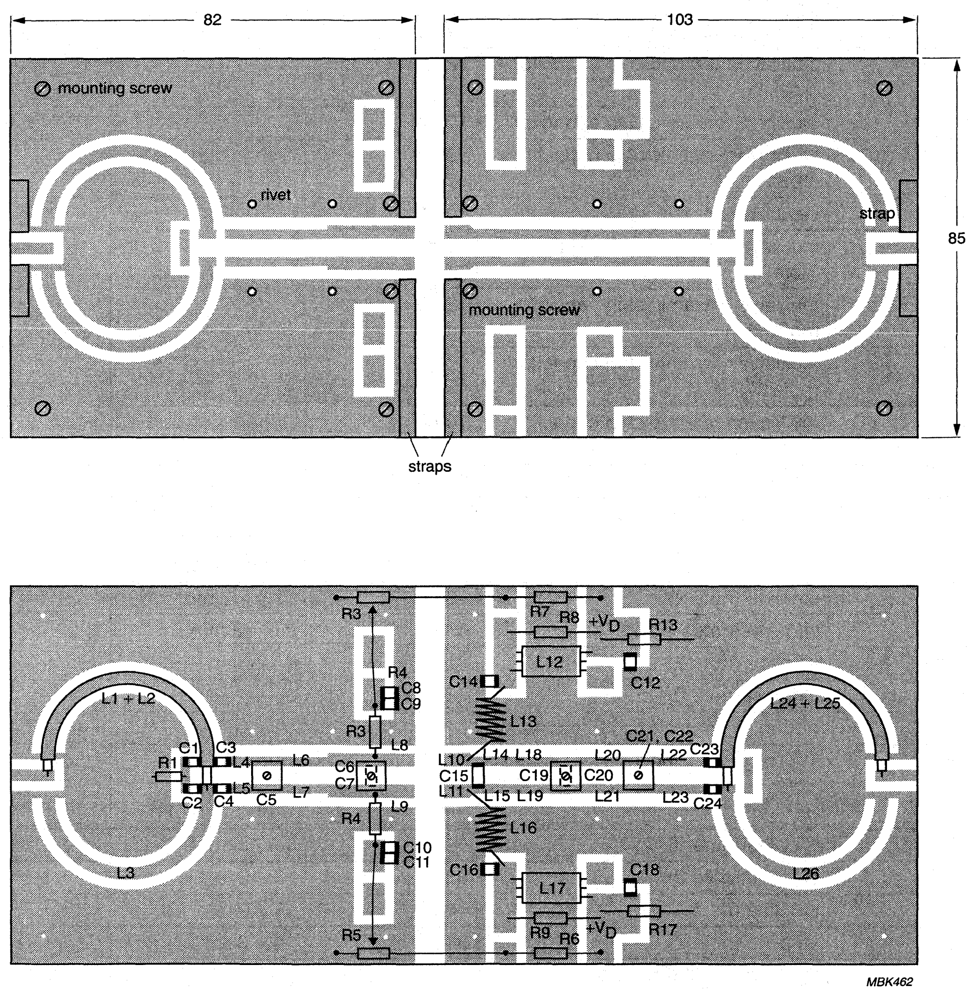
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	5.1 pF		
C3, C4	multilayer ceramic chip capacitor (note 1)	16 pF		
C5, C7, C20, C22	film dielectric trimmer	1.8 to 10 pF		2222 809 05002
C6	multilayer ceramic chip capacitor (note 1)	22 pF		
C8, C11, C12, C18	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9, C10, C14, C16	multilayer ceramic chip capacitor (note 1)	390 pF		
C13, C17	electrolytic capacitor	10 μF, 63 V		
C15	multilayer ceramic chip capacitor (note 1)	18 pF		
C19	multilayer ceramic chip capacitor (note 1)	13 pF		
C21	multilayer ceramic chip capacitor (note 1)	6.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	10 pF		
L1, L3, L24, L26	stripline (note 2)	50 Ω	56 × 2.4 mm	
L2, L25	semi-rigid cable (note 3)	50 Ω	ext. dia. 2.2 mm ext. conductor length 56 mm	
L4, L5	stripline (note 2)	56 Ω	13.4 × 2 mm	
L6, L7	stripline (notes 2 and 4)	56 Ω	9.6 × 2 mm	
L8, L9	stripline (note 2)	42 Ω	9 × 3 mm	
L10, L11	stripline (note 2)	42 Ω	6 × 3 mm	
L12, L17	grade 3B Ferroxcube RF choke			4312 020 36642
L13, L16	4 turns enamelled 1.2 mm copper wire	62 nH	length 7.6 mm int. dia. 5 mm leads 2 × 5 mm	
L14, L15	stripline (note 2)	56 Ω	8 × 2 mm	
L18, L19	stripline (note 2)	56 Ω	13 × 2 mm	
L20, L21	stripline (note 2)	56 Ω	18 × 2 mm	
L22, L23	stripline (note 2)	56 Ω	14 × 2 mm	
R1	0.4 W metal film resistor	5.11 Ω		2322 151 75118
R2, R5	10 turns cermet potentiometer	50 kΩ		
R3, R4	0.4 W metal film resistor	10 kΩ		2322 151 71003
R6, R7	0.4 W metal film resistor	205 kΩ		2322 151 72054
R8, R9	1 W metal film resistor	10 Ω		2322 151 71009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.

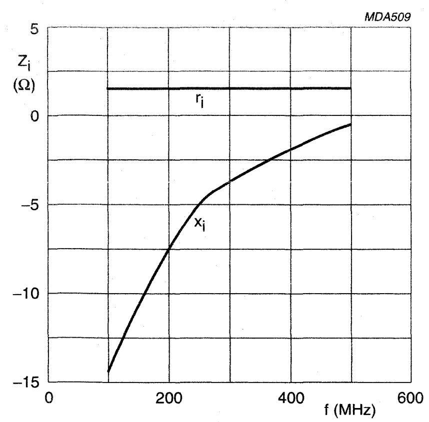
2. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE (ε_r = 2.2); thickness $^1/_{32}$ inch.
3. Semi-rigid cables L2 and L25 are soldered on to striplines L1 and L26.
4. Striplines L6 and L7 are used in series with a 42 Ω stripline (11 × 3 mm).



The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

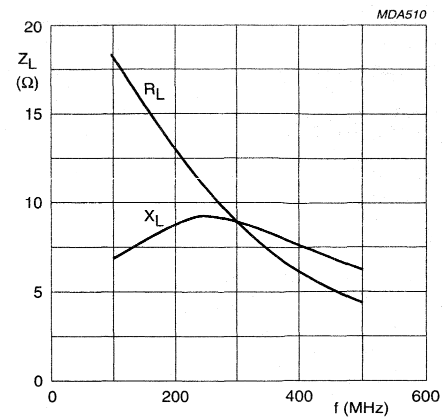
Dimensions in mm.

Fig.12 Component layout for 500 MHz class-B test circuit.



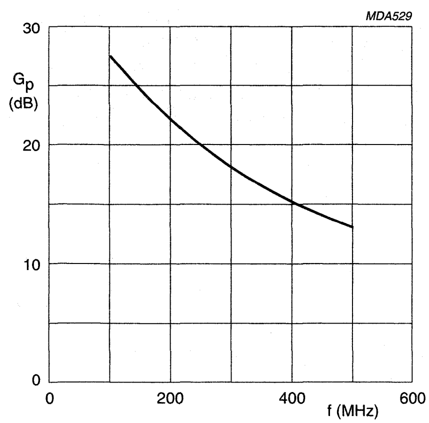
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 40 mA;
P_L = 40 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 40 mA;
P_L = 40 W.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 40 mA;
P_L = 40 W.

Fig.15 Power gain as a function of frequency, typical values per section.

UHF push-pull power MOS transistor BLF546

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT268

PIN	DESCRIPTION
1	drain 1
2	gate 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION

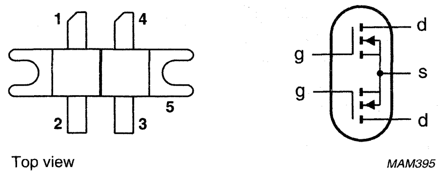


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	80	> 11	> 50

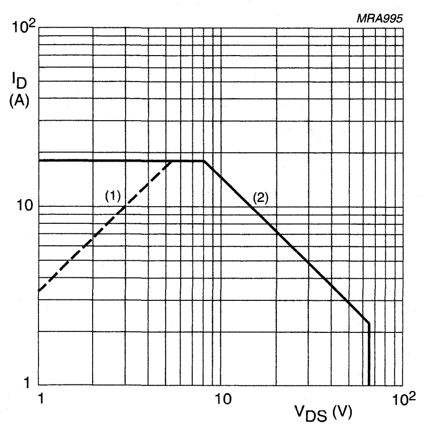
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	9	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	145	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

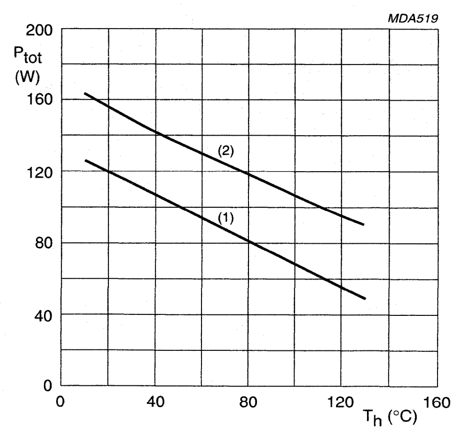
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.2 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



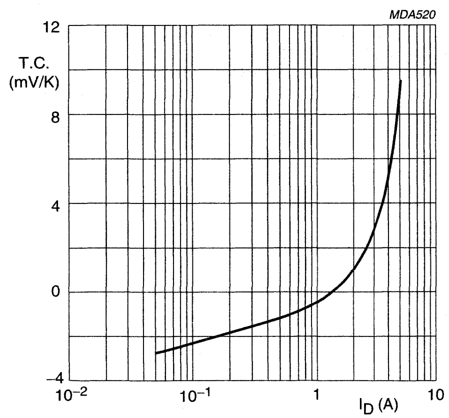
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

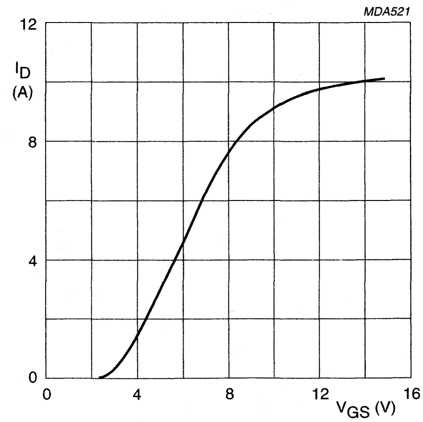
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 20 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 80 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 2.4 A; V_{DS} = 10 V	1.2	1.7	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 2.4 A; V_{GS} = 10 V	–	0.4	0.6	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	46	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	15	–	pF



V_{DS} = 10 V.

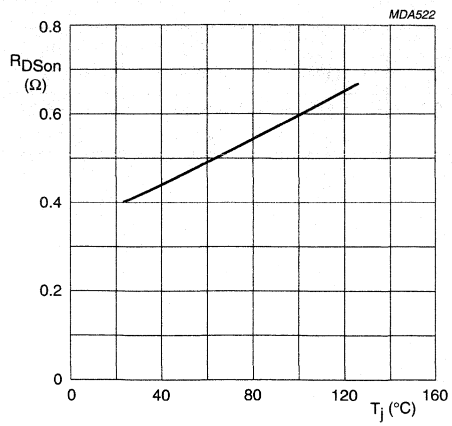
Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



V_{DS} = 10 V; T_j = 25 °C.

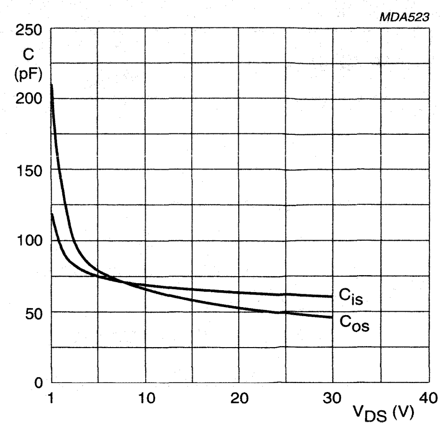
Fig.5 Drain current as a function of gate-source voltage, typical values per section.

UHF push-pull power MOS transistor BLF546



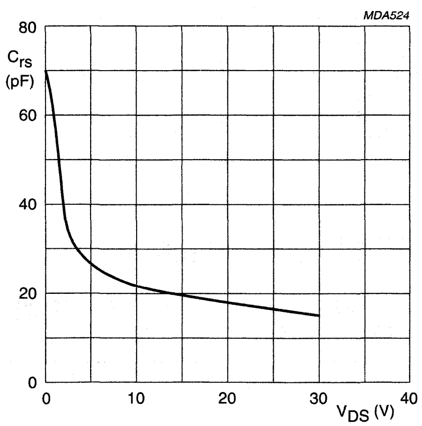
I_D = 2.4 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

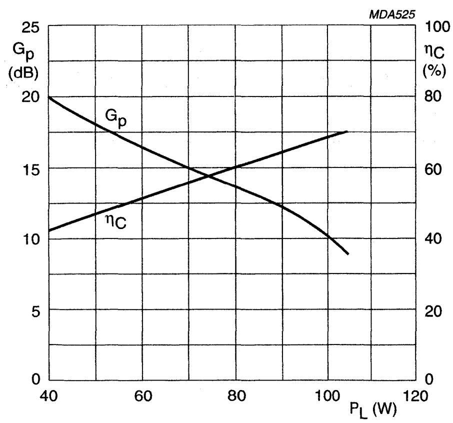
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.25 K/W, unless otherwise specified.
RF performance in a common source, class-B, push-pull circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 × 80	80	> 11 typ. 13	> 50 typ. 60

Ruggedness in class-B operation

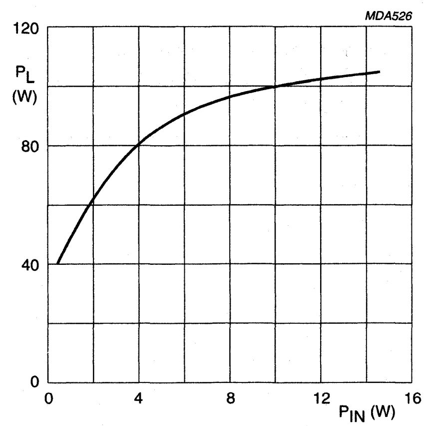
The BLF546 is capable of withstanding a full load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 80 mA;
Z_L = 2.3 + j2.7 Ω (per section); f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 80 mA;
Z_L = 2.3 + j2.7 Ω (per section); f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.

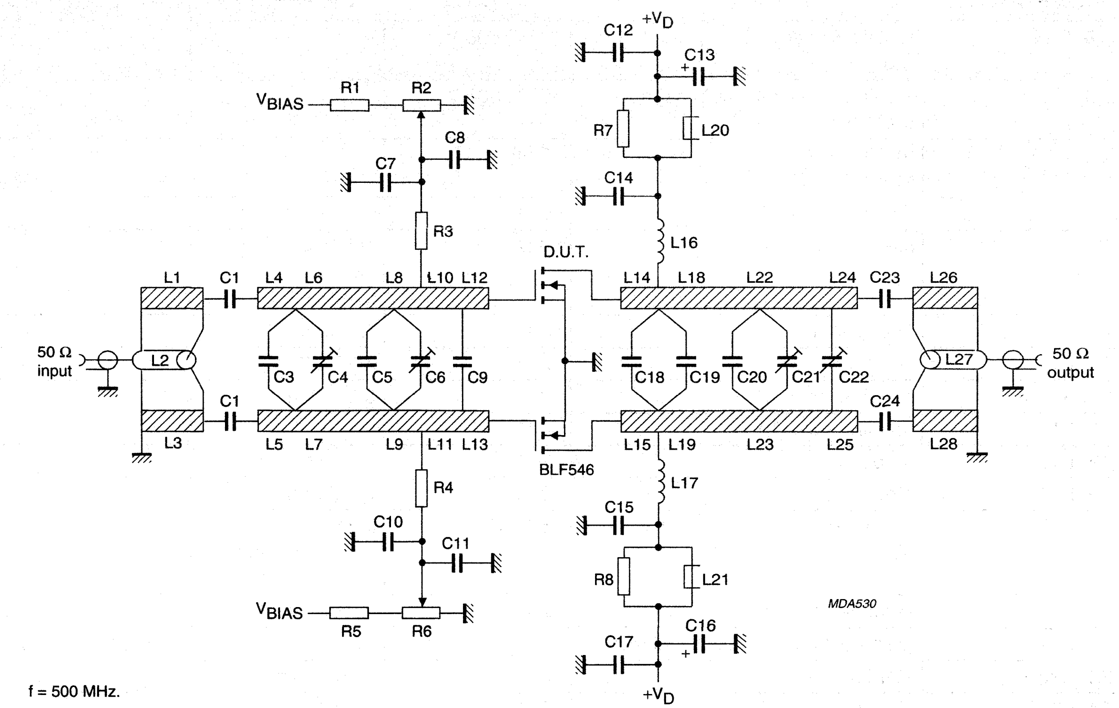


Fig.11 Test circuit for class-B operation.

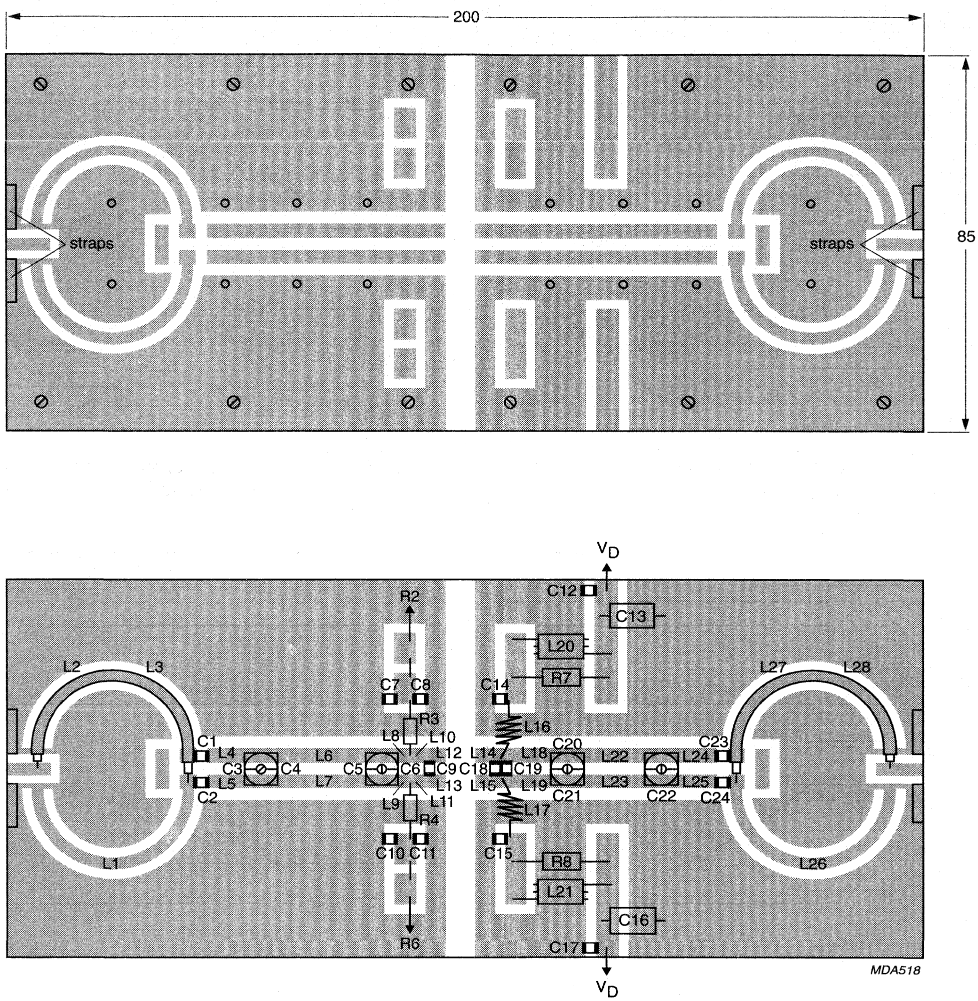
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	33 pF, 500 V		
C3	multilayer ceramic chip capacitor (note 1)	11 pF, 500 V		
C4, C6, C21, C22	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 2)	12 pF, 500 V		
C7, C10, C14, C15	multilayer ceramic chip capacitor (note 1)	390 pF, 500 V		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C9	multilayer ceramic chip capacitor (note 2)	39 pF, 500 V		
C13, C16	electrolytic capacitor	4.7 μF, 63 V		2222 030 38478

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C18, C19	multilayer ceramic chip capacitor (note 2)	18 pF, 500 V		
C20	multilayer ceramic chip capacitor (note 2)	15 pF, 500 V		
C23, C24	multilayer ceramic chip capacitor (note 1)	15 pF, 500 V		
L1, L3, L26, L28	stripline (note 3)	50 Ω	55.6 × 2.4 mm	
L2	semi-rigid cable (note 4)	50 Ω	ext. dia. 2 mm ext. conductor length 55.6 mm	
L4, L5	stripline (note 3)	42 Ω	12 × 3 mm	
L6, L7	stripline (note 3)	42 Ω	26.5 × 3 mm	
L8, L9	stripline (note 3)	42 Ω	5.5 × 3 mm	
L10, L11	stripline (note 3)	42 Ω	6 × 3 mm	
L12, L13	stripline (note 3)	42 Ω	3 × 3 mm	
L14, L15	stripline (note 3)	42 Ω	7 × 3 mm	
L16, L17	3 turns enamelled 1 mm copper wire	15.6 nH	length 8.5 mm int. dia. 5.4 mm leads 2 × 5 mm	
L18, L19	stripline (note 3)	42 Ω	12 × 3 mm	
L20, L21	grade 3B Ferroxcube RF choke			4312 020 36642
L22, L23	stripline (note 3)	42 Ω	20 × 3 mm	
L24, L25	stripline (note 3)	42 Ω	14 × 3 mm	
L27	semi-rigid cable (note 5)	50 Ω	ext. dia. 2 mm ext. conductor length 55.6 mm	
R1, R5	0.4 W metal film resistor	11.5 kΩ		2322 151 71153
R2, R6	10 turns cermet potentiometer	50 kΩ		
R3, R4	0.4 W metal film resistor	10 kΩ		2322 151 71003
R7, R8	1 W metal film resistor	10 Ω		2322 153 51009

Notes

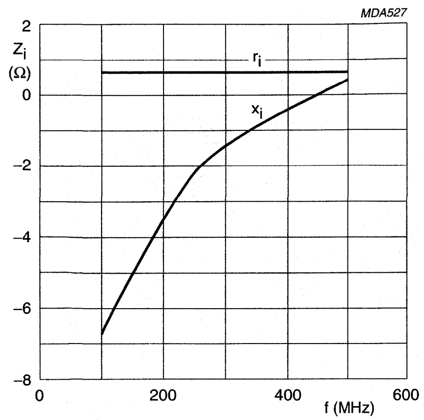
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness $\frac{1}{32}$ inch.
4. Semi-rigid cable L2 is soldered on to stripline L3.
5. Semi-rigid cable L27 is soldered on to stripline L28.



The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

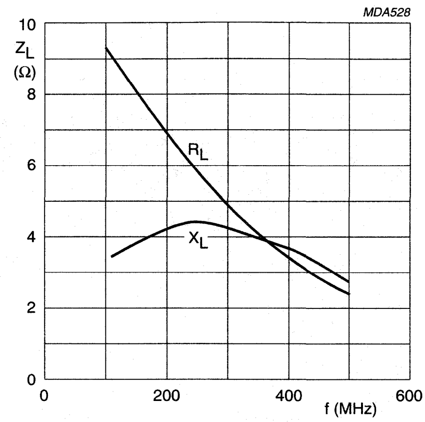
Dimensions in mm.

Fig.12 Component layout for 500 MHz test circuit.



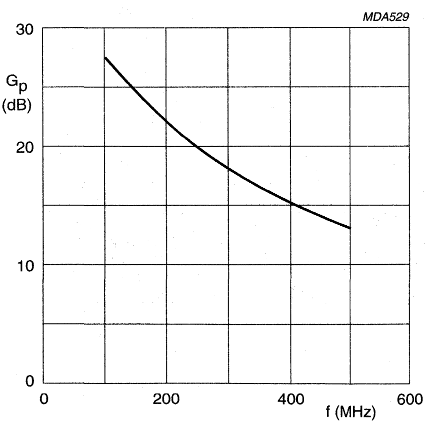
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 80 mA; P_L = 80 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 80 mA; P_L = 80 W.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 80 mA; P_L = 80 W.

Fig.15 Power gain as a function of frequency, typical values per section.

UHF push-pull power MOS transistor BLF547

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A2

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

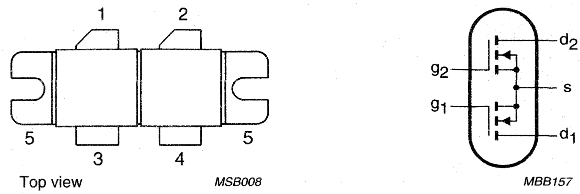


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common-source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	500	28	100	> 10	> 50

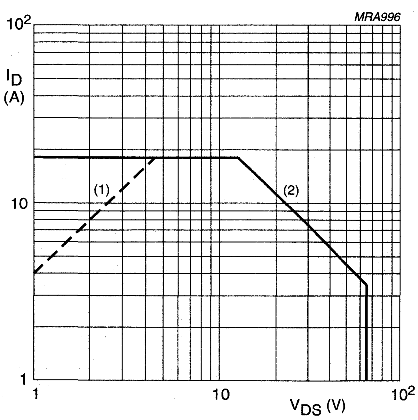
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	9	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	225	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

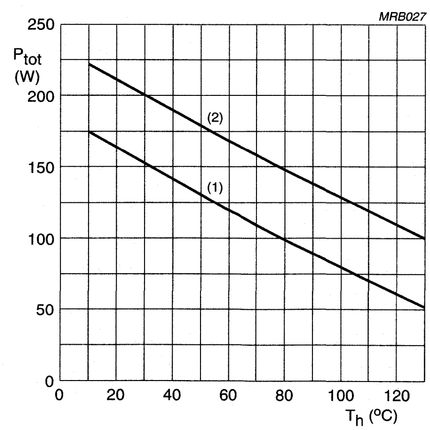
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 225 W total device; both sections equally loaded	max. 0.78 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	max. 0.15 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C;
Total device; both sections equally loaded.

Fig.2 DC SOAR.



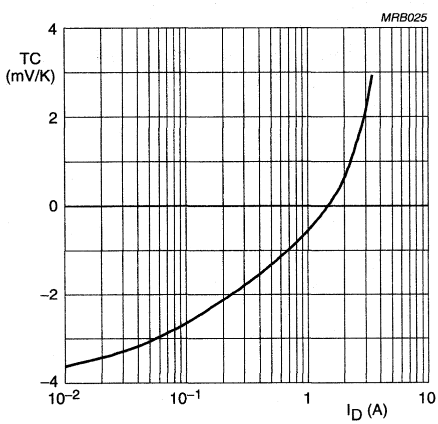
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

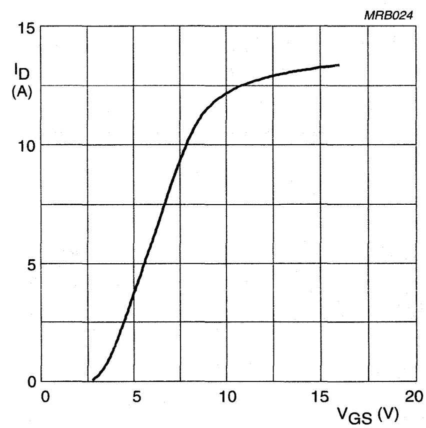
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 25 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 100 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 3 A; V_{DS} = 10 V	1.5	2.1	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 3 A; V_{GS} = 10 V	–	0.4	0.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	10	13	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	77	85	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	62	70	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	18	21	pF



V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.

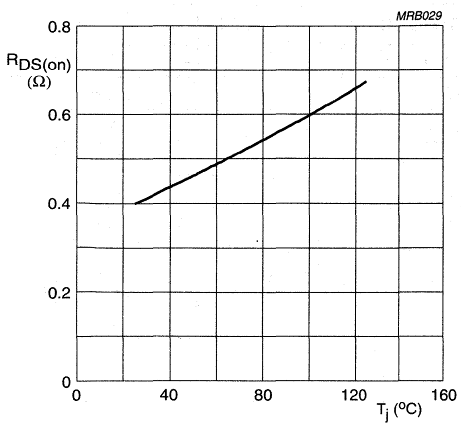


V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.

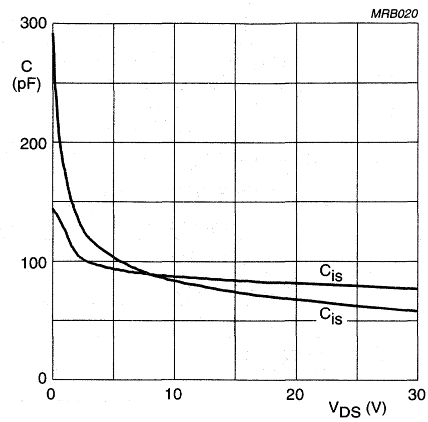
UHF push-pull power MOS transistor

BLF547



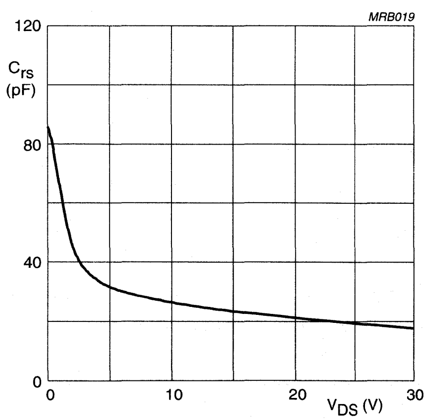
I_D = 3 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

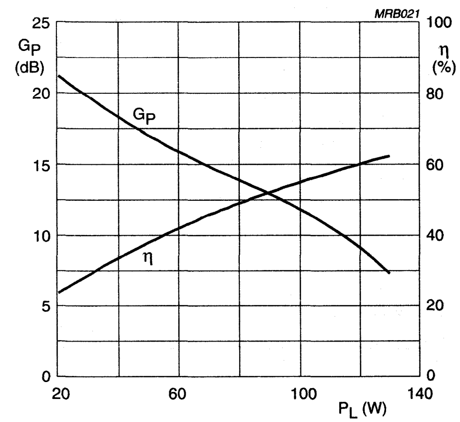
T_h = 25 °C; $R_{th\ mb-h}$ = 0.15 K/W, unless otherwise specified.
RF performance in a common source, push-pull, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	500	28	2 × 100	100	> 10 typ. 12	> 50 typ. 55

Ruggedness in class-B operation

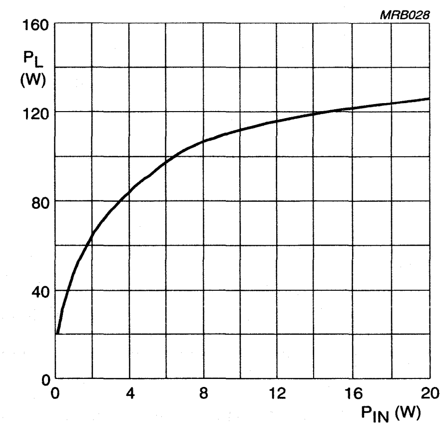
The BLF547 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 100 mA;
f = 500 MHz; Z_L = 1.5 + j1.8 Ω (per section).

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 100 mA;
f = 500 MHz; Z_L = 1.5 + j1.8 Ω (per section).

Fig.10 Load power as a function of input power, typical values.

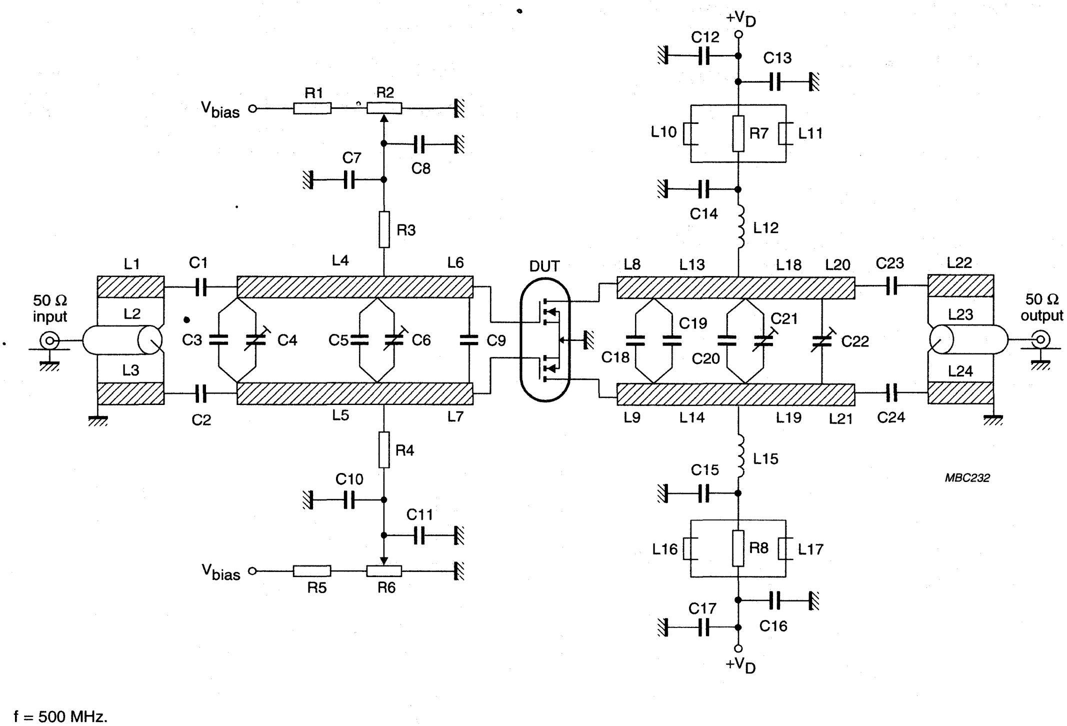


Fig.11 Test circuit for class-B operation.

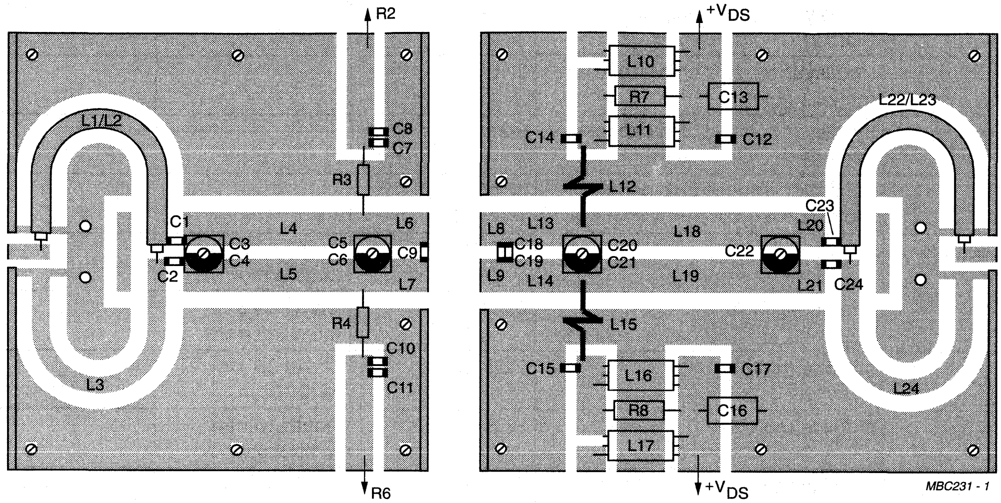
List of components (see class-B test circuit)

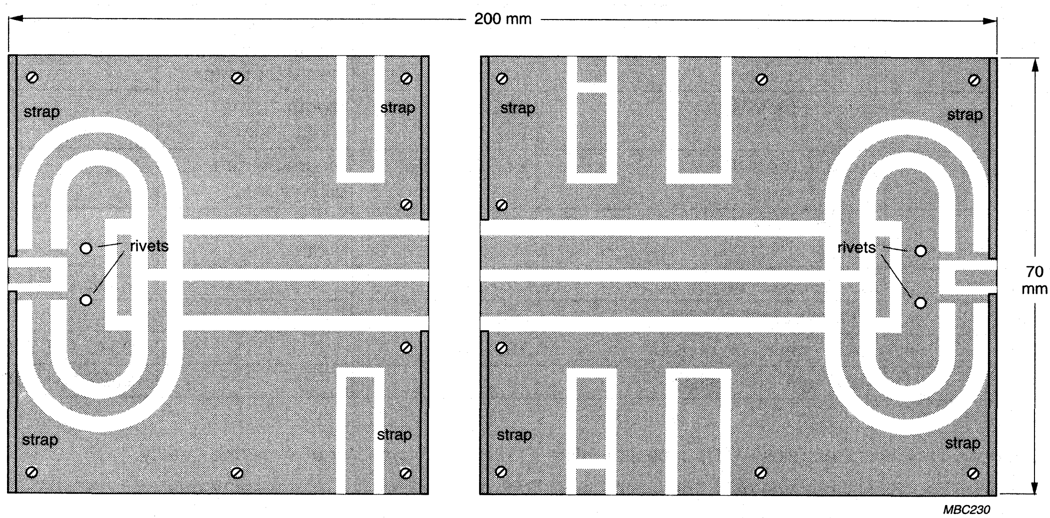
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	15 pF		
C3	multilayer ceramic chip capacitor (note 1)	16 pF		
C4	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 2)	15 pF		
C6, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7, C10, C14, C15	multilayer ceramic chip capacitor (note 1)	390 pF		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9	multilayer ceramic chip capacitor (note 3)	2 × 68 pF in series		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C13, C16	electrolytic capacitor	10 μF, 63 V		2222 030 28109
C18	multilayer ceramic chip capacitor (note 2)	10 pF		
C19	multilayer ceramic chip capacitor (note 2)	27 pF		
C20	multilayer ceramic chip capacitor (note 2)	8.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	30 pF		
L1, L3, L22, L24	stripline (note 4)	34.5 Ω	length 66.5 mm width 4 mm	
L2, L23	semi-rigid cable	50 Ω	length 66.5 mm width 3.6 mm	
L4, L5	stripline (note 4)	22.3 Ω	length 35 mm width 7 mm	
L6, L7	stripline (note 4)	22.3 Ω	length 10 mm width 7 mm	
L8, L9	stripline (note 4)	22.3 Ω	length 5.5 mm width 7 mm	
L10, L11, L16, L17	grade 3B Ferroxcube RF choke			4312 020 36640
L12, L15	1 turn enamelled 1.5 mm copper wire	17 nH	length 5 mm int. dia. 9 mm leads 2 × 5 mm	
L13, L14	stripline (note 4)	22.3 Ω	length 15 mm width 7 mm	
L18, L19	stripline (note 4)	22.3 Ω	length 36 mm width 7 mm	
L20, L21	stripline (note 4)	22.3 Ω	length 8.5 mm width 7 mm	
R1, R5	0.4 W metal film resistor	24.7 kΩ		2322 151 72473
R2, R6	10 turn potentiometer	5 kΩ		
R3, R4	0.4 W metal film resistor	10.5 kΩ		2322 151 71053
R7, R8	1 W metal film resistor	10 Ω		2322 151 71009

Notes

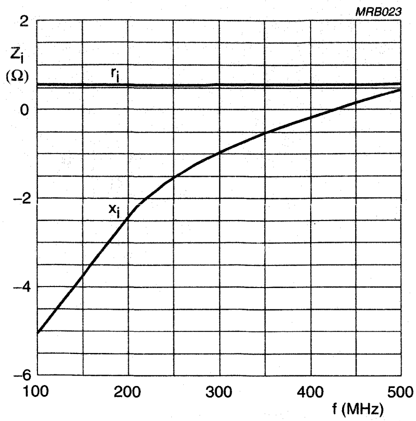
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
4. The striplines are on a double copper-clad printed circuit board, with PTFE fiber-glass dielectric ($\varepsilon_r = 2.2$), thickness 0.79 mm.





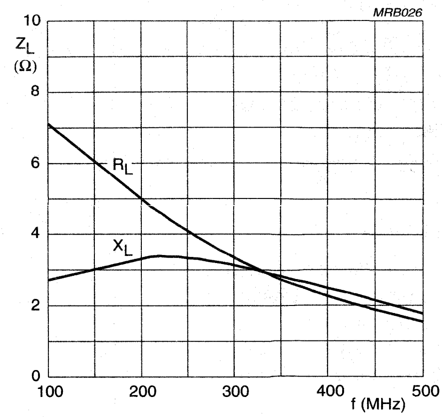
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized to serve as a ground plane. Connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 100 mA (per section); P_L = 100 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 100 mA (per section); P_L = 100 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

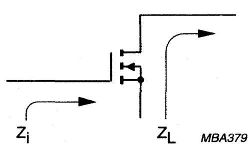
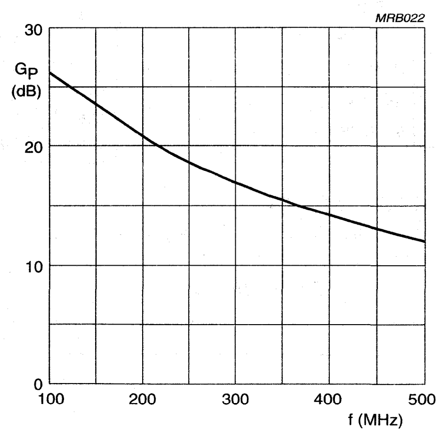


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 100 mA (per section); P_L = 100 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

UHF push-pull power MOS transistor — BLF548

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A2

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

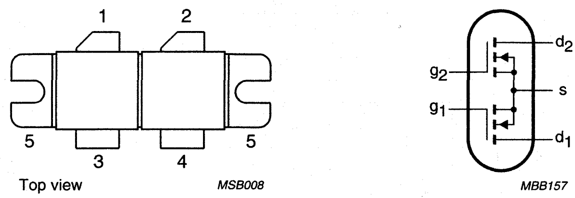


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	150	> 10	> 50

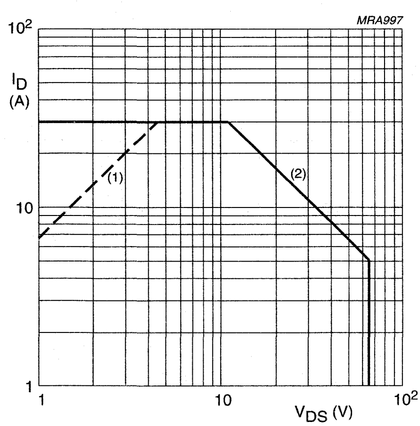
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	15	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	330	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

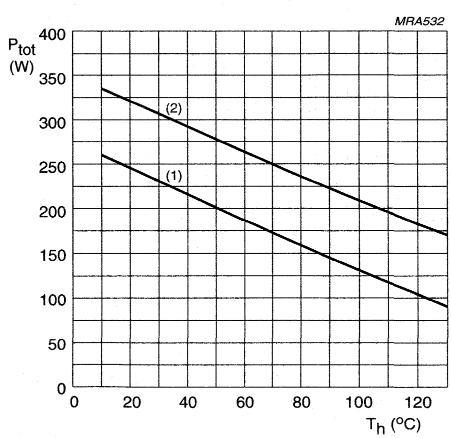
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 330 W; total device; both sections equally loaded	0.5 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



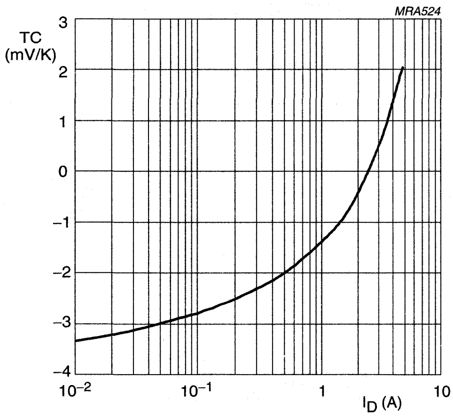
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

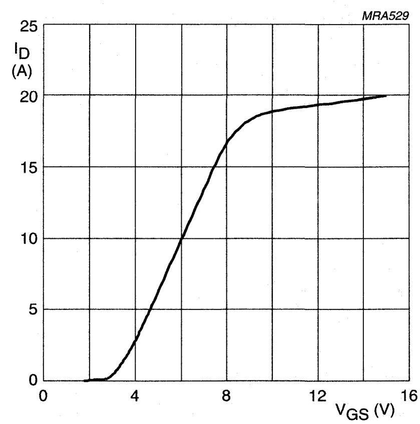
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 40 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 160 mA; V_{DS} = 10 V	2	–	4	V
g_{fs}	forward transconductance	I_D = 4.8 A; V_{DS} = 10 V	2.4	3.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 4.8 A; V_{GS} = 10 V	–	0.25	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	16	20	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	105	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	90	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF



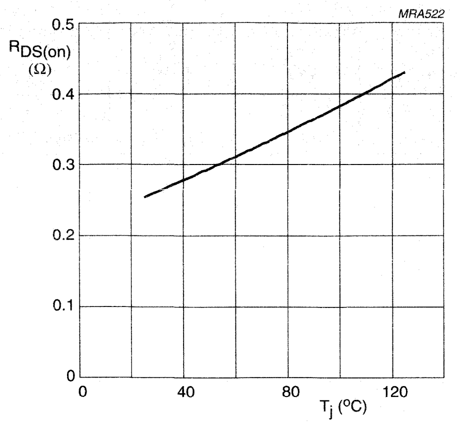
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



I_D = 4.8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.

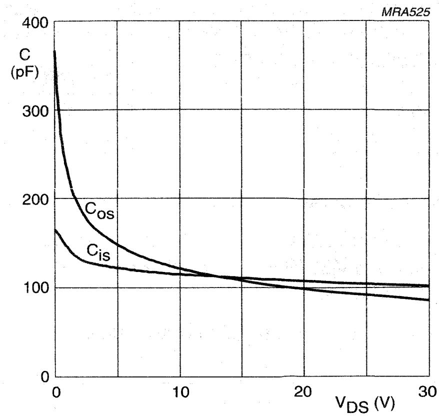


Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.

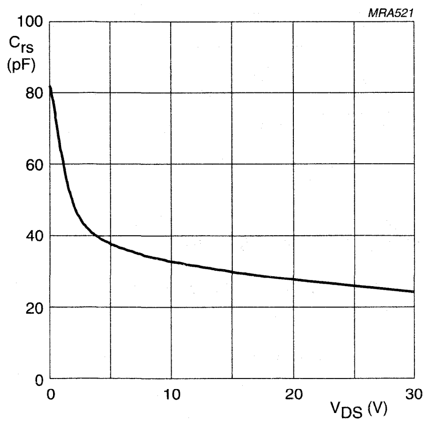


Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

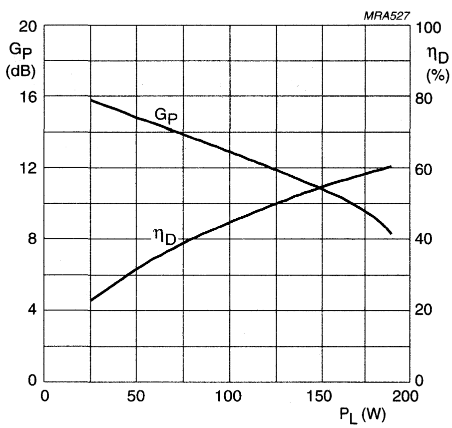
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W, unless otherwise specified.
RF performance in a common source, push-pull, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 160	150	> 10 typ. 11	> 50 typ. 55

Ruggedness in class-B operation

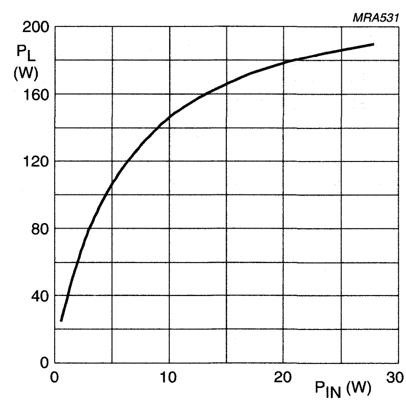
The BLF548 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 160 mA;
f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 160 mA;
f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.10 Load power as a function of input power, typical values.

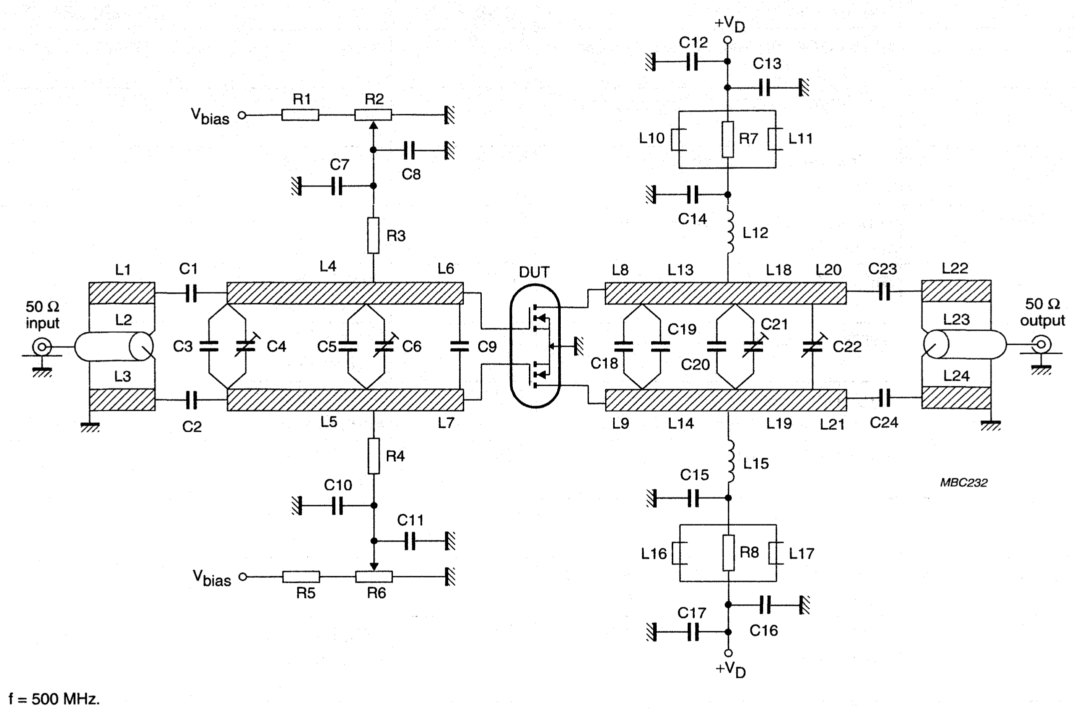


Fig.11 Test circuit for class-B operation.

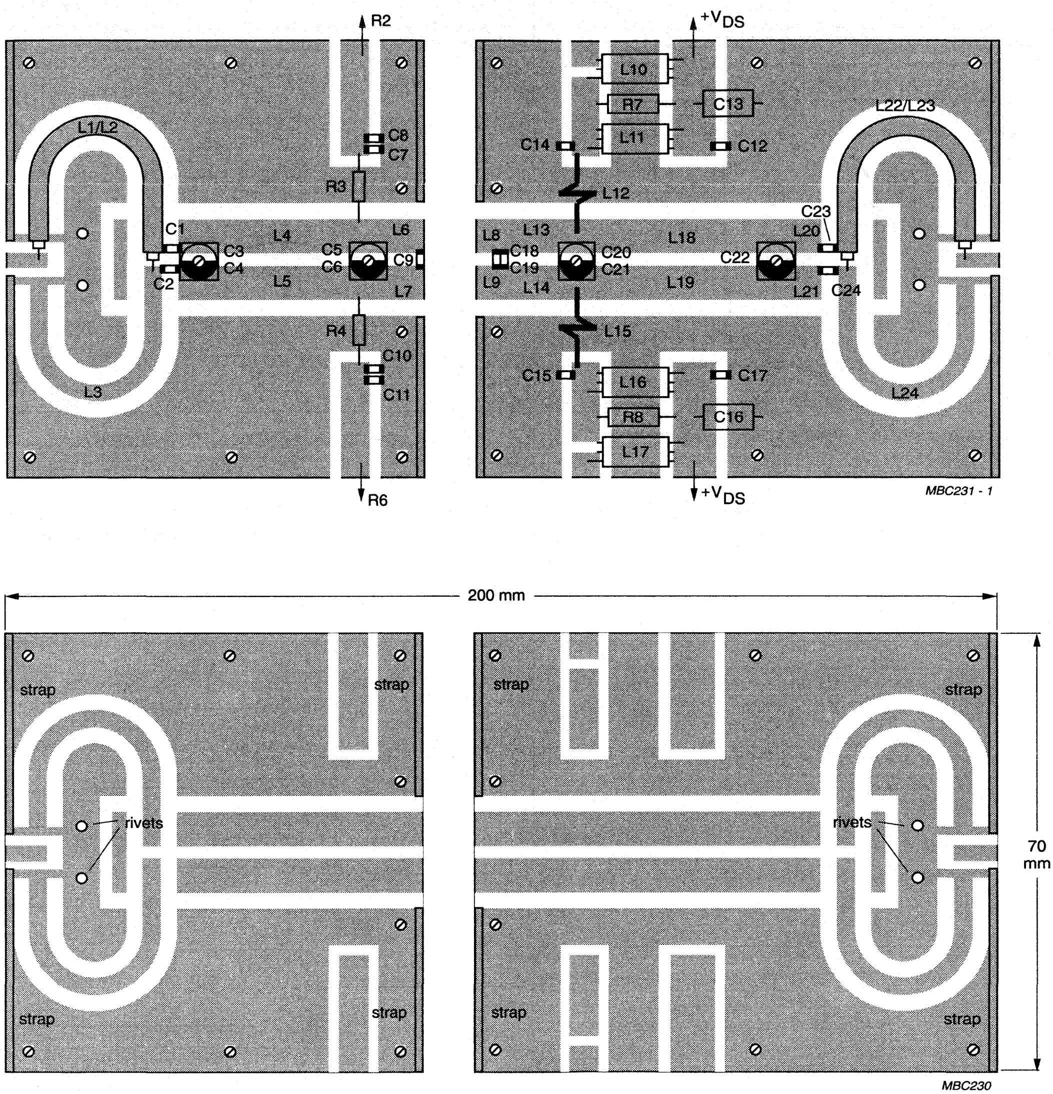
List of components (see class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	22 pF		
C3	multilayer ceramic chip capacitor (note 1)	16 pF		
C4	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 2)	27 pF		
C6, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7, C10, C14, C15	multilayer ceramic chip capacitor (note 1)	390 pF		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9	multilayer ceramic chip capacitor (note 3)	2 × 56 pF in series		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C13, C16	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C18	multilayer ceramic chip capacitor (note 2)	18 pF		
C19	multilayer ceramic chip capacitor (note 2)	12 pF		
C20	multilayer ceramic chip capacitor (note 2)	8.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	30 pF		
L1, L3, L22, L24	stripline (note 4)	34.5 Ω	length 66.5 mm width 4 mm	
L2, L23	semi-rigid cable (note 5)	50 Ω	length 66.5 mm width 3.6 mm	
L4, L5	stripline (note 4)	22.3 Ω	length 35 mm width 7 mm	
L6, L7	stripline (note 4)	22.3 Ω	length 10 mm width 7 mm	
L8, L9	stripline (note 4)	22.3 Ω	length 5.5 mm width 7 mm	
L10, L11, L16, L17	grade 3B Ferroxcube wideband RF choke			4312 020 36642
L12, L15	1 turn enamelled 1.5 mm copper wire	17 nH	length 5 mm int. dia. 9 mm leads 2 × 5 mm	
L13, L14	stripline (note 4)	22.3 Ω	length 15 mm width 7 mm	
L18, L19	stripline (note 4)	22.3 Ω	length 36 mm width 7 mm	
L20, L21	stripline (note 4)	22.3 Ω	length 8.5 mm width 7 mm	
R1, R5	0.4 W metal film resistor	24.7 kΩ		2322 151 72473
R2, R6	10 turn potentiometer	5 kΩ		
R3, R4	0.4 W metal film resistor	10.5 kΩ		2322 151 71053
R7, R8	1 W metal film resistor	10 Ω		2322 151 51009

Notes

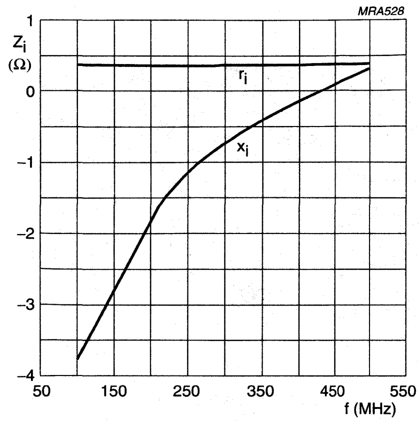
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
4. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 0.79 mm.
5. Cables L2 and L23 are soldered to striplines L1 and L22 respectively.



The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as a ground plane. Connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

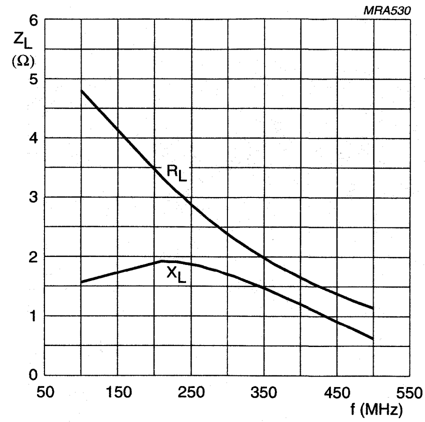
Fig.12 Component layout for 500 MHz class-B test circuit.

UHF push-pull power MOS transistor BLF548



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

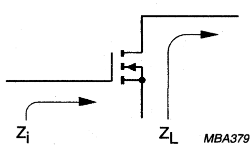
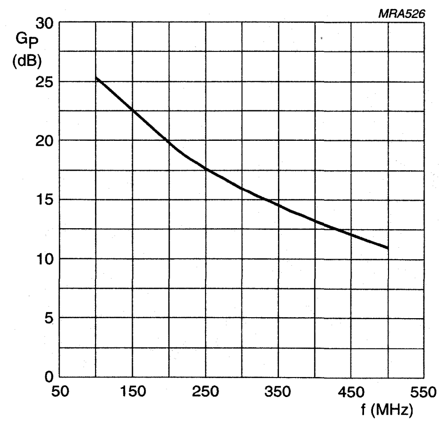


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

UHF power LDMOS transistor BLF861

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (UHF band).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS push-pull transistor in a SOT540A package with ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT540A

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source connected to flange

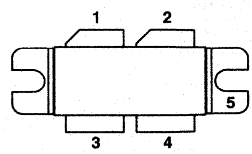


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	ΔG_p (dB)
CW, class-AB	860	32	150	>14	>50	≤1
PAL BG (TV), class-AB	860 (ch 69)	32	typ.170 (peak sync)	>14	>40	note 1

Note

1. Sync compression: input sync ≥ 33%; output sync 27%.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	T_{mb} ≤ 25 °C	–	318	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 318 W	0.55	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.2	K/W

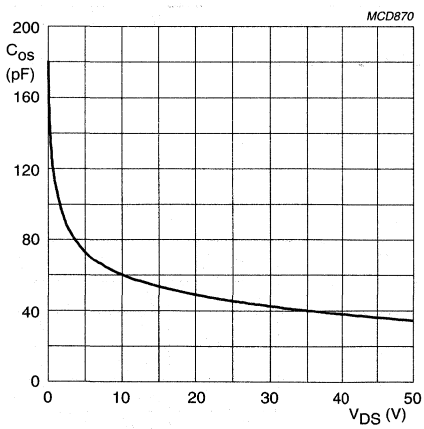
CHARACTERISTICS

T_j = 25 °C; per section; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.5 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 150 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 32 V	–	–	1	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	18	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	10	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 4 A	–	4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 4 A	–	160	–	mΩ
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz (1)	–	84	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz (1)	–	42	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz (1)	–	6	–	pF

Note

1. Capacitance values without internal matching.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.2 Output capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb-h}$ = 0.15 K/W, unless otherwise specified.

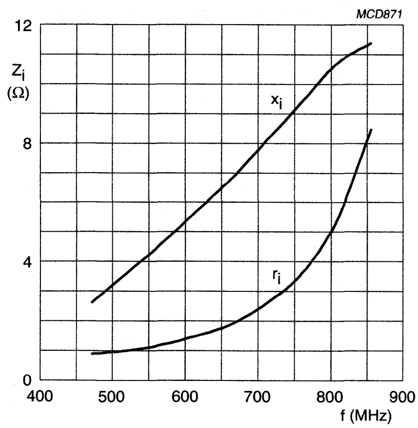
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)	ΔG_p (dB)
CW, class-AB	860	32	1	150	>14	>50	–	≤1
2-tone, class-AB	f_1 = 860 f_1 = 860.1	32	1	150 (PEP)	>14	>40	≤–25 typ. –30	–
PAL BG (TV), class-AB	860 (ch 69)	32	1	typ.170 (peak sync)	>14	>40	–	note 1

Note

1. Sync compression: input sync ≥ 33%; output sync 27% measured in narrowband test circuit.

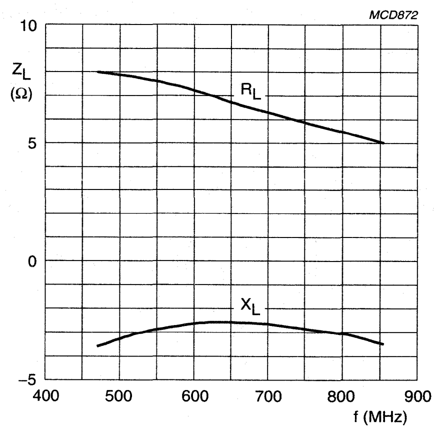
Ruggedness in class-AB operation

The BLF861 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 860 MHz at rated load power.



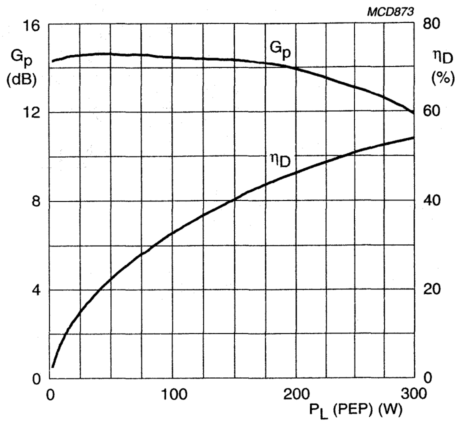
CW, class-AB operation; V_{DS} = 32 V; I_{DQ} = 1 A;
P_L = 170 W (total device); T_h = 25 °C.

Fig.3 Input impedance as a function of frequency (series components); typical push-pull values.



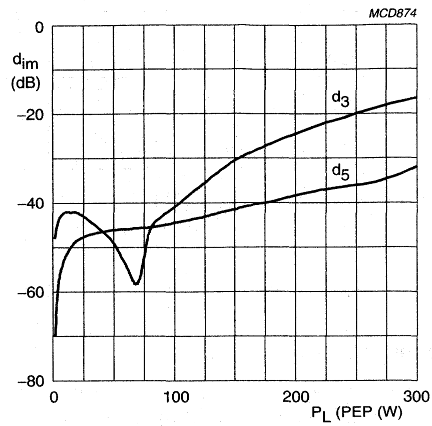
CW, class-AB operation; V_{DS} = 32 V; I_{DQ} = 1 A;
P_L = 170 W (total device); T_h = 25 °C.

Fig.4 Load impedance as a function of frequency (series components); typical push-pull values.



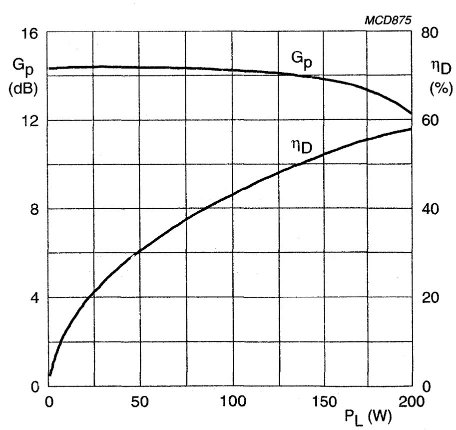
T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A.
2-tone: f_1 = 860 MHz (−6 dB); f_2 = 860.1 MHz (−6 dB)
measured in 860 MHz test circuit.

Fig.5 Power gain and drain efficiency as functions of peak envelope load power; typical values.



T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A.
2-tone: f_1 = 860 MHz (−6 dB); f_2 = 860.1 MHz (−6 dB)
measured in 860 MHz test circuit.

Fig.6 Intermodulation distortion as a function of peak envelope output power; typical values.



T_h = 25 °C; V_{DS} = 32 V; ; I_{DQ} = 1 A; CW, class-AB; f = 860 MHz;
measured in 860 MHz test circuit.

Fig.7 Power gain and drain efficiency as functions of load power; typical values.

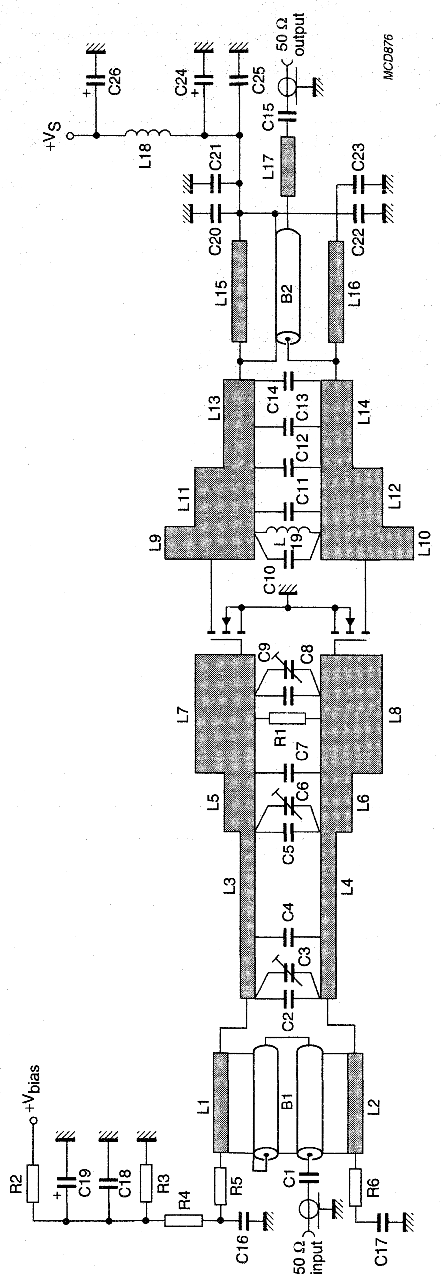


Fig.8 Class-AB broadband test circuit.

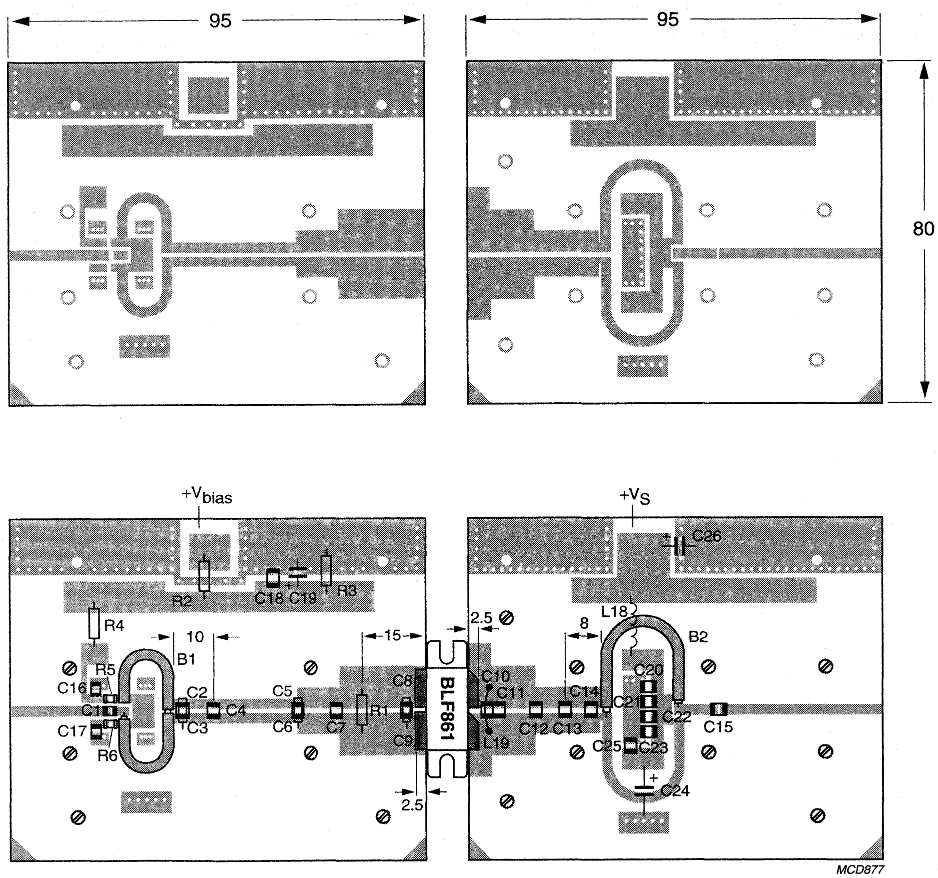
List of components class-AB test circuit (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	multilayer ceramic chip capacitor; note 1	20 pF	
C2	multilayer ceramic chip capacitor; note 1	4.3 pF	
C3, C6, C9	Tekelec trimmer	0.6 to 4.5 pF	
C4	multilayer ceramic chip capacitor; note 1	9.1 pF	
C5	multilayer ceramic chip capacitor; note 1	10 pF	
C7	multilayer ceramic chip capacitor; note 1	5.1 pF	
C8	multilayer ceramic chip capacitor; note 1	13 pF	
C10, C11	multilayer ceramic chip capacitor; note 2	8.2 pF	
C12, C13	multilayer ceramic chip capacitor; note 2	6.8 pF	
C14	multilayer ceramic chip capacitor; note 3	1 pF	
C15	multilayer ceramic chip capacitor; note 3	20 pF	
C16, C17	multilayer ceramic chip capacitor	1 nF	
C18	multilayer ceramic chip capacitor	100 nF	
C19, C26	multilayer ceramic chip capacitor	100 μF	
C20, C21, C22, C23	multilayer ceramic chip capacitor; note 2	100 pF	
C24	electrolytic capacitor	1000 μF	
C25	multilayer ceramic chip capacitor	1 μF	2222 595 16754
L1, L2	stripline; note 4		30.6 x 2.4 mm
L3, L4	stripline; note 4		28 x 2.4 mm
L5, L6	stripline; note 4		10 x 5 mm
L7, L8	stripline; note 4		20 x 10 mm
L9, L10	stripline; note 4		5.5 x 15 mm
L11, L12	stripline; note 4		10 x 10 mm
L13, L14	stripline; note 4		15 x 5 mm
L15, L16	stripline; note 4		48.5 x 2.4 mm
L17	stripline; note 4		10 x 2.4 mm
L18	ferrite		
L19	wire inductor (hairpin)		length = 17 mm
B1	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	70 mm
B2	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	48.5 mm
R1	resistor	33 Ω	
R2	resistor	1 kΩ	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
R3	resistor	100 kΩ	
R4	resistor	100 Ω	
R5, R6	SMD resistor	3.9 Ω	

Notes

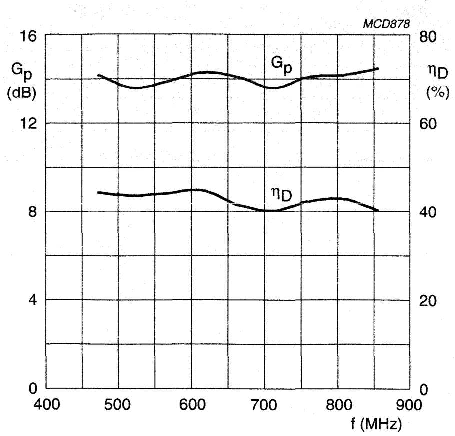
1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 180R or capacitor of same quality.
3. American Technical Ceramics type 100B or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board: Rogers 5880 (ε_r = 2.2); thickness 0.79 mm.



Dimensions in mm.

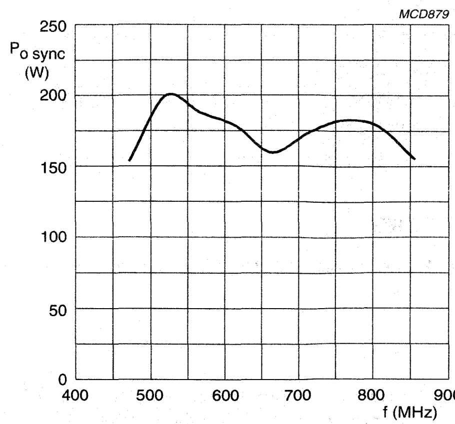
The components are situated on one side of the Rogers 5880 printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.9 Printed-circuit board and component layout for the class-AB broadband test circuit.



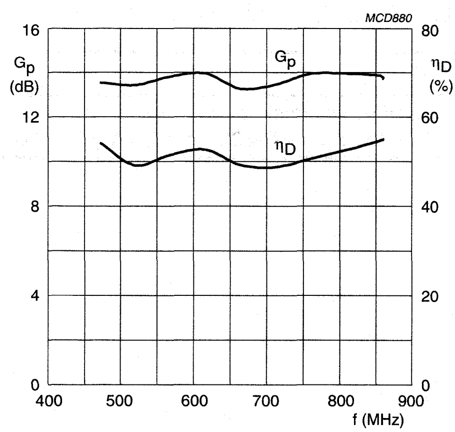
T_h = 25 °C; V_{CE} = 32 V; I_{DQ} = 1 A; PAL BG signal (TV);
Sync compression: input 33%, output 27%;
measured in broadband test circuit.

Fig.10 Power gain and drain efficiency as functions of frequency; typical values.



T_h = 25 °C; V_{CE} = 32 V; I_{DQ} = 1 A; PAL BG signal (TV);
Sync compression: input 33%, output 27%;
measured in broadband test circuit.

Fig.11 Peak envelope sync power as a function of frequency; typical values.



T_h = 25 °C; V_{DS}= 32 V; I_{DQ} = 1 A; CW, class-AB operation;
P_L = 150 W; measured in broadband test circuit.

Fig.12 Power gain and drain efficiency as functions of frequency; typical values.

UHF power LDMOS transistor BLF1043

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flangeless package (SOT538A) with a ceramic cap. The common source is connected to the mounting base.

PINNING - SOT538A

PIN	DESCRIPTION
1	drain
2	gate
3	source

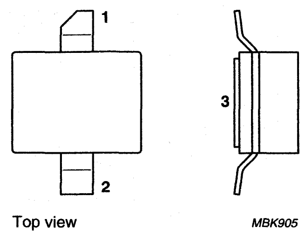


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	10 (PEP)	>16	>35	≤–30
CW, class-AB (1-tone)	960	26	10	>16	>45	–

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	2.2	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	tbf	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25$ °C; note 1	4.6	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

Note

1. Thermal resistance is determined under RF operating conditions.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 0.2$ mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10$ V; $I_D = 20$ mA	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26$ V	–	–	0.15	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9$ V; $V_{DS} = 10$ V	3	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15$ V; $V_{DS} = 0$	–	–	1	μA
g_{fs}	forward transconductance	$V_{DS} = 10$ V; $I_D = 0.75$ A	–	0.5	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 0.75$ A	–	1.2	–	Ω
C_{is}	input capacitance	$V_{GS} = 0$; $V_{DS} = 26$ V; f = 1 MHz	–	11	–	pF
C_{os}	output capacitance	$V_{GS} = 0$; $V_{DS} = 26$ V; f = 1 MHz	–	9	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26$ V; f = 1 MHz	–	0.6	–	pF

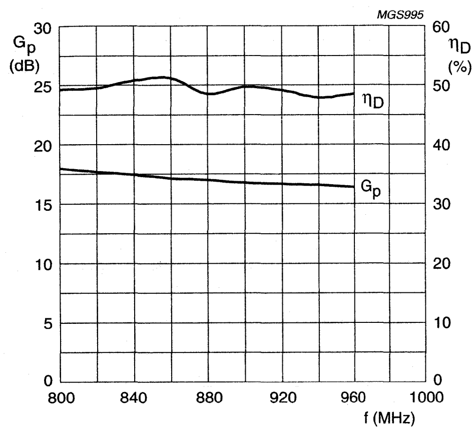
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	25	10 (PEP)	>16	>35	≤−30
CW, class-AB (1-tone)	960	26	25	10	>16	>45	−

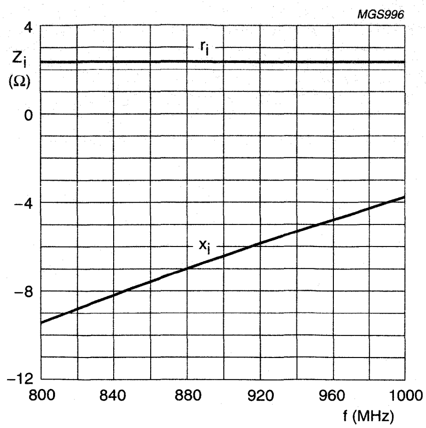
Ruggedness in class-AB operation

The BLF1043 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 960 MHz at rated load power.



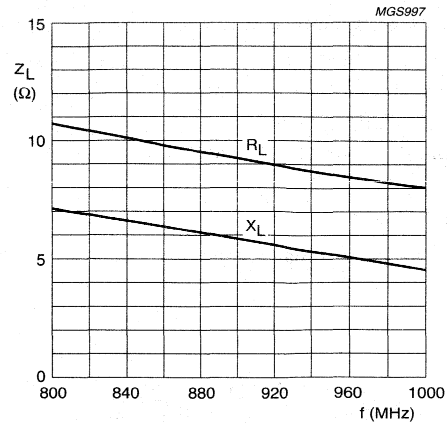
Class-AB operation; V_{DS} = 26 V; I_{DQ} = 80mA;
P_L = 10 W (PEP).

Fig.2 Power gain and efficiency as functions of frequency, typical values.



V_{DS} = 26 V; I_{DQ} = 80 mA; P_L = 10 W (PEP); $T_h \le 25$ °C.
Impedance measured at reference planes (see Fig.5).

Fig.3 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 80 mA; P_L = 10 W (PEP); $T_h \le 25$ °C.
Impedance measured at reference planes (see Fig.5).

Fig.4 Load impedance as a function of frequency (series components); typical values.

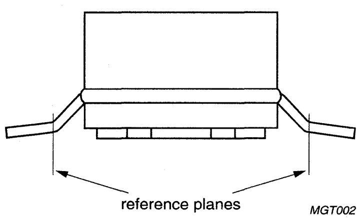


Fig.5 Measuring reference planes SOT538A.

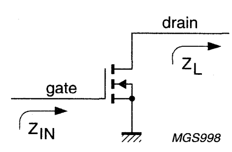


Fig.6 Definition of transistor impedance.

UHF power LDMOS transistor | BLF1046

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

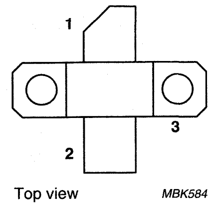


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	45 (PEP)	>14	>35	≤–28
CW, class-AB (1-tone)	960	26	45	>14	>45	–

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±20	V
I_D	drain current (DC)	–	4.5	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C, P_{dis} = 97 W; note 1	1.2	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.6	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.7 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 70 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	1	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	12.5	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	125	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.5 A	–	2	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 3.5 A	–	300	–	mΩ
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	46	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	37	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	1.5	–	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.6 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	45 (PEP)	>14	>35	≤–28
CW, class-AB (1-tone)	960	26	45	>14	>45	–

Ruggedness in class-AB operation

The BLF1046 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 960 MHz at rated load power.

UHF power LDMOS transistor BLF1047

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT541A) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT541A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

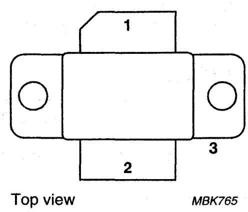


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	$f_1 = 960$; $f_2 = 960.1$	26	70 (PEP)	>14	>35	≤–26
CW, class-AB (1-tone)	960	26	70	>14	>45	–

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±20	V
I_D	drain current (DC)	–	9	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C, P_{dis} = 100 W; note 1	1.15	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.4 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 140 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	10	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	20	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	250	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	–	3	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 5 A	–	200	–	mΩ
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	75	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	65	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	2.5	–	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 1.15 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	70 (PEP)	>14	>35	≤–26
CW, class-AB (1-tone)	960	26	70	>14	>45	–

Ruggedness in class-AB operation

The BLF1047 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 960 MHz at rated load power.

UHF power LDMOS transistor BLF1048

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT502A) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

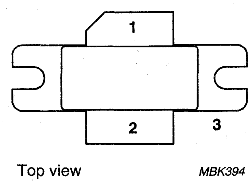


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	90 (PEP)	>14	>35	≤–26
CW, class-AB (1-tone)	960	26	90	>14	>45	–

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±20	V
I_D	drain current (DC)	–	9	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C; P_{tot} = 100 W; note 1	1.15	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.4 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 140 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	10	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	25	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	250	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7 A	–	4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 7 A	–	150	–	mΩ
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	92	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	74	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	3	–	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 1.15 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	90 (PEP)	>14	>35	≤–26
CW, class-AB (1-tone)	960	26	90	>14	>45	–

Ruggedness in class-AB operation

The BLF1048 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 960 MHz at rated load power.

UHF power LDMOS transistor — BLF2043

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 2.2 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flangeless package (SOT538A) with a ceramic cap. The common source is connected to the mounting base.

PINNING - SOT538A

PIN	DESCRIPTION
1	drain
2	gate
3	source

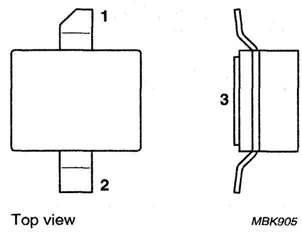


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 2000; f_2 = 2000.1	26	10 (PEP)	>12	>30	≤–26

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	2.2	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	tbf	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; note 1	5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

Note

1. Thermal resistance is determined under RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.2 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 20 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	1.5	μA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	3	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	40	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.75 A	–	0.5	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.75 A	–	1.2	–	Ω
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	11	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	9	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	0.5	–	pF

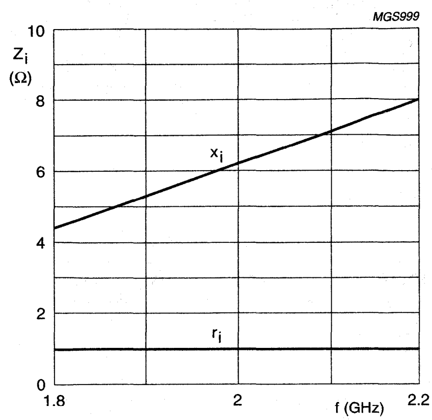
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 2000; f_2 = 2000.1	26	25	10 (PEP)	>12	>30	≤–26

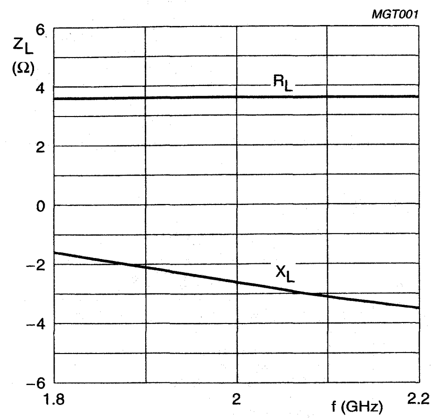
Ruggedness in class-AB operation

The BLF2043 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 2000 MHz at rated load power.



V_{DS} = 26 V; I_{DQ} = 25 mA; P_L = 10 W; $T_h \leq 25$ °C.
Impedance measured at reference planes (see Fig.4).

Fig.2 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 25 mA; P_L = 10 W; $T_h \leq 25$ °C.
Impedance measured at reference planes (see Fig.4).

Fig.3 Load impedance as a function of frequency (series components); typical values.

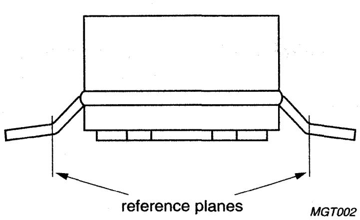


Fig.4 Measuring reference planes SOT538A.

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation.

APPLICATIONS

- Communication transmitter applications (PCN/PCS) in the 1.8 to 2.2 GHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

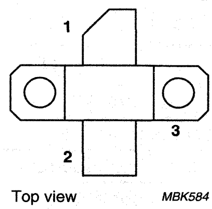


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	30 (PEP)	>10	>30	≤–25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	drain current (DC)	–	4.5	A
T_{stg}	storage temperature	–65	150	°C
T_j	junction temperature	–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	P_{tot} = 87.5 W; T_h = 25 °C; note 1	2.1	K/W

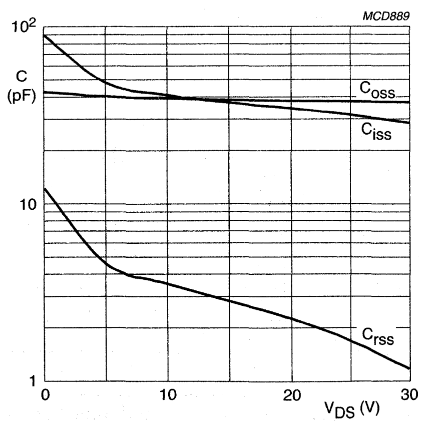
Note

1. Thermal resistance is determined under specified RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.7 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 70 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	5	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	9	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	125	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.5 A	–	2	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 2.5 A	–	340	–	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	38	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	31	–	pF
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	1.7	–	pF



V_{GS} = 0; f = 1 MHz.

Fig.2 Input, output and feedback capacitance as functions of drain-source voltage, typical values.

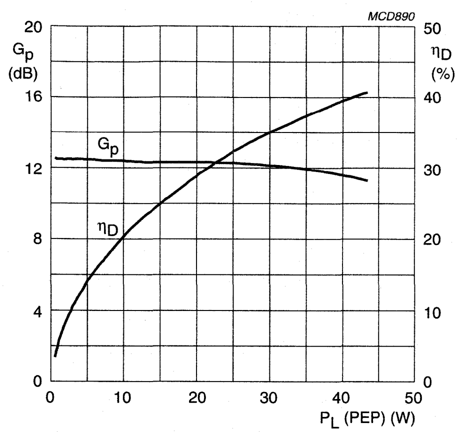
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.65 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	180	30 (PEP)	>10	>30	≤−25

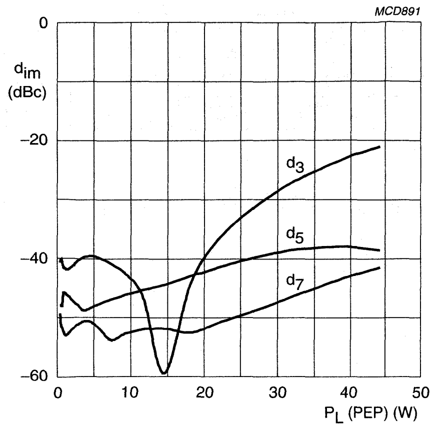
Ruggedness in class-AB operation

The BLF2045 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; P_L = 30 W (CW); f = 2000 MHz.



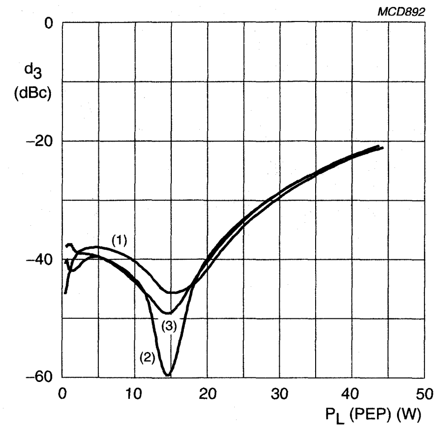
Class-AB operation; V_{DS} = 26 V; I_{DQ} = 180 mA;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.3 Power gain and efficiency as functions of peak envelope load power, typical values.



V_{DS} = 26 V; I_{DQ} = 180 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.4 Intermodulation distortion as a function of peak envelope load power; typical values.



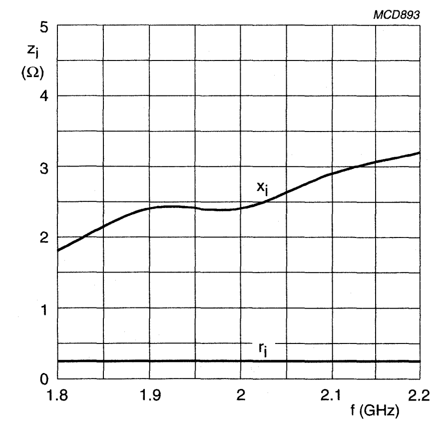
V_{DS} = 26 V; $T_h \leq 25$ °C; f_1 = 2000 MHz; f_2 = 2000.1 MHz.

(1) I_{DQ} = 140 mA.

(2) I_{DQ} = 180 mA.

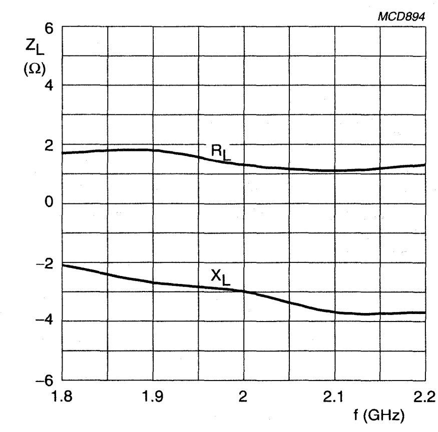
(3) I_{DQ} = 220 mA.

Fig.5 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 180 mA; P_L = 45 W; $T_h \leq 25$ °C.

Fig.6 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 180 mA; P_L = 45 W; $T_h \leq 25$ °C.

Fig.7 Load impedance as a function of frequency (series components); typical values.

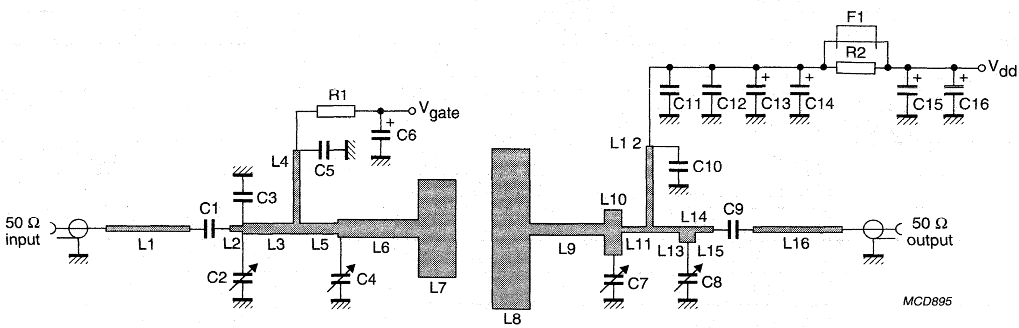


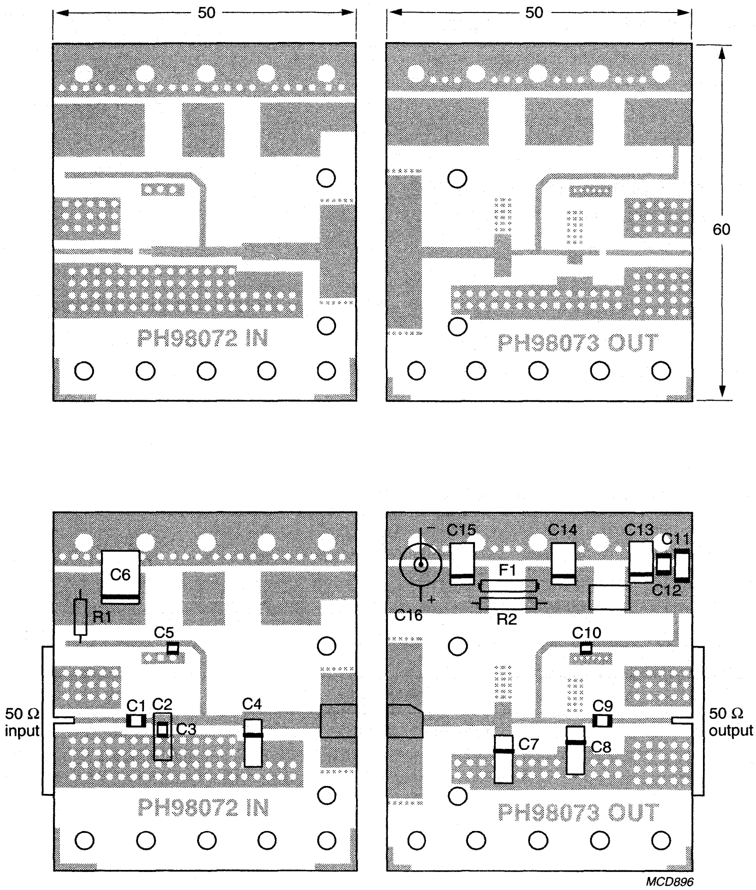
Fig.8 Class-AB test circuit for 2 GHz.

List of components (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C2, C4, C7 and C8	Tekelec variable capacitor; type 37281	0.4 to 2.5 pF		
C3	multilayer ceramic chip capacitor; note 1	2.4 pF		
C1, C5, C9 and C10	multilayer ceramic chip capacitor; note 1	11 pF		
C11	multilayer ceramic chip capacitor; note 2	1 nF		
C12	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C6, C13, C14 and C15	tantalum SMD capacitor	4.5 μF; 50 V		
C16	electrolytic capacitor	100 μF; 63 V		2222 037 58101
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	13 × 0.9 mm	
L2	stripline; note 3	50 Ω	2 × 0.9 mm	
L3	stripline; note 3	34.3 Ω	15 × 1.7 mm	
L4 and L12	stripline; note 3	50 Ω	37 × 0.9 mm	
L5	stripline; note 3	34.3 Ω	6 × 1.7 mm	
L6	stripline; note 3	23.6 Ω	13 × 2.9 mm	
L7	stripline; note 3	5.6 Ω	6 × 15.8 mm	
L8	stripline; note 3	3.5 Ω	6 × 26 mm	
L9	stripline; note 3	31.9 Ω	12 × 1.9 mm	
L10	stripline; note 3	24.9 Ω	7.4 × 2.7 mm	
L11	stripline; note 3	50 Ω	3 × 0.9 mm	
L13	stripline; note 3	50 Ω	4.15 × 0.9 mm	
L14	stripline; note 3	26.3 Ω	2.5 × 2.5 mm	
L15	stripline; note 3	50 Ω	2.8 × 0.9 mm	
L16	stripline; note 3	50 Ω	14 × 0.9 mm	
R1 and R2	metal film resistor	10 Ω, 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15); thickness 0.64 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15), thickness 0.64 mm. The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 2 GHz class-AB test circuit.

UHF power LDMOS transistor BLF2047

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (1.8 to 2.2 GHz).
- Internal input and output matching for high gain and efficiency

APPLICATIONS

- Common source class-AB operation for PCN and PCS applications in the 1800 to 2200 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange SOT502A package with a ceramic cap. The common source is connected to the mounting flange.

PINNING

PIN	DESCRIPTION
1	drain
2	gate
3	source connected to flange

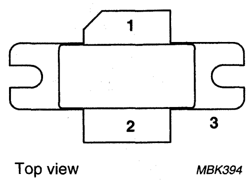


Fig.1 Simplified outline SOT502A.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
Two-tone, class-AB	f_1 = 2200; f_2 = 2200.1	26	65 (PEP)	>10	>30	≤−25
		28	65 (PEP)	typ. 12.6	typ. 31	typ. −29

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	DC drain current	–	9	A
T_{stg}	storage temperature	−65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C, P_{tot} = 152 W, note 1	1.15	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.4 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 140 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	10	μA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	18	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	250	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	–	4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 5 A	–	0.17	–	Ω
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	3.4	–	pF

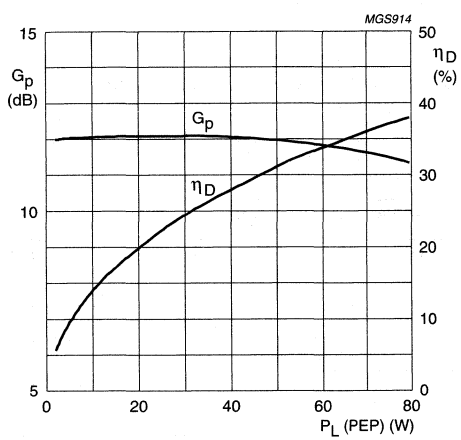
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j-h}$ = 1.15 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
Two-tone, class-AB	f_1 = 2200; f_2 = 2200.1	26	400	65 (PEP)	>10	>30	≤−25
		28	400	65 (PEP)	typ. 12.6	typ. 31	typ. −29

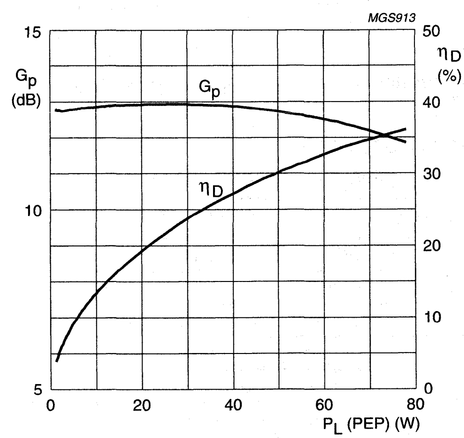
Ruggedness in class-AB operation

The BLF2047 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; I_{DQ} = 400 mA; P_L = 65 W (CW); f = 2200 MHz.



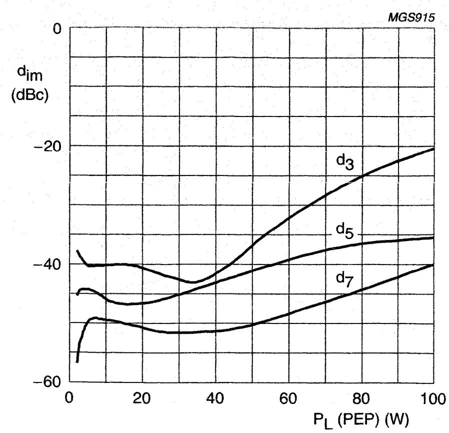
V_{DS} = 26 V; I_{DQ} = 400 mA; T_h ≤ 25 °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.2 Power gain and drain efficiency as functions of peak envelope load power; typical values.



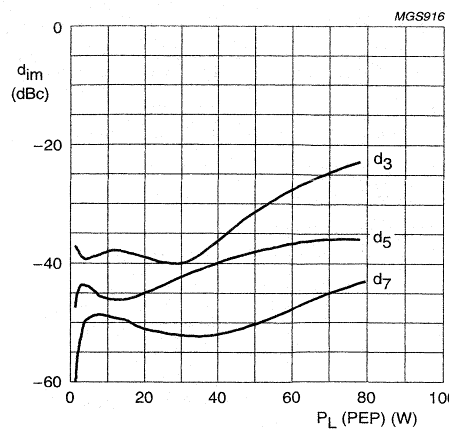
V_{DS} = 26 V; I_{DQ} = 400 mA; T_h ≤ 25 °C;
f_1 = 2200 MHz; f_2 = 2200.1 MHz.

Fig.3 Power gain and drain efficiency as functions of peak envelope load power; typical values.



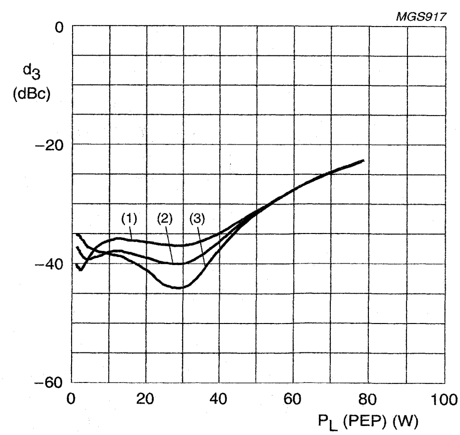
V_{DS} = 26 V; I_{DQ} = 400 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.4 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 400 mA; $T_h \leq 25$ °C;
f_1 = 2200 MHz; f_2 = 2200.1 MHz.

Fig.5 Intermodulation distortion as a function of peak envelope load power; typical values.



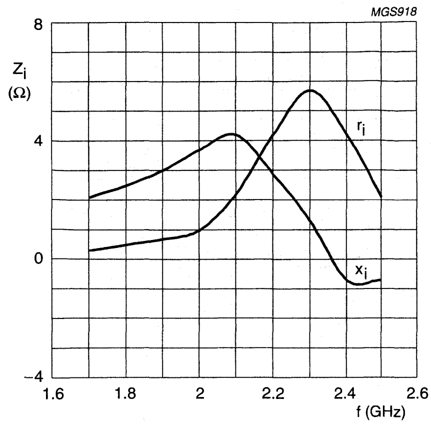
V_{DS} = 26 V; $T_h \leq 25$ °C; f_1 = 2200 MHz; f_2 = 2200.1 MHz.

(1) I_{DQ} = 350 mA.

(2) I_{DQ} = 400 mA.

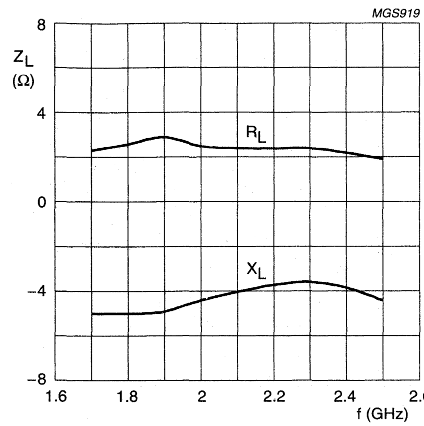
(3) I_{DQ} = 450 mA.

Fig.6 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 400 mA; P_L = 80 W; $T_h \leq 25$ °C.

Fig.7 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 400 mA; P_L = 80 W; $T_h \leq 25$ °C.

Fig.8 Load impedance as a function of frequency (series components); typical values.

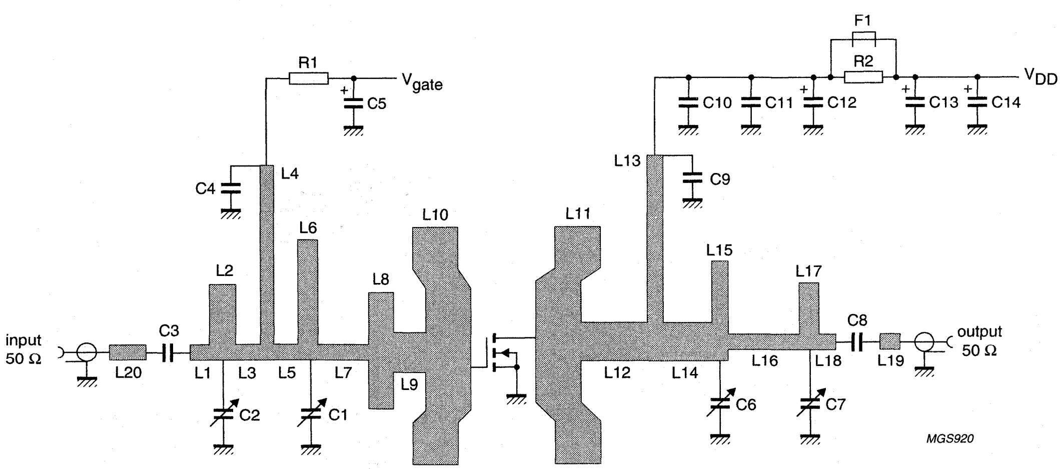


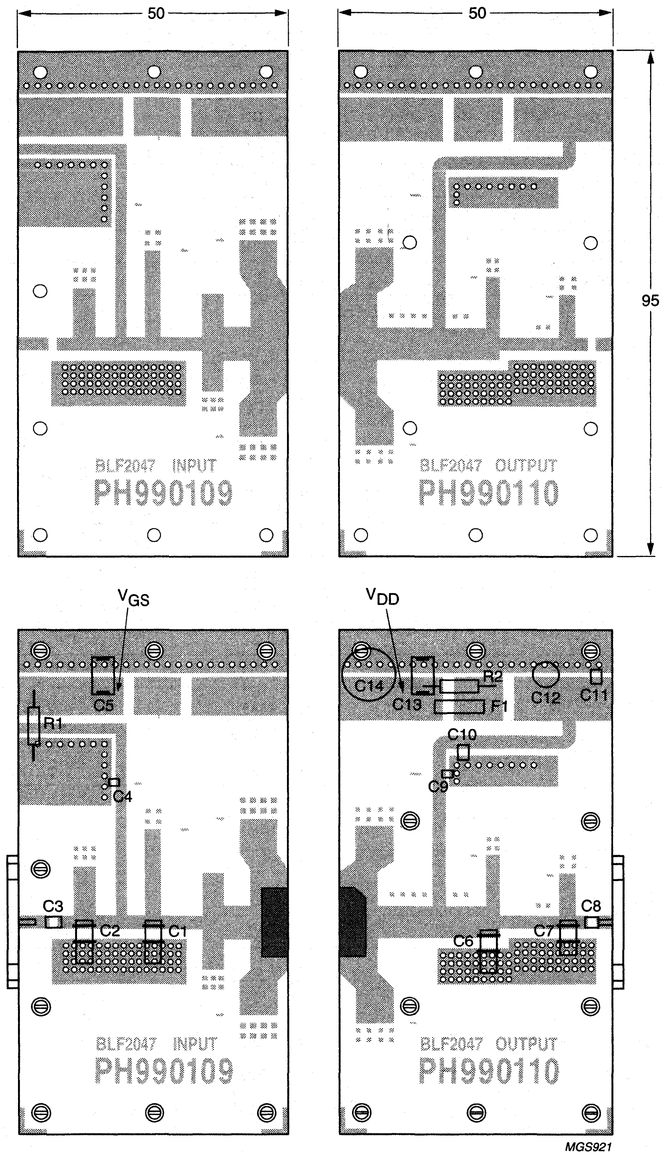
Fig.9 Class-AB test circuit at f = 2.2 GHz.

List of components (See Figs 9 and 10)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C6, C7	Tekelec variable capacitor; type 37281	0.4 to 2.5 pF		
C3, C8	multilayer ceramic chip capacitor; note 1	12 pF		
C4, C9	multilayer ceramic chip capacitor; note 2	12 pF		
C5, C12	electrolytic capacitor	10 μF; 100 V		2222 037 59109
C10	multilayer ceramic chip capacitor; note 1	1 nF		
C11	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C13	tantal SMD capacitor	4.5 μF; 50 V		
C14	electrolytic capacitor	100 μF; 63 V		2222 037 58101
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	2.9 × 2.4 mm	
L2	stripline; note 3	14.5 Ω	4 × 11.7 mm	
L3	stripline; note 3	50 Ω	3.7 × 2.4 mm	
L4	stripline; note 3	6 Ω	2 × 30.8 mm	
L5	stripline; note 3	50 Ω	3.6 × 2.4 mm	
L6	stripline; note 3	9.5 Ω	3 × 18.8 mm	
L7	stripline; note 3	50 Ω	7.8 × 2.4 mm	
L8	stripline; note 3	9.8 Ω	4 × 18.3 mm	
L9	stripline; note 3	24.4 Ω	5 × 6.3 mm	
L10, L11	stripline; note 3	5.1 Ω	7 × 37 mm	
L12	stripline; note 3	25.4 Ω	10.1 × 6 mm	
L13	stripline; note 3	5.7 Ω	2.4 × 32.8 mm	
L14	stripline; note 3	25.4 Ω	7.4 × 6 mm	
L15	stripline; note 3	11.3 Ω	2.5 × 15.6 mm	
L16	stripline; note 3	50 Ω	10.8 × 2.4 mm	
L17	stripline; note 3	16.1 Ω	3 × 10.4 mm	
L18	stripline; note 3	50 Ω	2.3 × 2.4 mm	
L19	stripline; note 3	50 Ω	3 × 2.4 mm	
L20	stripline; note 3	50 Ω	5.5 × 2.4 mm	
R1, R2	metal film resistor	10 Ω, 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric ($\varepsilon_r = 2.2$); thickness 0.79 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.10 Component layout for 2.2 GHz class-AB test circuit.

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (1.8 to 2 GHz)
- Internal input and output matching for high gain and efficiency.

APPLICATIONS

- Common source class-AB operation for PCN and PCS applications in the 1800 to 2000 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistors encapsulated in a 2-lead SOT502A flange package with a ceramic cap. The common source is connected to the mounting flange.

PINNING

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

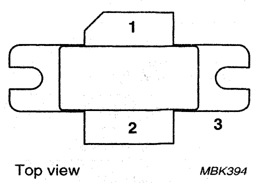


Fig.1 Simplified outline SOT502A.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
Two-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	65 (PEP)	>10.5	>30	≤–25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	DC drain current	–	9	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

UHF power LDMOS transistor — BLF2047L

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	$T_h = 25$ °C, $P_{tot} = 152$ W, note 1	1.15	K/W

Note

1. Determined under specified RF operating conditions.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 1.4$ mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10$ V; $I_D = 140$ mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26$ V	–	–	10	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GS\ th} + 9$ V; $V_{DS} = 10$ V	18	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15$ V; $V_{DS} = 0$	–	–	250	nA
g_{fs}	forward transconductance	$V_{DS} = 10$ V; $I_D = 5$ A	–	4	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GS\ th} + 9$ V; $I_D = 5$ A	–	0.17	–	Ω
C_{rss}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26$ V; f = 1 MHz	–	3.4	–	pF

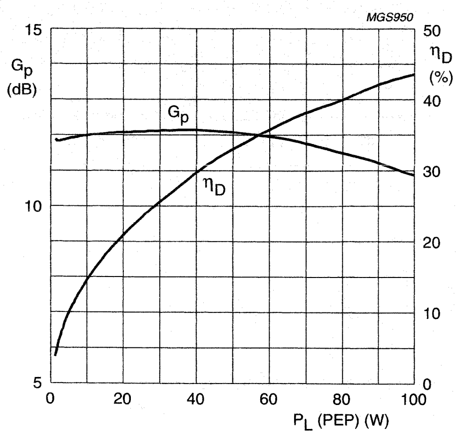
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25$ °C; $R_{th\ j\text{-}h} = 1.15$ K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
Two-tone, class-AB	$f_1 = 2000$; $f_2 = 2000.1$	26	350	65 (PEP)	>10.5	>30	≤–25

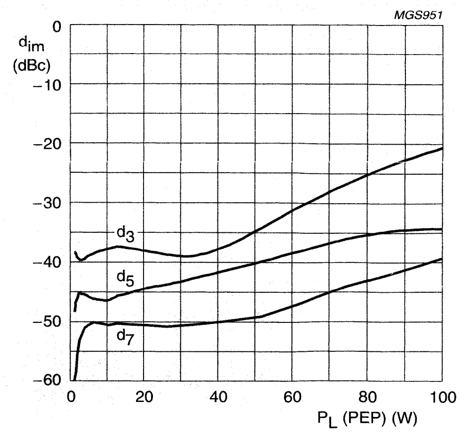
Ruggedness in class-AB operation

The BLF2047L is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 26$ V; $I_{DQ} = 350$ mA; $P_L = 65$ W; f = 2000 MHz.



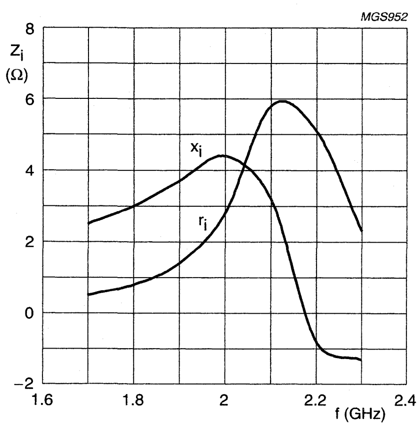
f_1 = 2000 MHz; f_2 = 2000.1 MHz; V_{DS} = 26 V; I_{DQ} = 350 mA; $T_h \leq 25$ °C.

Fig.2 Power gain and drain efficiency as a function of load power; typical values.



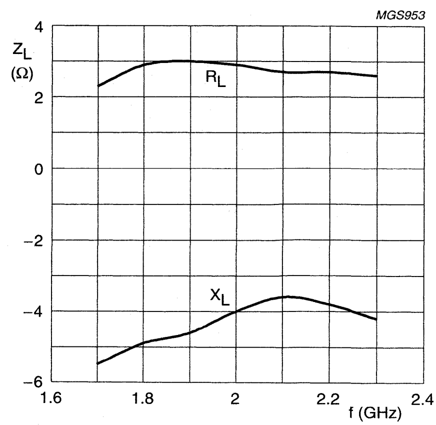
f_1 = 2000 MHz; f_2 = 2000.1 MHz; V_{DS} = 26 V; I_{DQ} = 350 mA; $T_h \leq 25$ °C.

Fig.3 Intermodulation distortion as a function of load power; typical values.



V_{DS} = 26 V; I_D = 350 mA; P_L = 65 W; $T_h \leq 25$ °C.

Fig.4 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_D = 350 mA; P_L = 65 W; $T_h \leq 25$ °C.

Fig.5 Load impedance as a function of frequency (series components); typical values.

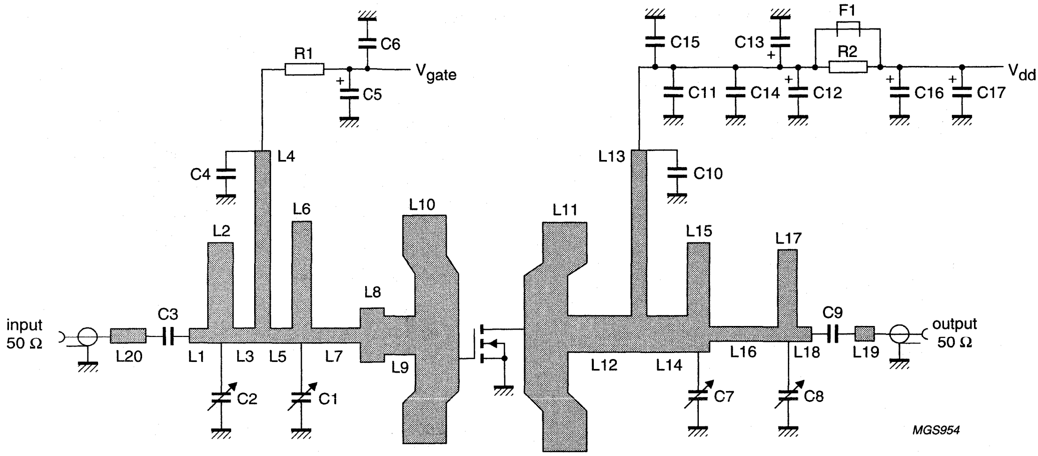


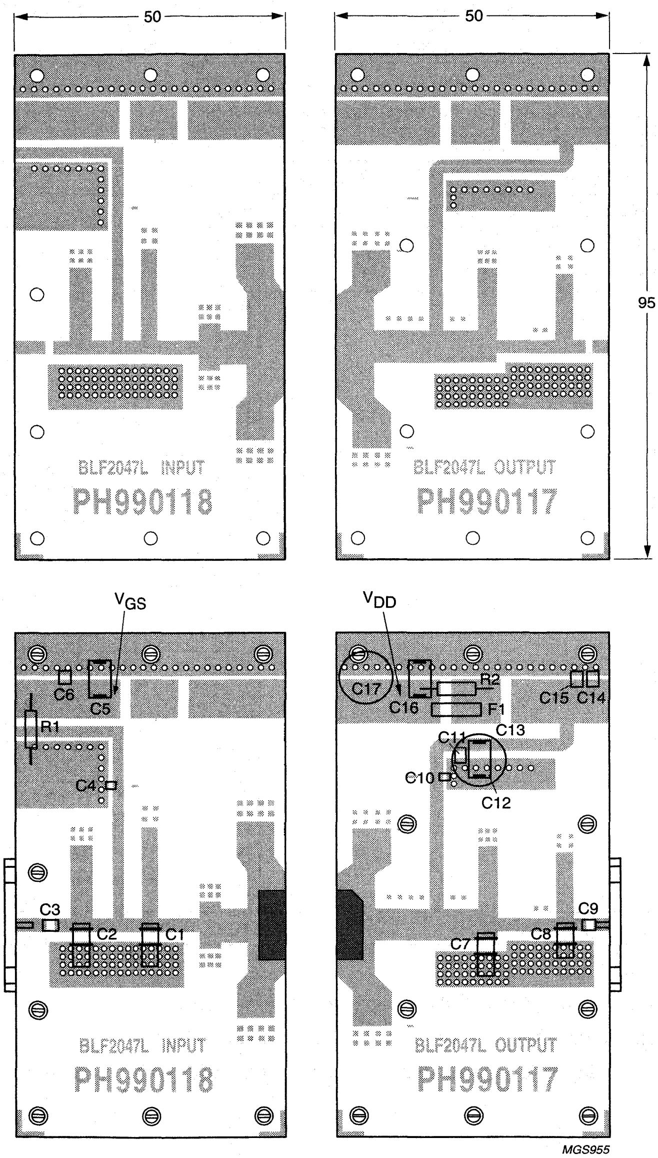
Fig.6 Class-AB test circuit at f = 2 GHz.

List of components (see Figs. 6 and 7)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7 and C8	Tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C3, C9	multilayer ceramic chip capacitor; note 1	12 pF		
C4, C10	multilayer ceramic chip capacitor; note 2	12 pF		
C5, C12 and C16	electrolytic capacitor	4.5 μF; 50 V		
C6, C11 and C15	multilayer ceramic chip capacitor; note 1	1 nF		
C13 and C17	electrolytic capacitor	100 μF; 63 V		2222 037 58101
C14	multilayer ceramic chip capacitor	100 nF		2222 581 16641
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	2.9 × 2.4 mm	
L2		10.8 Ω	4 × 16.3 mm	
L3		50 Ω	3.7 × 2.4 mm	
L4		6 Ω	2 × 30.8 mm	
L5		50 Ω	3.6 × 2.4 mm	
L6		9 Ω	3 × 19.9 mm	
L7		50 Ω	7.8 × 2.4 mm	
L8		18.5 Ω	4 × 8.8 mm	
L9		24.4 Ω	5 × 6.3 mm	
L10 and L11		5.1 Ω	7 × 37 mm	
L12		25.4 Ω	10.1 × 6 mm	
L13		5.7 Ω	2.4 × 32.8 mm	
L14		25.4 Ω	6.4 × 6 mm	
L15		10 Ω	3.5 × 17.8 mm	
L16		50 Ω	10.8 × 2.4 mm	
L17		11.8 Ω	3 × 14.9 mm	
L18		50 Ω	2.3 × 2.4 mm	
L19		50 Ω	3 × 2.4 mm	
L20		50 Ω	5.5 × 2.4 mm	
R1 and R2	metal film resistor	10 Ω, 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2); thickness 0.79 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.7 Component layout for 2 GHz class-AB test circuit.

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (1.8 to 2.0 GHz)
- Internal input and output matching for high gain and efficiency.

APPLICATIONS

- Common source class-AB operation for PCN and PCS applications in the 1800 to 2000 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistors encapsulated in a 2-lead SOT502A flange package with a ceramic cap. The common source is connected to the mounting flange.

PINNING

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

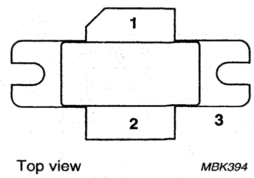


Fig.1 Simplified outline SOT502A.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
Two-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	90 (PEP)	>10.5	>30	≤−25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	DC drain current	–	12	A
T_{stg}	storage temperature	−65	+150	°C
T_j	junction temperature	–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C; P_{tot} = 92 W; note 1	0.81	K/W

Note

1. Determined under specified RF operating conditions, based on maximum junction temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 2.1 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 210 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	15	μA
I_{DSX}	on-state drain current	V_{GS} =V_{GSth} + 9 V; V_{DS} = 10 V	27	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	38	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	–	6.0	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 7.5 A	–	0.11	–	Ω
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz; note 1	–	5.1	–	pF

Note

1. The value of capacitance is that of the die only.

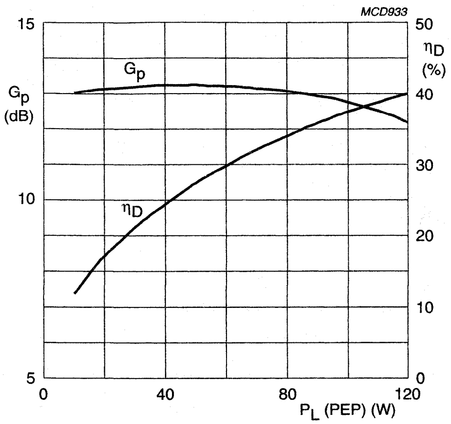
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 0.81 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
Two-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	525	90 (PEP)	>10.5	>30	≤−25

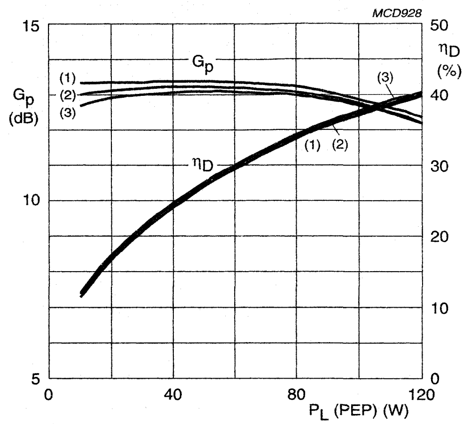
Ruggedness in class-AB operation

The BLF2047L/90 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; I_{DQ} = 525 mA; P_L = 90 W; f = 2000 MHz (single tone).



V_{DS} = 26 V; I_{DQ} = 525 mA; T_h ≤ 25 °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.2 Power gain and drain efficiency as functions of peak envelope load power; typical values.



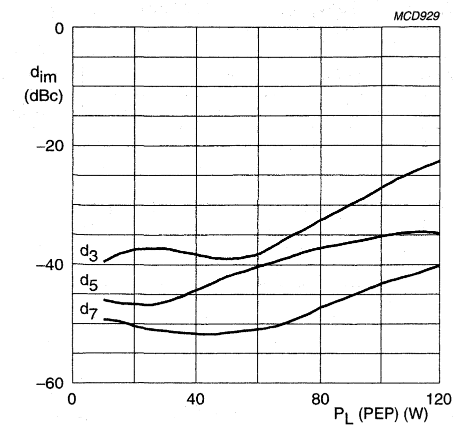
V_{DS} = 26 V; T_h ≤ 25 °C; f_1 = 2000 MHz; f_2 = 2000.1 MHz.

(1) I_{DQ} = 650 mA.

(2) I_{DQ} = 525 mA.

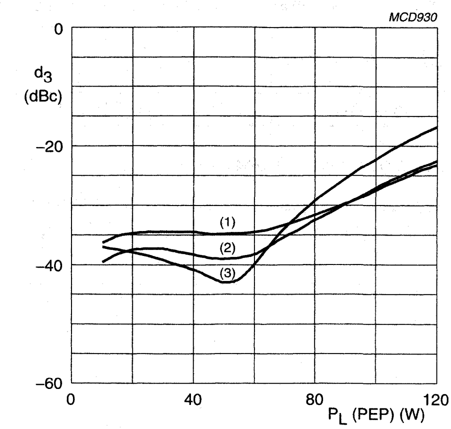
(3) I_{DQ} = 400 mA.

Fig.3 Power gain and drain efficiency as functions of peak envelope load power; typical values.



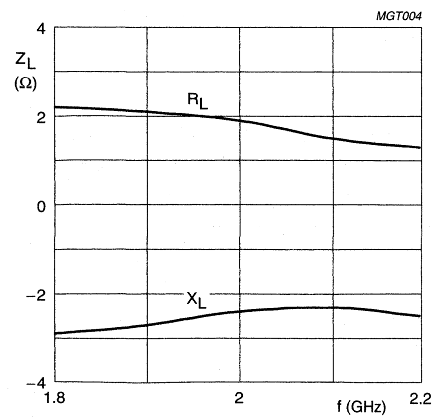
V_{DS} = 26 V; I_{DQ} = 525 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.4 Intermodulation distortion products as functions of peak envelope load power; typical values.



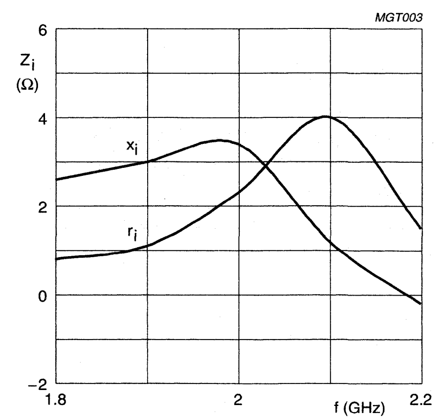
V_{DS} = 26 V; $T_h \leq 25$ °C; f_1 = 2000 MHz; f_2 = 2000.1 MHz.
(1) I_{DQ} = 400 mA.
(2) I_{DQ} = 525 mA.
(3) I_{DQ} = 650 mA.

Fig.5 Third-order intermodulation distortion as a function of peak envelope load power; typical values.



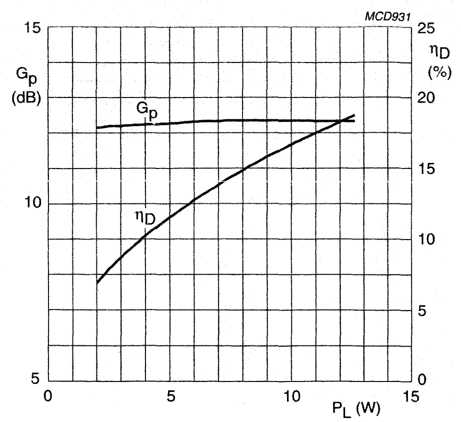
V_{DS} = 26 V; I_D = 525 mA; P_L = 90 W; $T_h \leq 25$ °C.

Fig.6 Load impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_D = 525 mA; P_L = 90 W; $T_h \leq 25$ °C.

Fig.7 Input impedance as a function of frequency (series components); typical values.

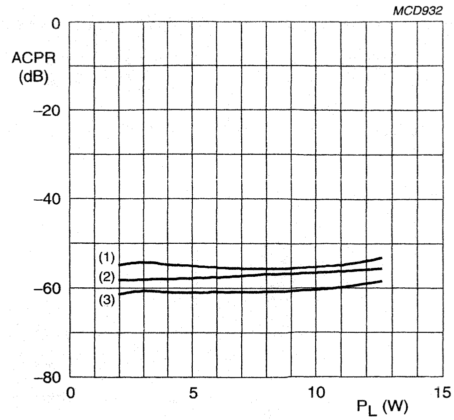


V_{DS} = 26 V; I_{DQ} = 465 mA; $T_h \leq 25$ °C; f = 1 960 MHz; CDMA mode.

CDMA conditions

CHANNEL	WALSH CODE
Pilot	0
Sync	32
Paging	1
Traffic	8 to 13

Fig.8 Power gain and drain efficiency as functions of average load power; typical values.



V_{DS} = 26 V; I_{DQ} = 465 mA; $T_h \leq 25$ °C; f = 1 960 MHz; CDMA mode.

(1) Channel spacing/Bandwidth: 2.25 MHz/1 MHz.

(2) Channel spacing/Bandwidth: 1.25 MHz/12.5 kHz.

(3) Channel spacing/Bandwidth: 885 kHz/30 kHz.

CDMA conditions

CHANNEL	WALSH CODE
Pilot	0
Sync	32
Paging	1
Traffic	8 to 13

Fig.9 Adjacent channel power reduction as a function of average load power; typical values.

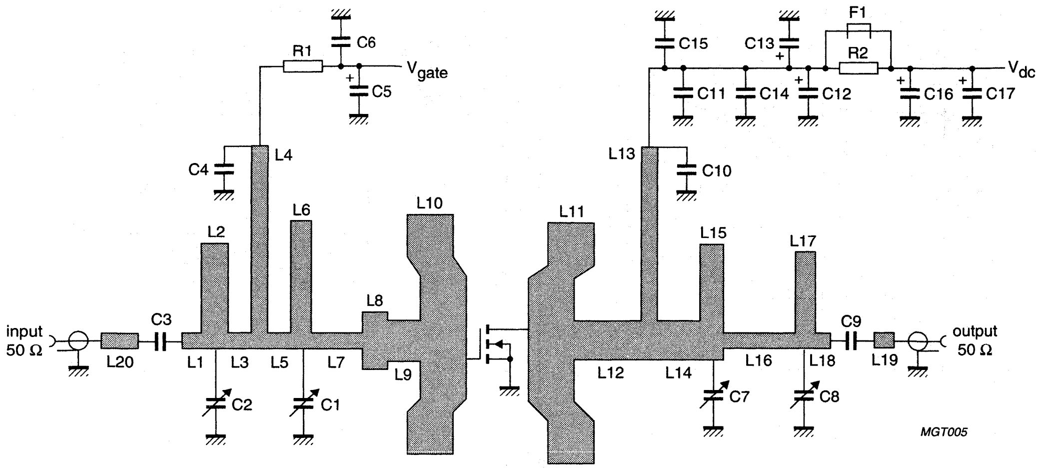


Fig.10 2 GHz class-AB test circuit.

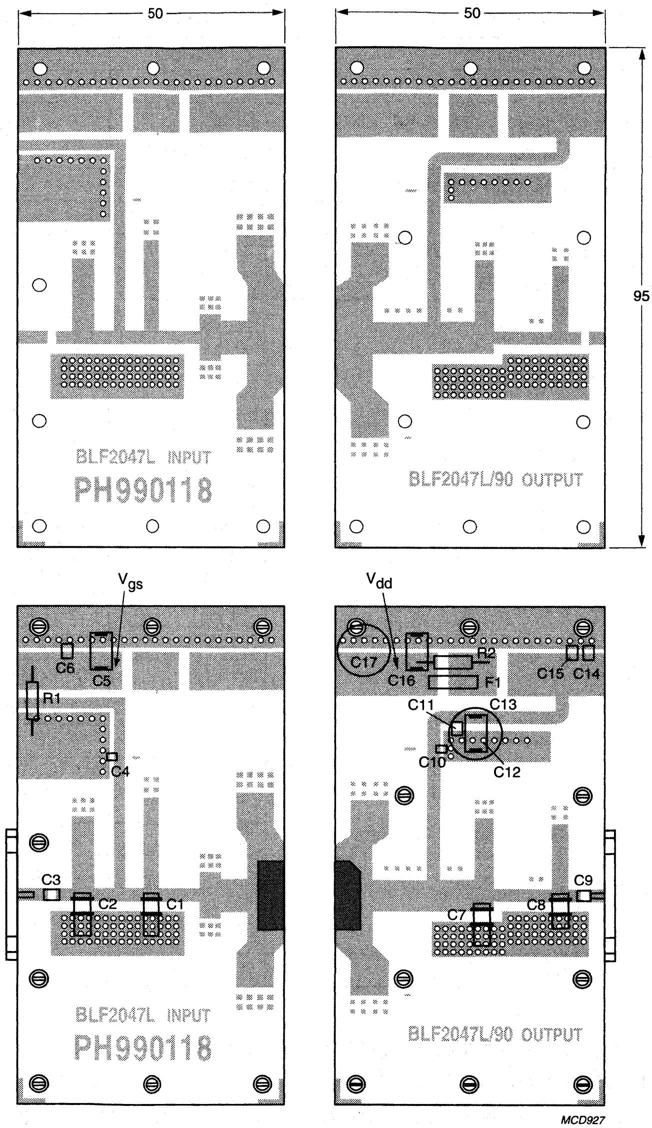
List of components

See Figs 10 and 11.

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7, C8	Tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C3, C9	multilayer ceramic chip capacitor; note 1	12 pF		
C4, C10	multilayer ceramic chip capacitor; note 2	12 pF		
C5, C12, C16	electrolytic capacitor	4.5 μF; 50 V		
C6, C11, C15	multilayer ceramic chip capacitor; note 1	1 nF		
C13, C17	electrolytic capacitor	100 μF; 63 V		2222 037 58101
C14	multilayer ceramic chip capacitor	100 nF		2222 581 16641
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	2.9 × 2.4 mm	
L2		10.8 Ω	4 × 16.3 mm	
L3		50 Ω	3.7 × 2.4 mm	
L4		6 Ω	2 × 30.8 mm	
L5		50 Ω	3.6 × 2.4 mm	
L6		9 Ω	3 × 19.9 mm	
L7		50 Ω	7.8 × 2.4 mm	
L8		18.5 Ω	4 × 8.8 mm	
L9		24.4 Ω	5 × 6.3 mm	
L10		5.1 Ω	7 × 37 mm	
L11		5.1 Ω	7 × 40.9 mm	
L12		25.4 Ω	10.1 × 6 mm	
L13		5.7 Ω	2.4 × 32.8 mm	
L14		25.4 Ω	6.4 × 6 mm	
L15		10 Ω	3.5 × 20.7 mm	
L16		50 Ω	10.8 × 2.4 mm	
L17		11.8 Ω	3 × 7.9 mm	
L18		50 Ω	2.3 × 2.4 mm	
L19		50 Ω	3 × 2.4 mm	
L20		50 Ω	5.5 × 2.4 mm	
R1, R2	metal film resistor	10 Ω, 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric ($\varepsilon_r = 2.2$); thickness 0.79 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.11 Component layout for 2 GHz class-AB test circuit.

UHF push-pull power LDMOS transistor — BLF2048

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 2.2 GHz).

APPLICATIONS

- Common source class-AB operation for PCN and PCS applications in the 1800 to 2200 MHz frequency range.

DESCRIPTION

Push-pull silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 4-lead flange package (SOT539A) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT539A

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source connected to flange

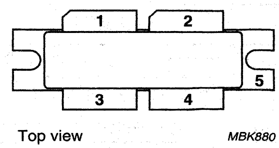


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2200; f_2 = 2200.1	26	120 (PEP)	>10	>30	≤−26
		28	140 (PEP)	typ. 11.2	typ. 31	typ. −25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	drain current (DC)	–	18	A
T_{stg}	storage temperature	−65	+150	°C
T_j	junction temperature	–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	P_L = 120 W; T_{mb} = 50 °C, note 1	0.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink		0.15	K/W

Note

1. Thermal resistance is determined under nominal 2-tone RF operating conditions.

CHARACTERISTICS

T_j = 25 °C; per section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.4 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 140 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	10	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	18	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	250	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	–	4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 5 A	–	0.17	–	Ω
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz; note 1	–	3.4	–	pF

Note

1. Capacitance of die only.

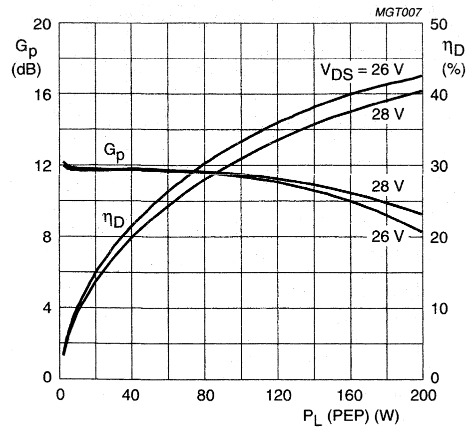
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 0.5 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2200; f_2 = 2200.1	26	2 x 400	120 (PEP)	>10	>30	≤–26
		28	2 x 400	140 (PEP)	typ. 11.2	typ. 31	typ. –25

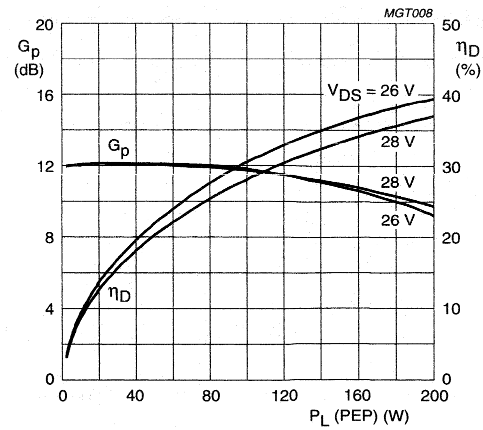
Ruggedness in class-AB operation

The BLF2048 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 2200 MHz, P_L = 120 W (CW).



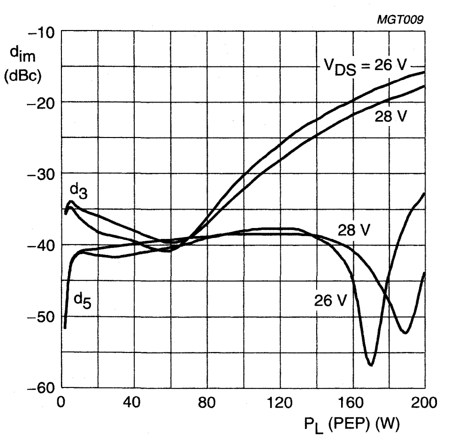
f_1 = 2000 MHz; f_2 = 2000.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.2 Power gain and drain efficiency as functions of peak envelope load power; typical values.



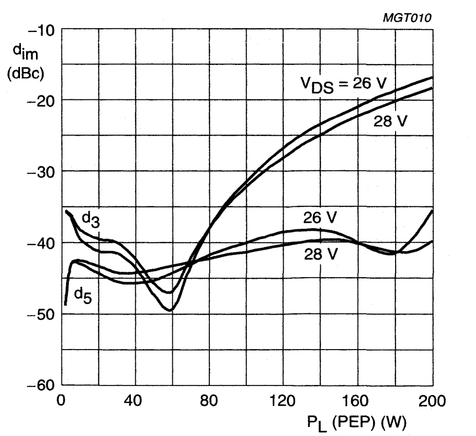
f_1 = 2200 MHz; f_2 = 2200.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.3 Power gain and drain efficiency as functions of peak envelope load power; typical values.



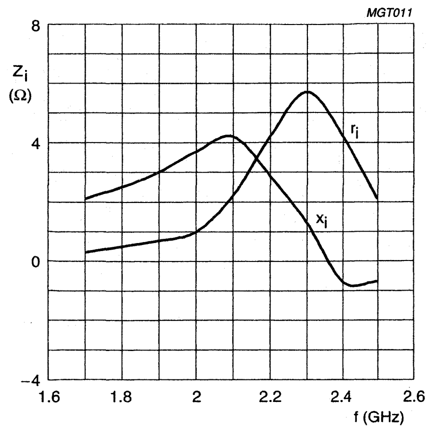
f_1 = 2000 MHz; f_2 = 2000.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.4 Intermodulation distortion as a function of peak envelope load power; typical values.



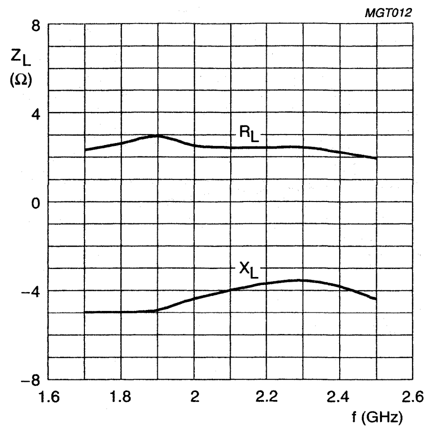
f_1 = 2200 MHz; f_2 = 2200.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.5 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 2 x 400 mA; P_L = 160 W (total device);
$T_h \leq 25$ °C.

Fig.6 Input impedance per section as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 2 x 400 mA; P_L = 160 W (total device);
$T_h \leq 25$ °C.

Fig.7 Load impedance per section as a function of frequency (series components); typical values.

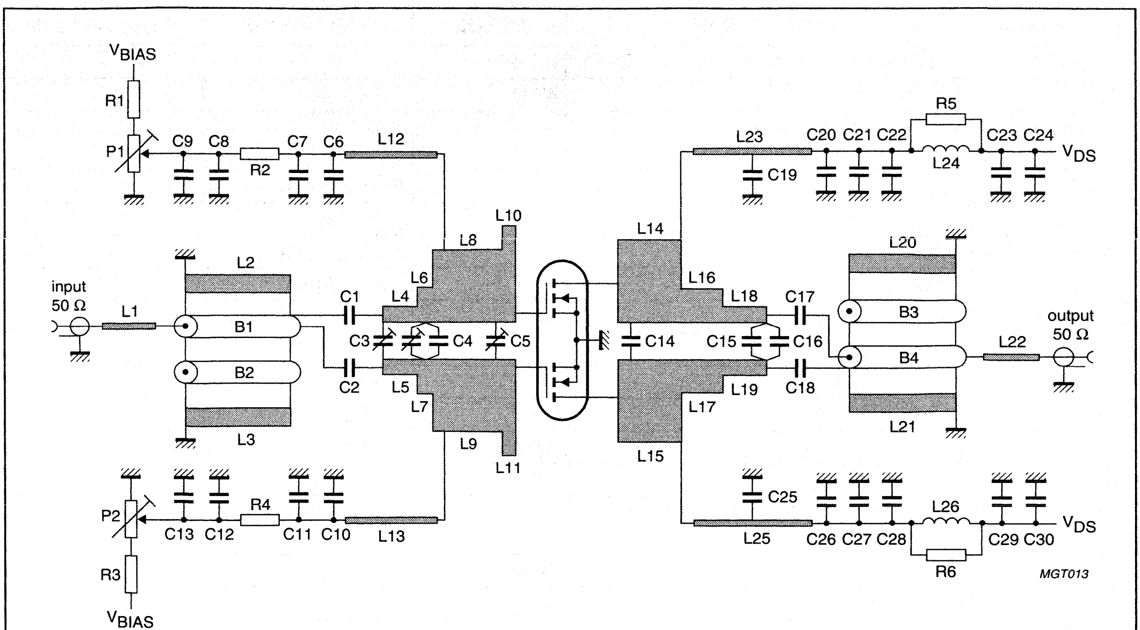


Fig.8 2.2 GHz class-AB test circuit.

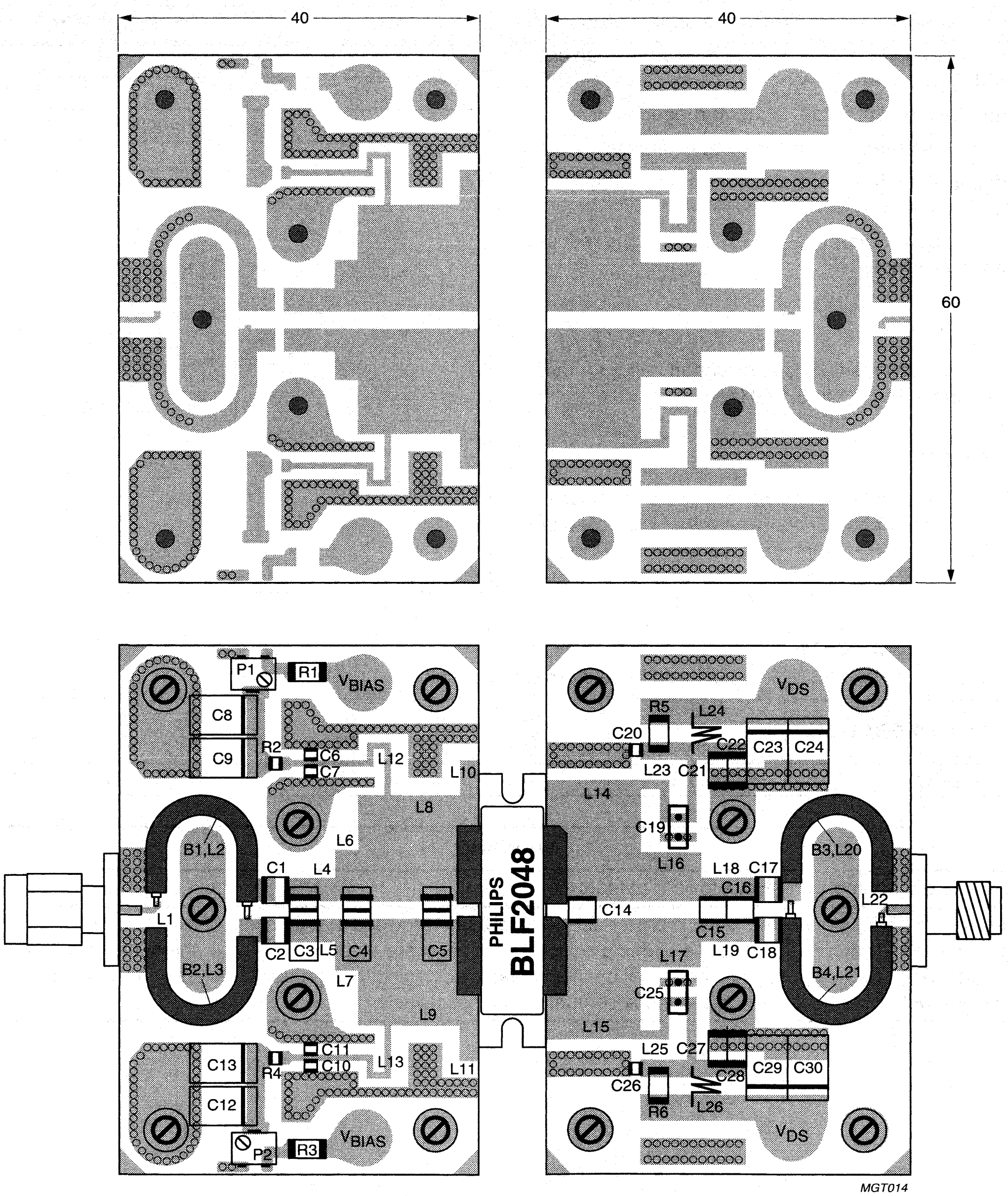
List of components (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	5.1 pF		
C3, C5	Tekelec variable capacitor	0.6 to 4.5 pF		
C4	Tekelec variable capacitor + multilayer ceramic chip capacitor; note 1	0.6 to 4.5 pF + 2.4 pF		
C6, C10	multilayer ceramic chip capacitor; note 2	100 pF		
C7, C11	multilayer ceramic chip capacitor; note 2	18 pF		
C8, C12, C23, C29	tantalum SMD capacitor	4.7 μF; 35 V		
C9, C13, C24, C30	tantalum SMD capacitor	10 μF; 35 V		
C14	multilayer ceramic chip capacitor; note 3	0.5 pF		
C15	multilayer ceramic chip capacitor; note 3	1 pF		
C16	multilayer ceramic chip capacitor; note 1	1.5 pF		
C17, C18	multilayer ceramic chip capacitor; note 1	10 pF		
C19, C25	MKT ceramic chip capacitor	33 nF		2222 370 11333
C20, C26	multilayer ceramic chip capacitor; note 2	6.2 pF		
C21, C27	multilayer ceramic chip capacitor	100 nF		2222 581 16641

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C22, C28	multilayer ceramic chip capacitor; note 1	8.2 pF		
L1	stripline; note 4	47 Ω	4.5 × 1 mm	
L2, L3, L20, L21	stripline; note 4		15 × 2 mm	
L4, L5	stripline; note 4		5.6 × 2.6 mm	
L6, L7	stripline; note 4		2.6 × 5.8 mm	
L8, L9	stripline; note 4		11.5 × 12 mm	
L10, L11	stripline; note 4		2.2 × 16 mm	
L12, L13	stripline; note 4	57 Ω	1/4 λ at 2.2 GHz	
L14, L15	stripline; note 4		10.4 × 13.7 mm	
L16, L17	stripline; note 4		6.6 × 5.5 mm	
L18, L19	stripline; note 4		7 × 2.6 mm	
L22	stripline; note 4	47 Ω	4 x 1 mm	
L23, L25	stripline; note 4	47 Ω	1/4 λ at 2.2 GHz	
L24, L26	1 turn enamelled 0.7 mm copper wire		int.dia. 7 mm; length: tbf	
B1, B4	balun of semi-rigid cable	50 Ω		
B2, B3	semi-rigid cable; note 5	50 Ω		
R1, R3, R5, R6	metal film resistor	5.6 Ω, 0.6 W		
R2, R4	metal film resistor	10 Ω, 0.6 W		
P1, P2	variable resistor (multiturn)	5 kΩ		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. Semi-rigid cable soldered along the stub to establish balance.
5. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (εr = 6.15); thickness 0.64 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15), thickness 0.64 mm. The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 2.2 GHz class-AB test circuit.

Microwave power transistor BLS2731-10

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifier for radar applications in the 2.7 to 3.1 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT445C) with the common base connected to the flange.

PINNING - SOT445C

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange

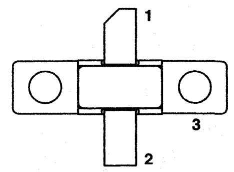


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed class-C	2.7 to 3.1	40	12.5	typ. 10	typ. 45

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100\ \mu s$; $\delta \leq 10\%$	–	1.5	A
P_{tot}	total power dissipation	$t_p = 100\ \mu s$; $\delta = 10\%$; $T_{mb} = 25\ °C$	–	145	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100\ \mu s$; $\delta = 10\%$; note 1	1.2	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

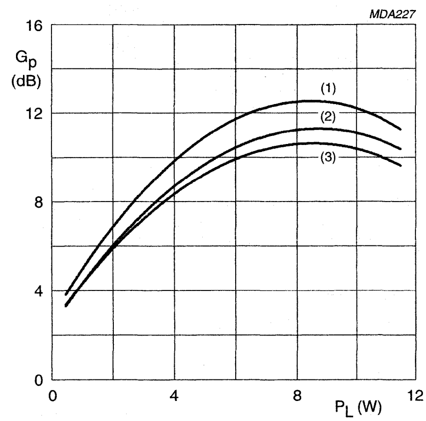
$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 2.5$ mA; open emitter	75	–	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 2.5$ mA; $V_{BE} = 0$	75	–	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	–	0.3	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	–	0.5	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	–	0.1	mA
h_{FE}	DC current gain	$V_{CE} = 5$ V; $I_C = 0.25$ A	40	–	–	
C_c	collector capacitance (die only)	$V_{CE} = 1$ V; $I_E = i_e = 0$; $f = 1$ MHz	–	10	–	pF

APPLICATION INFORMATION

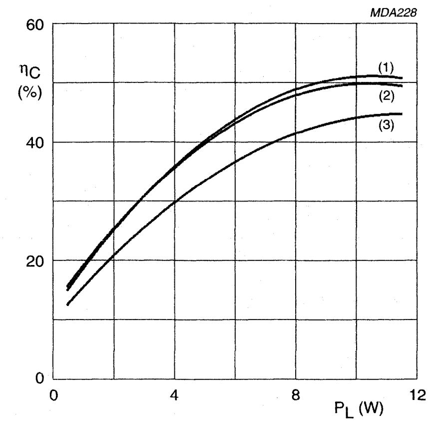
RF performance at T_h = 25 °C in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
Class-C; t_p = 100 μs; δ = 10%	2.7 to 3.1	40	≥10 typ. 12.5	≥9 typ. 10	≥35 typ. 45



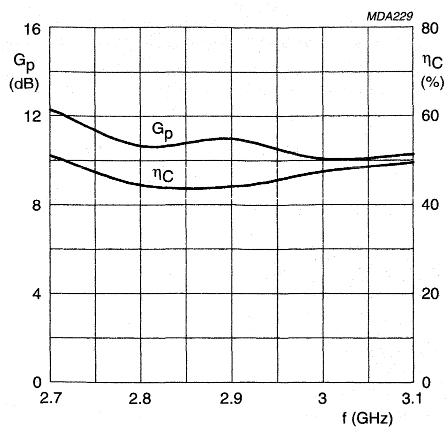
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 2.7 GHz.
(2) f = 2.9 GHz.
(3) f = 3.1 GHz.

Fig.2 Power gain as a function of load power; typical values.



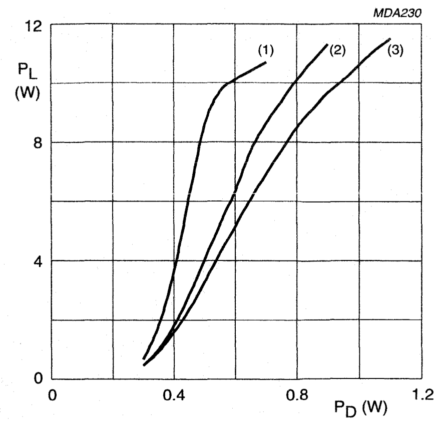
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 2.7 GHz.
(2) f = 3.1 GHz.
(3) f = 2.9 GHz.

Fig.3 Collector efficiency as a function of load power; typical values.



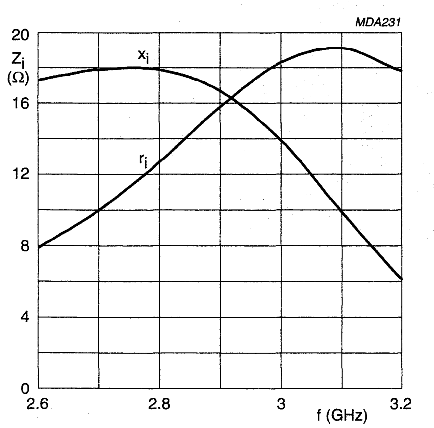
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.

Fig.4 Power gain and efficiency as functions of frequency; typical values.



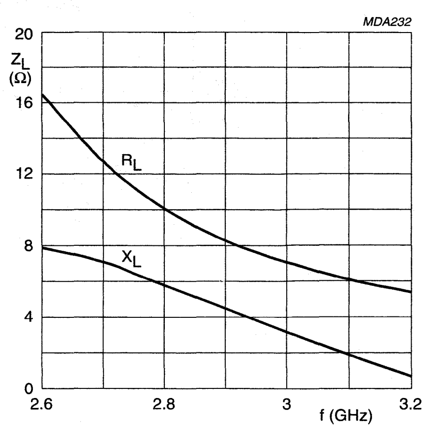
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 2.7 GHz.
(2) f = 2.9 GHz.
(3) f = 3.1 GHz.

Fig.5 Load power as a function of drive power; typical values.



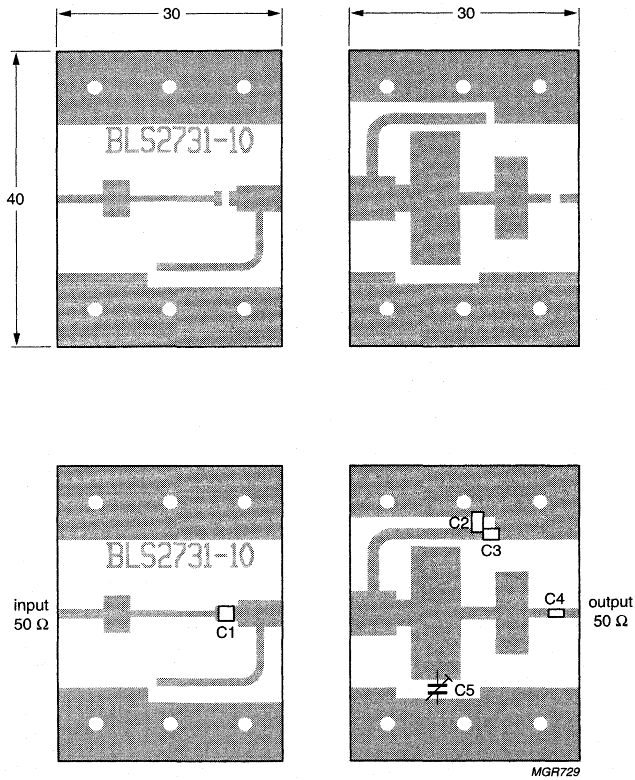
V_{CB} = 40 V; class-C; P_L = 10 W.

Fig.6 Input impedance as function of frequency (series components); typical values.



V_{CB} = 40 V; class-C; P_L = 10 W.

Fig.7 Load impedance as function of frequency (series components); typical values.



Dimensions in mm.

The components are located on one side of the copper-clad printed circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

The striplines are on double-clad printed-circuit board with Duroid dielectric (ε_r = 2.2); thickness = 0.38 mm.

Fig.8 Component layout for 2.7 to 3.1 GHz class-C test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE
C1	multilayer ceramic chip capacitor; note 1	0.7 nF
C2	multilayer ceramic chip capacitor; note 2	1 nF
C3	multilayer ceramic chip capacitor; note 1	10 pF
C4	multilayer ceramic chip capacitor; note 3	150 pF
C5	Tekelec trimmer type 37281SL	0.4 to 2.5 pF

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 200A or capacitor of same quality.
3. American Technical Ceramics type 700A or capacitor of same quality.

Microwave power transistor | BLS2731-20

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifiers for radar applications in the 2.7 to 3.1 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT445C) with the common base connected to the flange.

PINNING - SOT445C

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

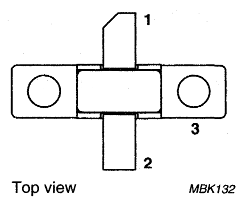


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed class-C	2.7 to 3.1	40	25	typ. 10	typ. 40

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100\ \mu s$; $\delta \leq 10\%$	–	3	A
P_{tot}	total power dissipation	$t_p = 100\ \mu s$; $\delta = 10\%$; $T_{mb} = 25\ °C$	–	270	W
T_{stg}	storage temperature		−65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100\ \mu s$; $\delta = 10\%$; note 1	0.65	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

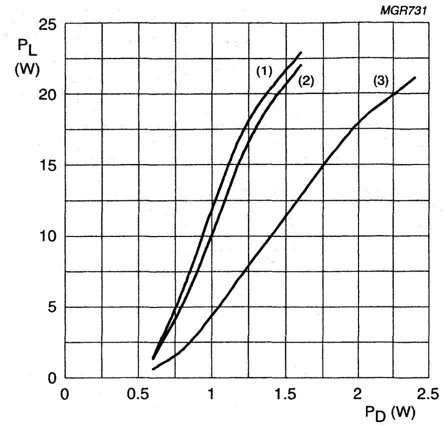
$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 5$ mA; open emitter	75	–	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 5$ mA; $V_{BE} = 0$	75	–	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	–	0.5	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	–	0.5	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	–	0.1	mA
h_{FE}	DC current gain	$V_{CB} = 5$ V; $I_C = 0.5$ A	40	–	–	
C_c	collector capacitance (die only)	$V_{CE} = 1$ V; $I_E = i_e = 0$; f = 1 MHz	–	10	–	pF

APPLICATION INFORMATION

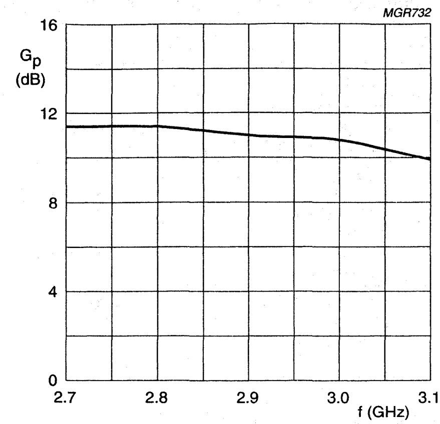
RF performance at $T_h = 25\ °C$ in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
Class-C; $t_p = 100\ \mu s$; $\delta = 10\%$	2.7 to 3.1	40	≥20 typ. 25	≥9 typ. 10	≥35 typ. 40



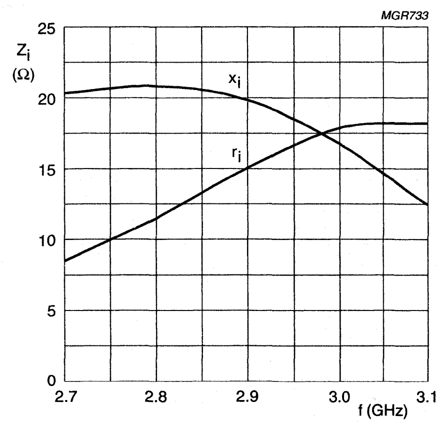
V_{CB} = 40 V; class-C; t_p = 100 µs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 2.7 GHz.
(3) f = 2.9 GHz.

Fig.2 Load power as a function of drive power; typical values.



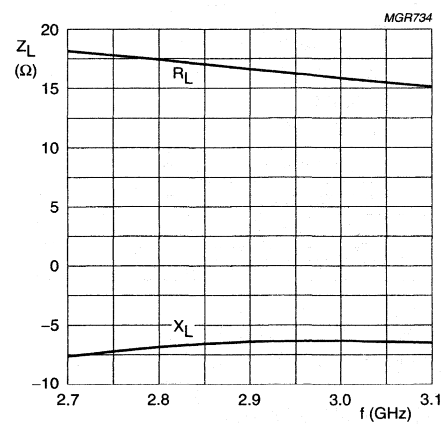
V_{CB} = 40 V; class-C; P_L = 20 W; t_p = 100 µs; δ = 10%.

Fig.3 Power gain as function of frequency; typical values.



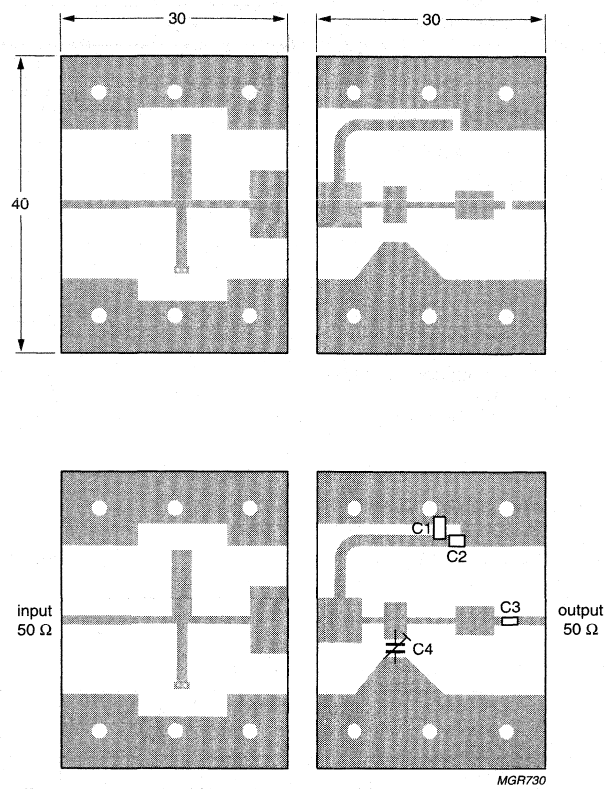
V_{CB} = 40 V; class-C; P_L = 20 W.

Fig.4 Input impedance as function of frequency (series components); typical values.



V_{CB} = 40 V; class-C; P_L = 20 W.

Fig.5 Load impedance as function of frequency (series components); typical values.



Dimensions in mm.

The components are located on one side of the copper-clad printed circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

The striplines are on double-clad printed-circuit board with Duroid dielectric (ε_r = 2.2); thickness = 0.38 mm.

Fig.6 Component layout for 2.7 to 3.1 GHz class-C test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE
C1	multilayer ceramic chip capacitor; note 1	1 nF
C2	multilayer ceramic chip capacitor; note 2	10 pF
C3	multilayer ceramic chip capacitor; note 3	150 pF
C4	Tekelec trimmer type 37281SL	0.4 to 2.5 pF

Notes

1. American Technical Ceramics type 200A or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. American Technical Ceramics type 700A or capacitor of same quality.

Microwave power transistor

BLS2731-50

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifiers for radar applications in the 2.7 to 3.1 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT422A) with the common base connected to the flange.

PINNING - SOT422A

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange

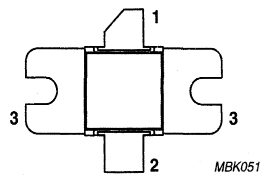


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed, class-C	2.7 to 3.1	40	60	typ. 9	typ. 40

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100\ \mu s$; $\delta \leq 10\%$	–	6	A
P_{tot}	total power dissipation	$t_p = 100\ \mu s$; $\delta = 10\%$; $T_{mb} = 25\ °C$	–	80	W
T_{stg}	storage temperature		−65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100\ \mu s$; $\delta = 10\%$; note 1	0.3	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

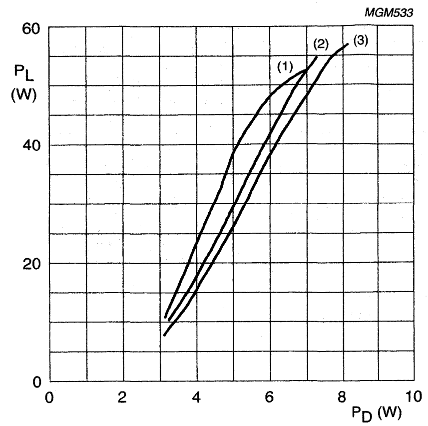
$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 15$ mA; open emitter	75	–	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 15$ mA; $V_{BE} = 0$	75	–	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	–	1.5	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	–	3	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	–	0.3	mA
h_{FE}	DC current gain	$V_{CB} = 5$ V; $I_C = 1.5$ A	40	–	–	
C_c	collector capacitance (die only)	$V_{CE} = 1$ V; $I_E = i_e = 0$; f = 1 MHz	–	30	–	pF

APPLICATION INFORMATION

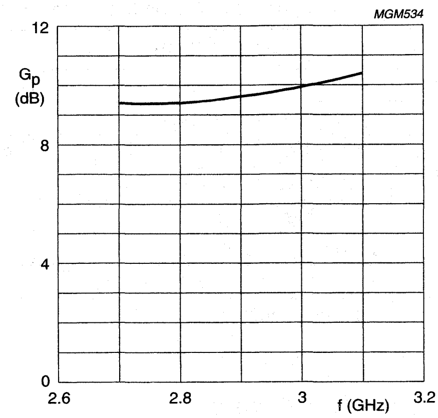
RF performance at $T_h = 25\ °C$ in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
Class-C; $t_p = 100\ \mu s$; $\delta = 10\%$	2.7 to 3.1	40	≥50 typ. 60	≥8 typ. 9	≥35 typ. 40



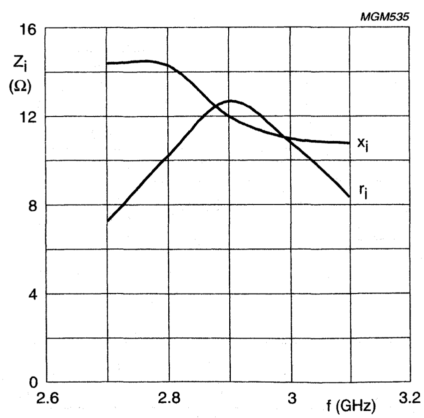
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 2.7 GHz.
(3) f = 2.9 GHz.

Fig.2 Load power as a function of drive power; typical values.



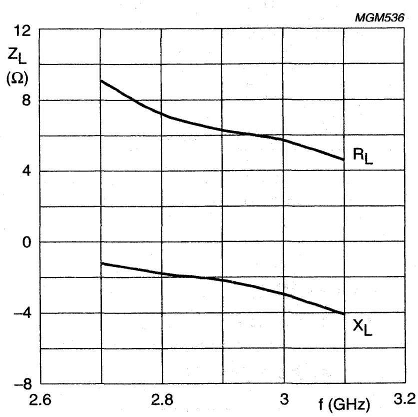
V_{CB} = 40 V; class-C; P_L = 50 W; t_p = 100 μs; δ = 10%.

Fig.3 Power gain as function of frequency; typical values.



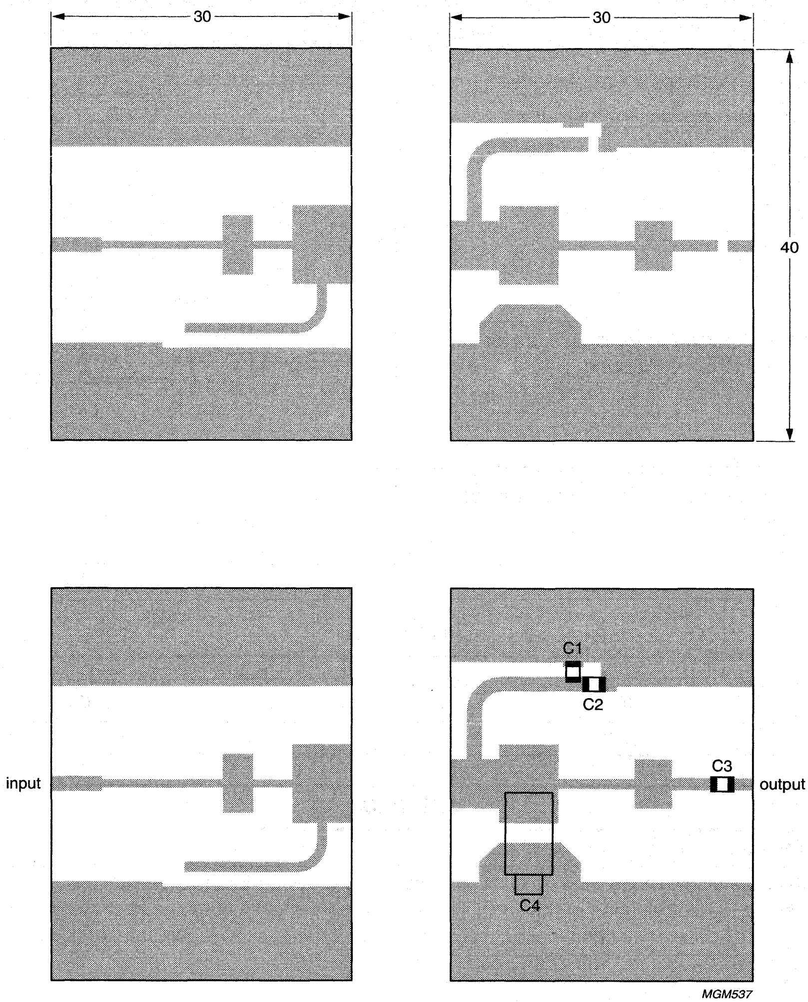
V_{CB} = 40 V; class-C; P_L = 50 W.

Fig.4 Input impedance as function of frequency (series components); typical values.



V_{CB} = 40 V; class-C; P_L = 50 W.

Fig.5 Load impedance as function of frequency (series components); typical values.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Duroid dielectric (ε_r = 2.2), thickness 0.38 mm. The other side is unetched and serves as a ground plane.

C1 = ATC 200A 10 nF
C2 = ATC 100A 10 pF
C3 = ATC 700A 150 pF
C4 = Tekelec trimmer 37281SL 0.4 to 2.5 pF.

Fig.6 Component layout for 2.7 to 3.1 GHz class-C test circuit.

Microwave power transistor BLS2731-110

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifiers for radar applications in the 2.7 to 3.1 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT423A) with the common base connected to the flange.

PINNING - SOT423A

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange

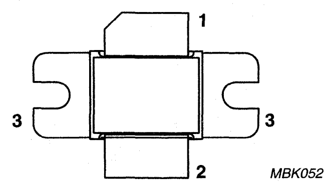


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed class-C	2.7 to 3.1	40	>110	>7	>35

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100\ \mu s$; $\delta \leq 10\%$	–	12	A
P_{tot}	total power dissipation	$t_p = 100\ \mu s$; $\delta = 10\%$; $T_{mb} = 25\ °C$	–	500	W
T_{stg}	storage temperature		−65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100\ \mu s$; $\delta = 10\%$; note 1	0.24	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

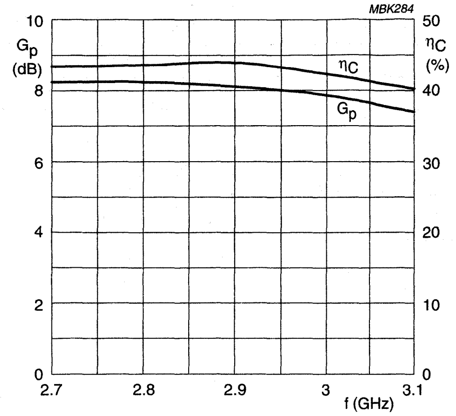
$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 30$ mA; open emitter	75	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 30$ mA; $V_{BE} = 0$	75	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	3	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	6	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	0.6	mA
h_{FE}	DC current gain	$V_{CE} = 5$ V; $I_C = 3$ A	40	100	

APPLICATION INFORMATION

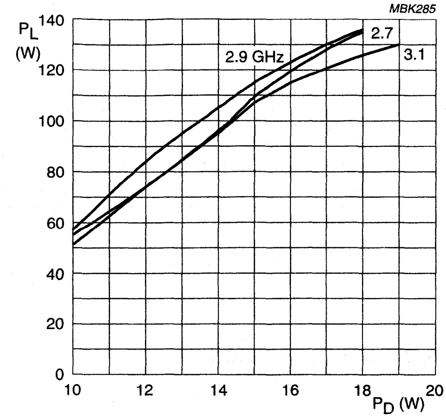
RF performance at $T_h = 25\ °C$ in a common base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_P (dB)	η_C (%)
Class-C; $t_p = 100\ \mu s$; $\delta = 10\%$	2.7 to 3.1	40	≥110	≥7	≥35
	2.7 to 2.9	40	typ. 130	typ. 8	typ. 42
	2.9 to 3.1	40	typ. 120	typ. 7.5	typ. 40



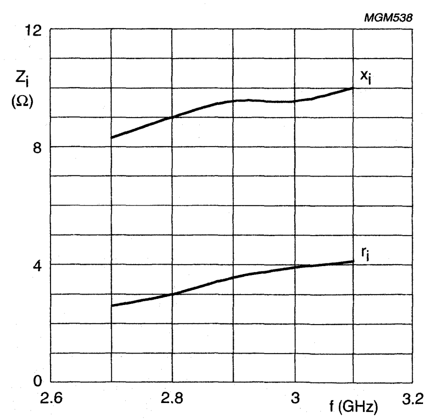
V_{CE} = 40 V; class-C; t_p = 100 μs; δ = 10%.

Fig.2 Power gain and efficiency as functions of frequency; typical values.



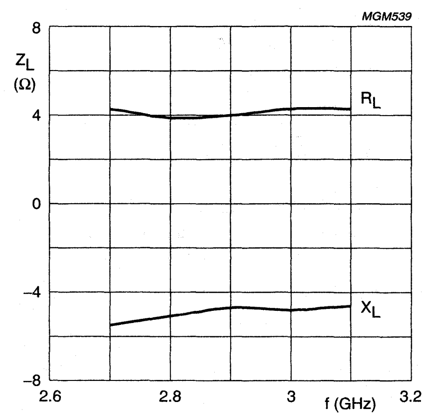
V_{CE} = 40 V; class-C; t_p = 100 μs; δ = 10%.

Fig.3 Load power as a function of drive power; typical values.



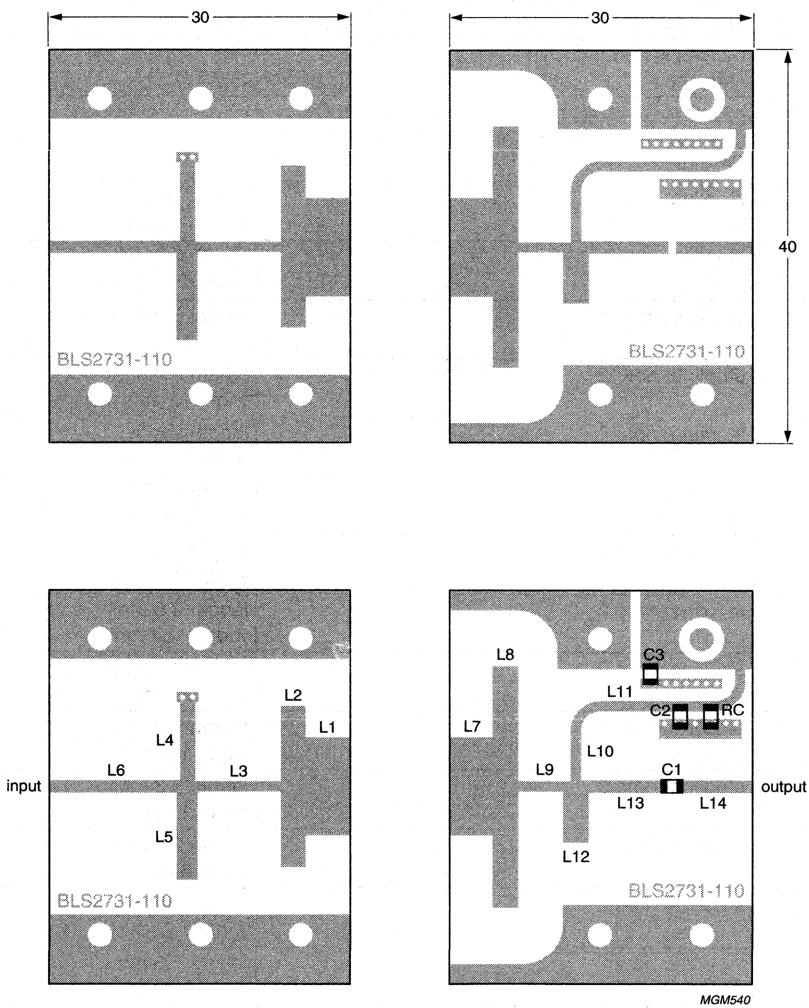
V_{CB} = 40 V; class-C; P_L = 110 W.

Fig.4 Input impedance as function of frequency (series components); typical values.



V_{CB} = 40 V; class-C; P_L = 110 W.

Fig.5 Load impedance as function of frequency (series components); typical values.



Dimensions in mm.

The components are located on one side of the copper-clad printed-circuit board, the other side is unetched and serves as a ground plane.
Earth connections from the component side to the ground plane are made by through metallization.

Fig.6 Component layout for 2.7 to 3.1 GHz class-C test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor; note 1	100 pF		
C3	multilayer ceramic chip capacitor	100 nF		
RC	multilayer ceramic chip capacitor in series with SMD resistor	100 nF + 5 Ω		
L1	stripline; note 2		length 4.5 mm width 10 mm	
L2	stripline; note 2		length 2.5 mm width 16.4 mm	
L3	stripline; note 2		length 8.3 mm width 1 mm	
L4	stripline; note 2		length 8 mm width 1.5 mm	
L5	stripline; note 2		length 2 mm width 8.9 mm	
L6	stripline; note 2		length 12.7 mm width 1.2 mm	
L7	stripline; note 2		length 4.5 mm width 10 mm	
L8	stripline; note 2		length 2.5 mm width 24.4 mm	
L9	stripline; note 2		length 4.4 mm width 1 mm	
L10	stripline; note 2		length 5.2 mm width 1 mm	
L11	stripline; note 2		length 9.3 mm width 1 mm	
L12	stripline; note 2		length 2.5 mm width 6 mm	
L13	stripline; note 2		length 7.8 mm width 1.2 mm	
L14	stripline; note 2		length 7.5 mm width 1.2 mm	

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on double-clad printed-circuit board with Duroid dielectric (ε_r = 2.2); thickness = 0.38 mm.

Microwave power transistor BLS3135-10

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifier for radar applications in the 3.1 to 3.5 GHz range.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT445C) with the common base connected to the flange.

PINNING - SOT445C

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange

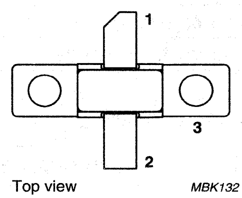


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed class-C	3.1 to 3.5	40	≥10	typ. 9	typ. 40

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100$ µs; $\delta \leq 10\%$	–	1.5	A
P_{tot}	total power dissipation	$t_p = 100$ µs; $\delta = 10\%$; $T_h = 25$ °C	–	34	W
T_{stg}	storage temperature		−65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100$ µs; $\delta = 10\%$; note 1	5.2	K/W
		$t_p = 200$ µs; $\delta = 10\%$; note 1	5.8	K/W
		$t_p = 300$ µs; $\delta = 10\%$; note 1	6.3	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

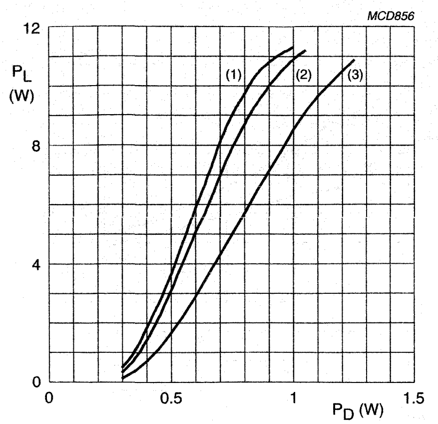
$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 2.5$ mA; open emitter	75	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 2.5$ mA; $V_{BE} = 0$	75	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	0.3	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	0.5	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	0.1	mA
h_{FE}	DC current gain	$V_{CE} = 5$ V; $I_C = 0.25$ A	40	–	

APPLICATION INFORMATION

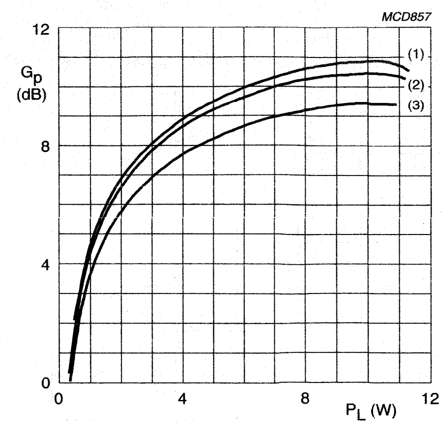
RF performance at $T_h = 25$ °C in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
Class-C; $t_p = 100$ µs; $\delta = 10\%$	3.1 to 3.5	40	≥10	≥7.5 typ. 9	≥35 typ. 40



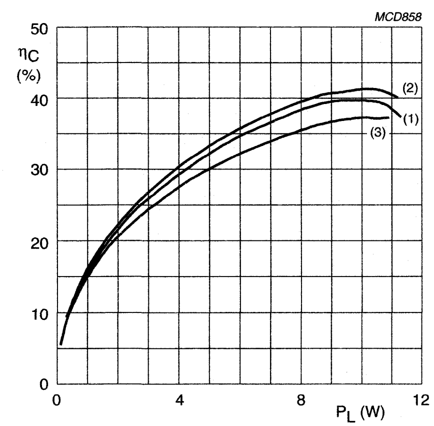
V_{CB} = 40 V; class-C; t_p = 100 µs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.2 Load power as a function of drive power; typical values.



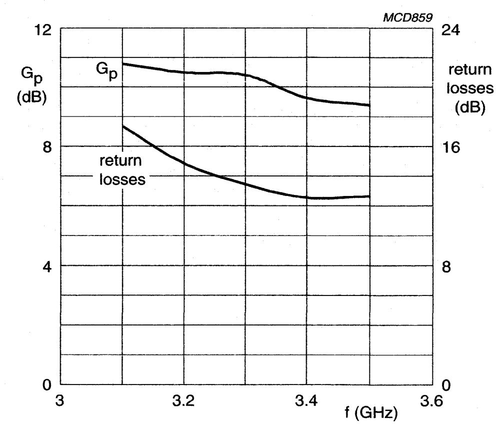
V_{CB} = 40 V; class-C; t_p = 100 µs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.3 Power gain as a function of load power; typical values.



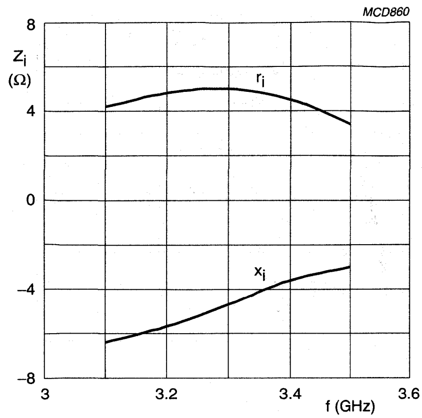
V_{CB} = 40 V; class-C; t_p = 100 µs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.4 Collector efficiency as a function of load power; typical values.



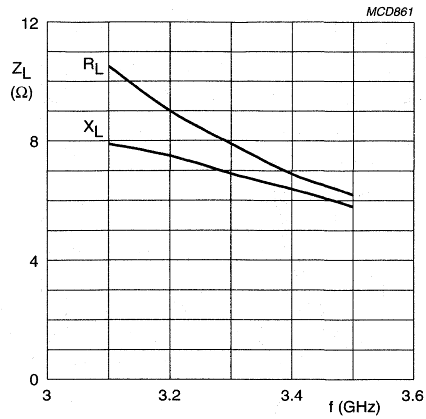
V_{CB} = 40 V; class-C; P_L = 10 W; t_p = 100 µs; δ = 10%.

Fig.5 Power gain and input return losses as functions of frequency; typical values.



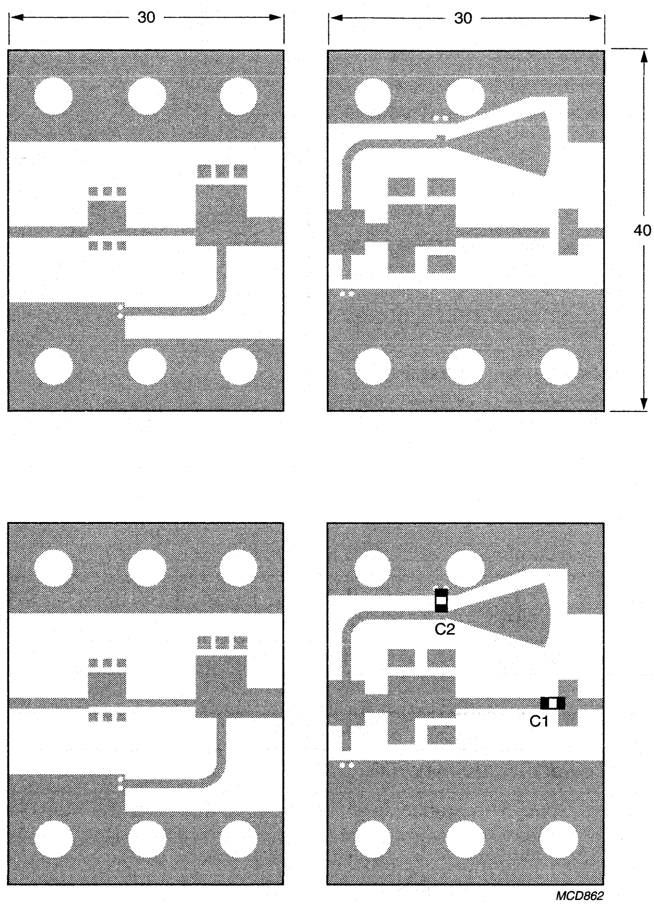
V_{CB} = 40 V; class-C; P_L = 10 W.

Fig.6 Input impedance as a function of frequency (series components); typical values.



V_{CB} = 40 V; class-C; P_L = 10 W.

Fig.7 Load impedance as a function of frequency (series components); typical values.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Duroid dielectric (ε_r = 2.2), thickness 0.38 mm. The other side is unetched and serves as a ground plane.

C1 = 10 pF (ATC 100A); C2 = 100 pF (ATC 100A).

Fig.8 Component layout for 3.1 to 3.5 GHz class-C test circuit.

Microwave power transistor BLS3135-20

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifiers for radar applications in the 3.1 to 3.5 GHz range.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT422A) with the common base connected to the flange.

PINNING - SOT422A

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange

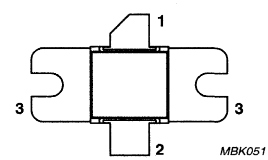


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed, class-C	3.1 to 3.5	40	20	typ. 8	typ. 40

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100$ µs; $\delta \leq 10\%$	–	2	A
P_{tot}	total power dissipation	$t_p = 100$ µs; $\delta = 10\%$; $T_{mb} = 25$ °C	–	80	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100$ µs; $\delta = 10\%$; note 1	2	K/W
		$t_p = 200$ µs; $\delta = 10\%$; note 1	2.45	K/W
		$t_p = 300$ µs; $\delta = 10\%$; note 1	2.75	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

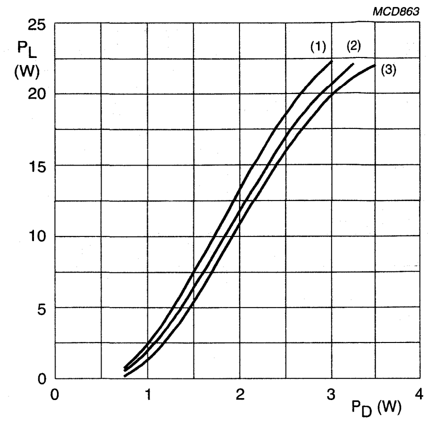
$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 15$ mA; open emitter	75	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 15$ mA; $V_{BE} = 0$	75	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	0.5	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	1	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	0.1	mA
h_{FE}	DC current gain	$V_{CB} = 5$ V; $I_C = 1.5$ A	40	–	

APPLICATION INFORMATION

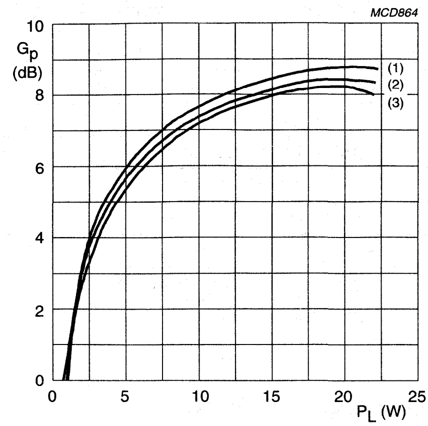
RF performance at $T_h = 25$ °C in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
Class-C; $t_p = 100$ µs; $\delta = 10\%$	3.1 to 3.5	40	≥20 typ. 22	≥7 typ. 8	≥35 typ. 40



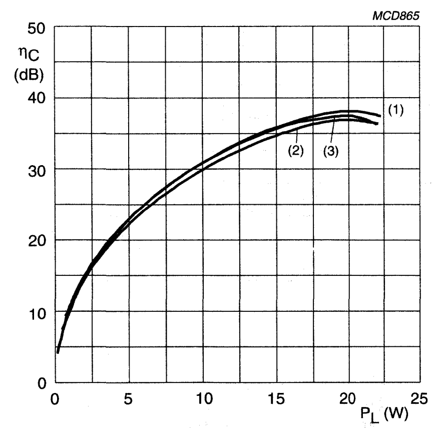
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.2 Load power as a function of drive power; typical values.



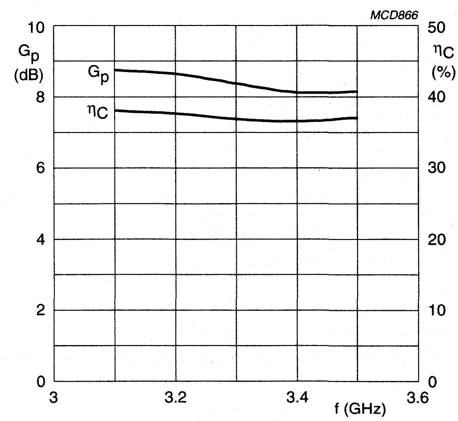
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.3 Power gain as a function of load power; typical values.



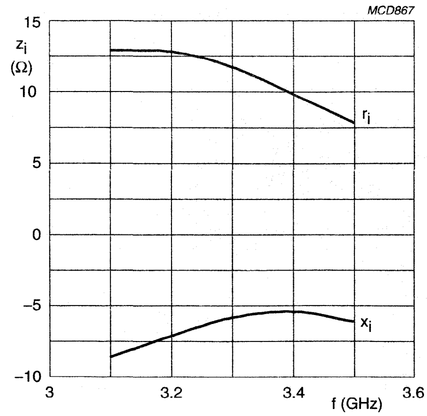
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.4 Collector efficiency as a function of load power; typical values.



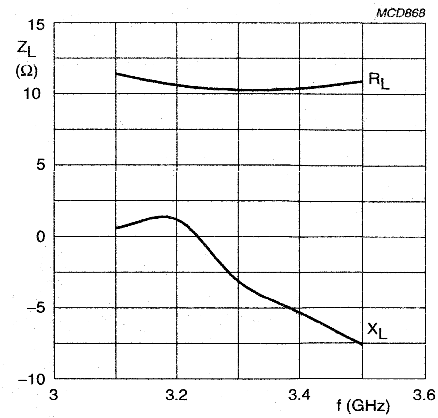
V_{CB} = 40 V; class-C; P_L = 20 W; t_p = 100 μs; δ = 10%.

Fig.5 Power gain and efficiency as functions of frequency; typical values.



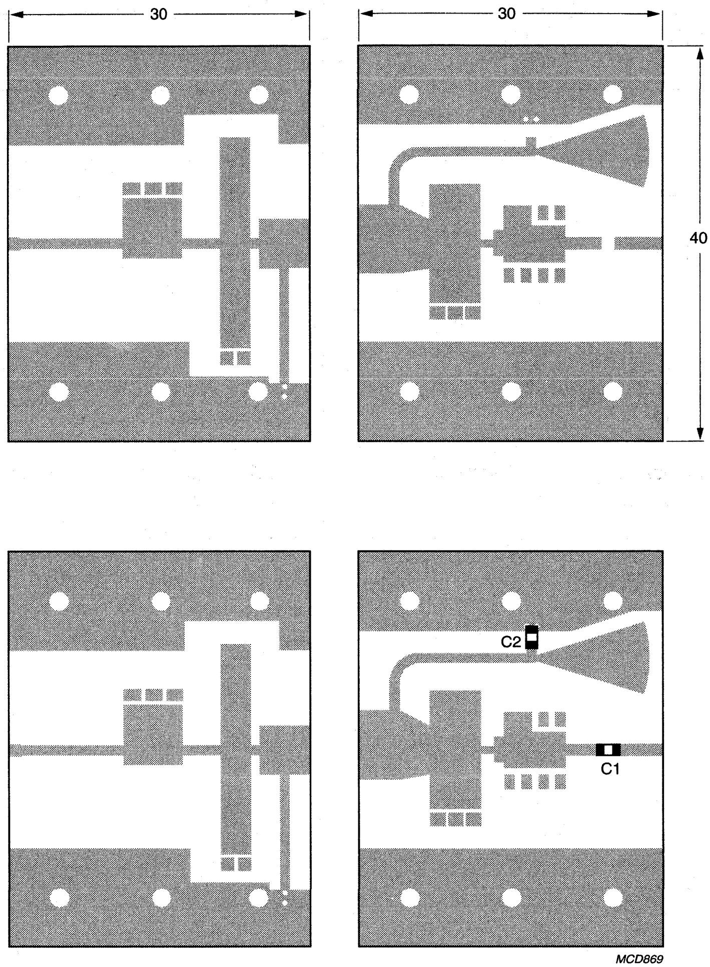
V_{CB} = 40 V; class-C; P_L = 20 W.

Fig.6 Input impedance as a function of frequency (series components); typical values.



V_{CB} = 40 V; class-C; P_L = 20 W.

Fig.7 Load impedance as a function of frequency (series components); typical values.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Duroid dielectric (ε_r = 2.2), thickness 0.38 mm. The other side is unetched and serves as a ground plane.

C1 = C2 = 4.7 pF (ATC 100A).

Fig.8 Component layout for 3.1 to 3.5 GHz class-C test circuit.

Microwave power transistor BLS3135-50

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifiers for radar applications in the 3.1 to 3.5 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT422A) with the common base connected to the flange.

PINNING - SOT422A

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange

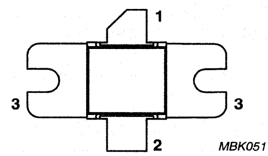


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed, class-C	3.1 to 3.5	40	50	typ. 8	typ. 40

WARNING
Product and environmental safety - toxic materials
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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100\ \mu s$; $\delta \leq 10\%$	–	6	A
P_{tot}	total power dissipation	$t_p = 100\ \mu s$; $\delta = 10\%$; $T_{mb} = 25\ °C$	–	80	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100\ \mu s$; $\delta = 10\%$; note 1	0.71	K/W
		$t_p = 300\ \mu s$; $\delta = 10\%$; note 1	0.99	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions. Measured with IR-scan with 20 μm spotsize at hotspot.

CHARACTERISTICS

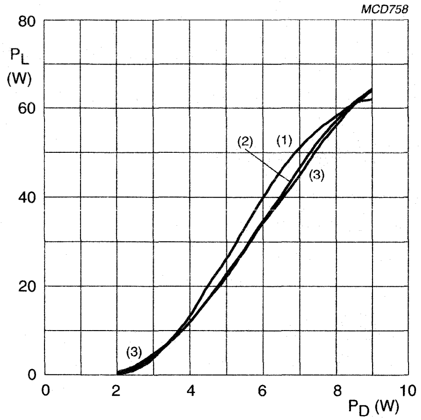
$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 15$ mA; open emitter	75	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 15$ mA; $V_{BE} = 0$	75	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	1.5	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	3	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	0.3	mA
h_{FE}	DC current gain	$V_{CB} = 5$ V; $I_C = 1.5$ A	40	–	

APPLICATION INFORMATION

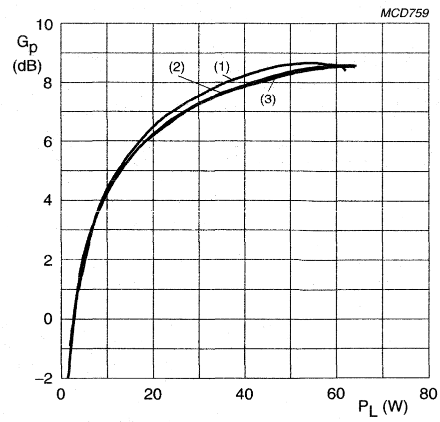
RF performance at $T_h = 25\ °C$ in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
Class-C; $t_p = 100\ \mu s$; $\delta = 10\%$	3.1 to 3.5	40	≥50 typ. 55	≥7 typ. 8	≥35 typ. 40



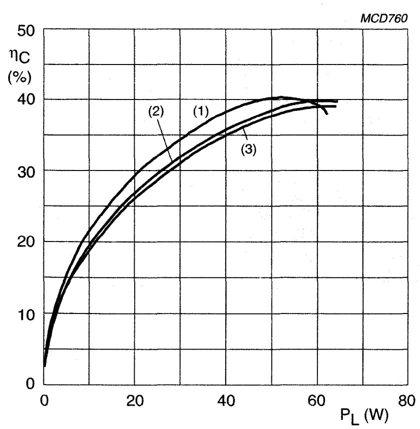
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.5 GHz.
(2) f = 3.3 GHz.
(3) f = 3.1 GHz.

Fig.2 Load power as a function of drive power; typical values.



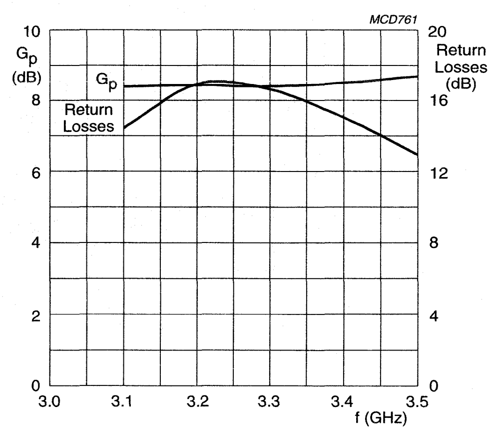
V_{CB} = 40 V; class-C; P_L = 50 W; t_p = 100 μs; δ = 10%.
(1) f = 3.5 GHz.
(2) f = 3.3 GHz.
(3) f = 3.1 GHz.

Fig.3 Power gain as a function of load power; typical values.



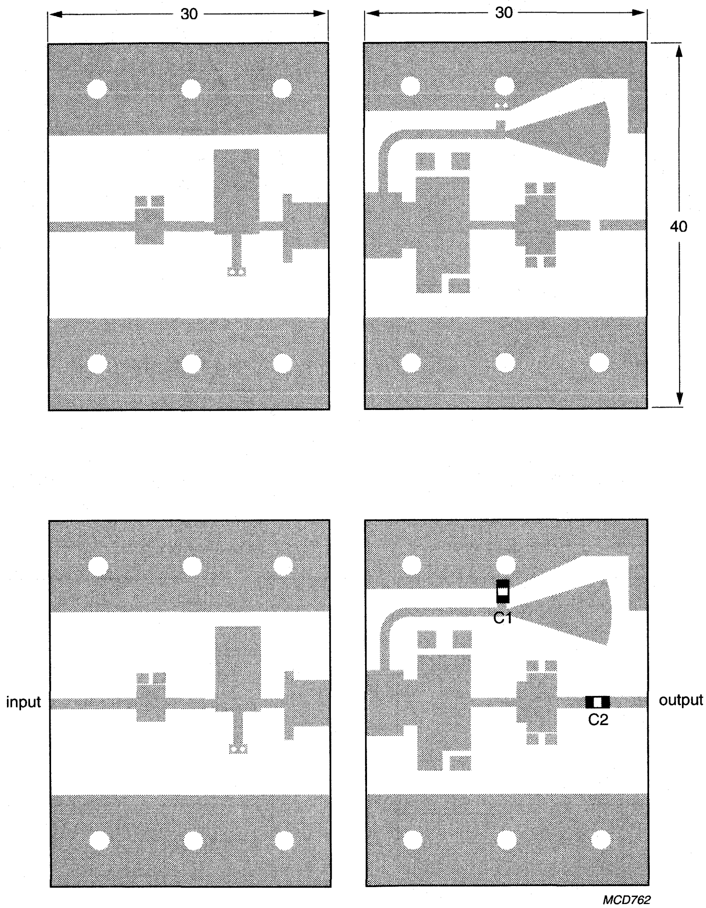
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.5 GHz.
(2) f = 3.3 GHz.
(3) f = 3.1 GHz.

Fig.4 Collector efficiency as a function of load power; typical values.



V_{CB} = 40 V; class-C; P_L = 50 W; t_p = 100 μs; δ = 10%.

Fig.5 Power gain and input return losses as functions of frequency; typical values.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Duroid dielectric (ε_r = 2.2), thickness 0.38 mm. The other side is unetched and serves as a ground plane.

C1 = C2 = ATC 100A 5.1 pF

Fig.6 Component layout for 3.1 to 3.5 GHz class-C test circuit.

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

- Common base class-C pulsed power amplifiers for radar applications in the 3.1 to 3.5 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT422A) with the common base connected to the flange.

PINNING - SOT422A

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange

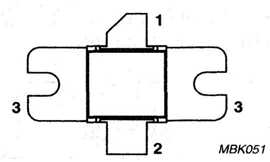


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_C (%)
Pulsed, class-C	3.1 to 3.5	40	65	≥7	≥35

WARNING
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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100\ \mu s$; $\delta \leq 10\%$	–	8	A
P_{tot}	total power dissipation	$t_p = 100\ \mu s$; $\delta = 10\%$; $T_{mb} = 25\ °C$	–	200	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10$ s	–	235	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 100\ \mu s$; $\delta = 10\%$; note 1	0.57	K/W
		$t_p = 300\ \mu s$; $\delta = 10\%$; note 1	0.74	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

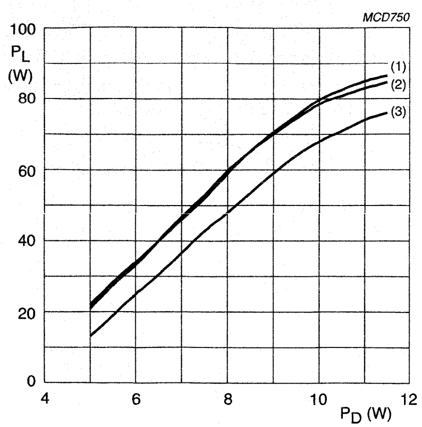
$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 20$ mA; open emitter	75	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 20$ mA; $V_{BE} = 0$	75	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40$ V; $I_E = 0$	–	2	mA
I_{CES}	collector leakage current	$V_{CE} = 40$ V; $V_{BE} = 0$	–	4	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5$ V; $I_C = 0$	–	0.4	mA
h_{FE}	DC current gain	$V_{CB} = 5$ V; $I_C = 2$ A	40	–	

APPLICATION INFORMATION

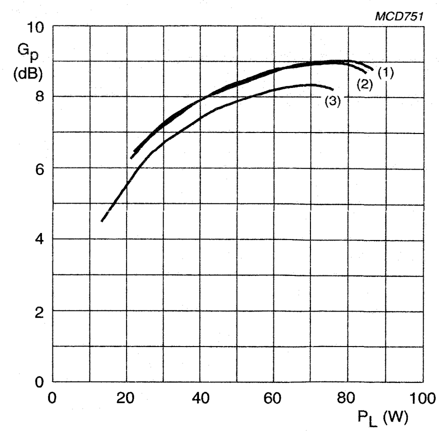
RF performance at $T_h = 25\ °C$ in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
Class-C; $t_p = 100\ \mu s$; $\delta = 10\%$	3.1 to 3.5	40	≥65	≥7	≥35



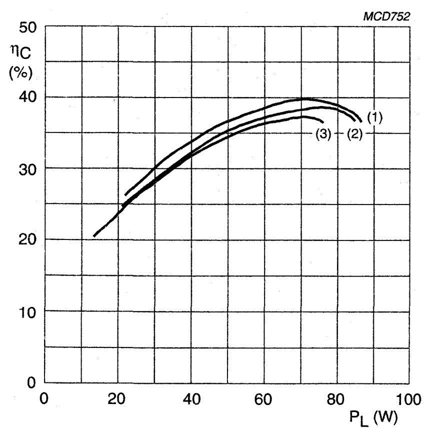
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.2 Load power as a function of the drive power; typical values.



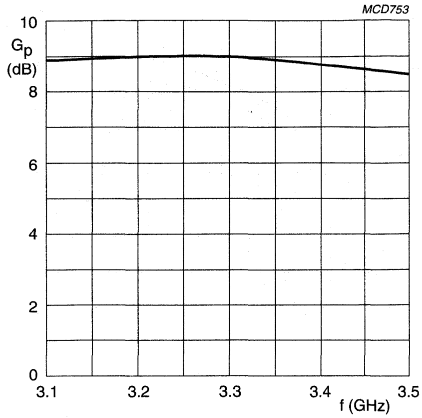
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.3 Power gain as a function of load power; typical values.



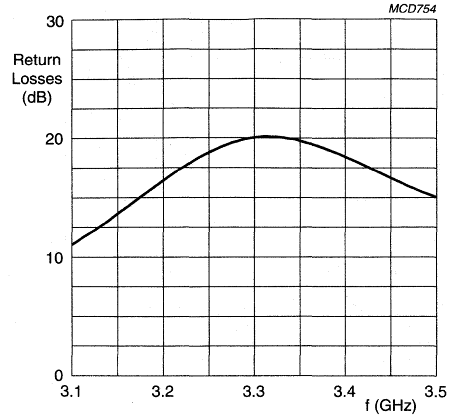
V_{CB} = 40 V; class-C; t_p = 100 μs; δ = 10%.
(1) f = 3.1 GHz.
(2) f = 3.3 GHz.
(3) f = 3.5 GHz.

Fig.4 Collector efficiency as a function of load power; typical values.



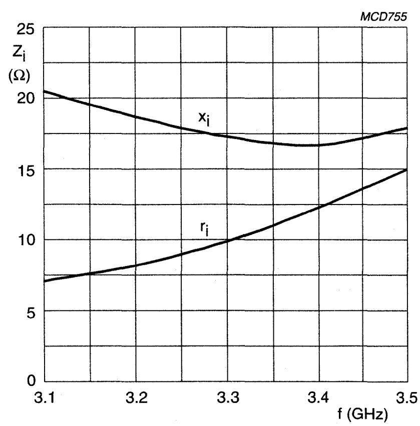
V_{CB} = 40 V; class-C; t_p = 100 µs; δ = 10%.

Fig.5 Power gain as a function of frequency; typical values.



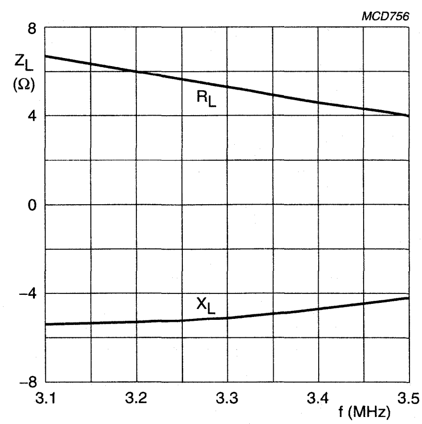
V_{CB} = 40 V; class-C; t_p = 100 µs; δ = 10%.

Fig.6 Return losses input as a function of frequency; typical values.



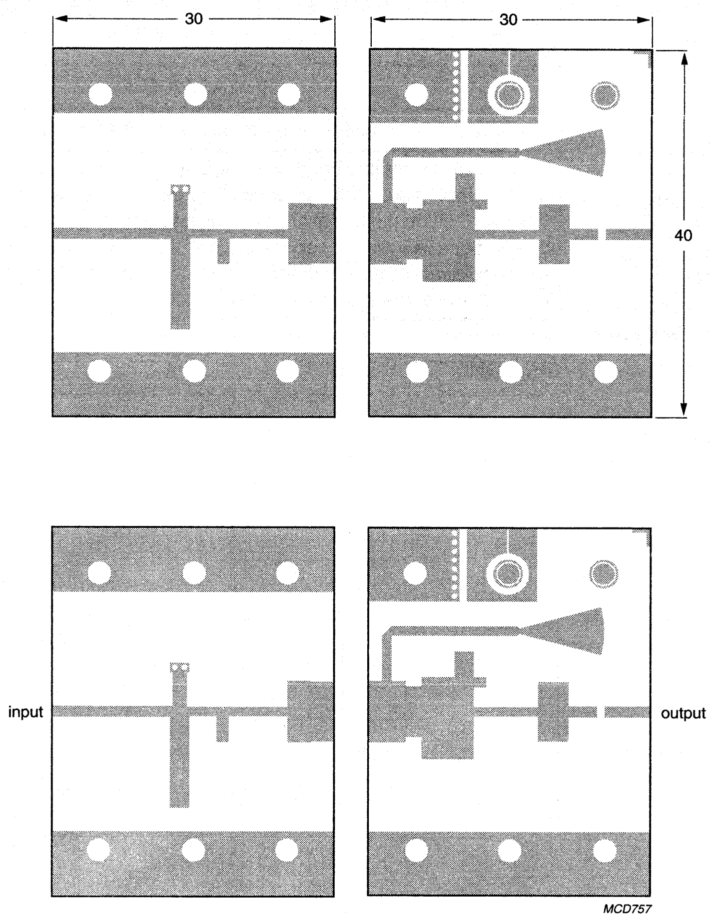
V_{CB} = 40 V; class-C; P_L = 65 W.

Fig.7 Input impedance as a function of frequency (series components); typical values.



V_{CB} = 40 V; class-C; P_L = 65 W.

Fig.8 Load impedance as a function of frequency (series components); typical values.



Dimensions in mm.

The components are located on one side of the copper-clad printed circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

The striplines are on double-clad printed-circuit board with Duroid dielectric (ε_r = 2.2); thickness = 0.38 mm.

Fig.9 Component layout for 3.1 to 3.5 GHz class-C test circuit.

UHF power transistor BLT53

FEATURES

- Emitter-ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability
- Withstands full load mismatch.

DESCRIPTION

NPN silicon planar epitaxial transistor encapsulated in a 4-lead SOT122D studless envelope with a ceramic cap. It is designed for common emitter, class-B operation in portable radio transmitters in the 470 MHz communications band. All leads are isolated from the mounting flange.

PINNING - SOT122D

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_c (%)
c.w. class-B	470	7.5	8	> 6	> 60

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

PIN CONFIGURATION

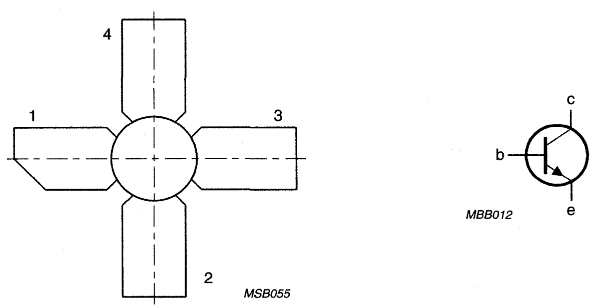


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	10	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C, $I_{C(AV)}$	collector current	DC or average value	–	2.5	A
I_{CM}	collector current	peak value f > 1 MHz	–	7.5	A
P_{tot}	total power dissipation	RF operation; T_{mb} = 25 °C	–	35.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction operating temperature		–	200	°C

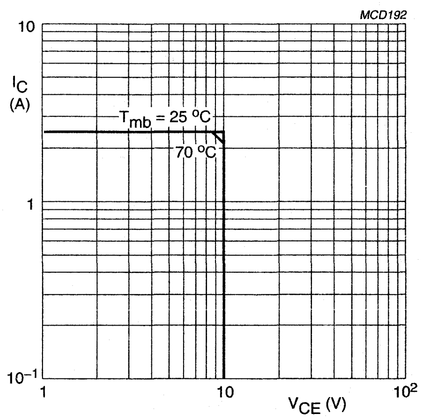
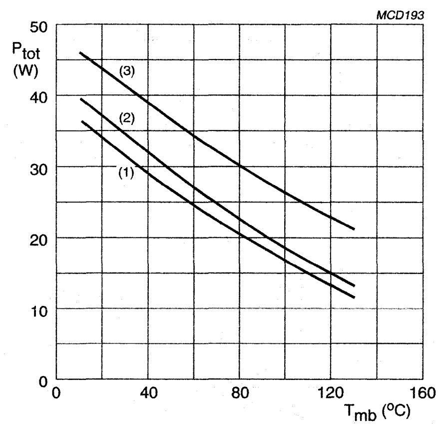


Fig.2 DC SOAR.



(1) Continuous DC operation.
(2) Continuous RF operation (f > 1 MHz).
(3) Short time operation during mismatch (f > 1 MHz).

Fig.3 Power derating curve.

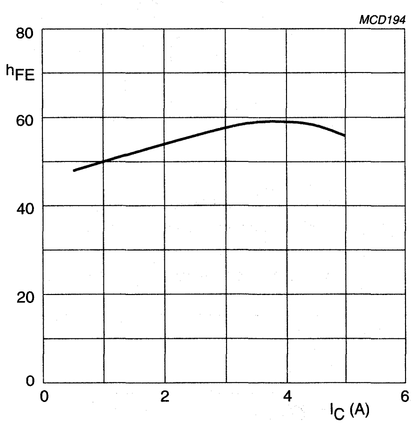
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb(RF)}$	from junction to mounting base	P_{tot} = 35.5 W; T_{mb} = 25 °C	4.9	K/W

CHARACTERISTICS

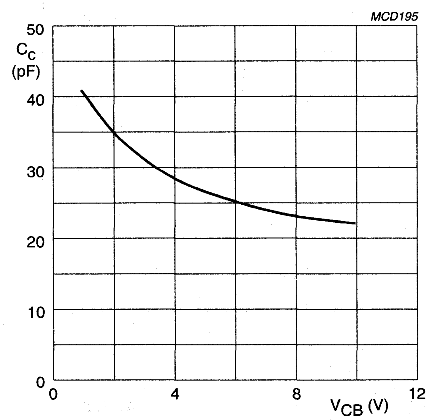
$T_j = 25\ °C$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; $I_C = 20$ mA	20	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; $I_C = 40$ mA	10	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 4$ mA	3	–	–	V
I_{CES}	collector-emitter leakage current	$V_{BE} = 0$; $V_{CE} = 10$ V	–	–	1	mA
h_{FE}	DC current gain	$V_{CE} = 5$ V; $I_C = 1.2$ A	25	–	–	
f_T	transition frequency	$V_{CE} = 7.5$ V; $I_E = 1.6$ A	–	3.9	–	GHz
C_c	collector capacitance	$V_{CB} = 7.5$ V; $I_E = I_e = 0$; f = 1 MHz	–	24	–	pF
C_{re}	feedback capacitance	$V_{CE} = 7.5$ V; $I_C = 0$; f = 1 MHz	–	17	–	pF
$C_{c\text{-}mb}$	collector-mounting base capacitance	f = 1 MHz	–	1.2	–	pF



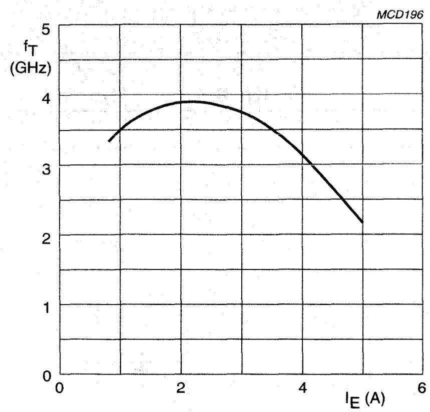
$V_{CE} = 5$ V.

Fig.4 DC current gain as a function of collector current, typical values.



$I_E = i_e = 0$; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage, typical values.



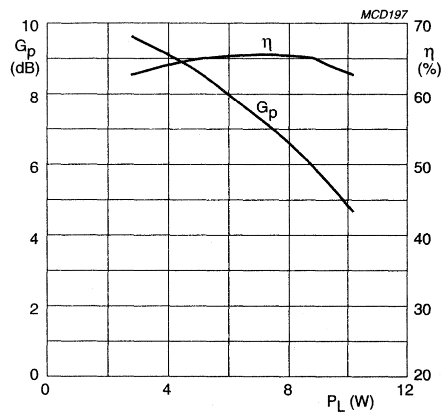
V_{CB} = 7.5 V.

Fig.6 Transition frequency as a function of emitter current, typical values.

APPLICATION INFORMATION

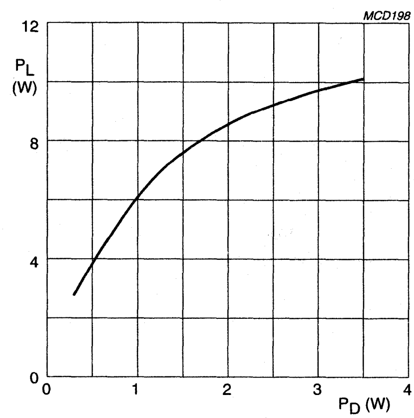
RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_c (%)
c.w. class-B	470	7.5	8	> 6 typ. 6.8	> 60 typ. 65



Class-B operation; V_{CE} = 7.5 V; f = 470 MHz.

Fig.7 Gain and efficiency as functions of load power, typical values.



Class-B operation; V_{CE} = 7.5 V; f = 470 MHz.

Fig.8 Load power as a function of drive power, typical values.

Ruggedness in class-B operation

The BLT53 is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases at rated output power, up to a supply voltage of 9 V, and f = 470 MHz.

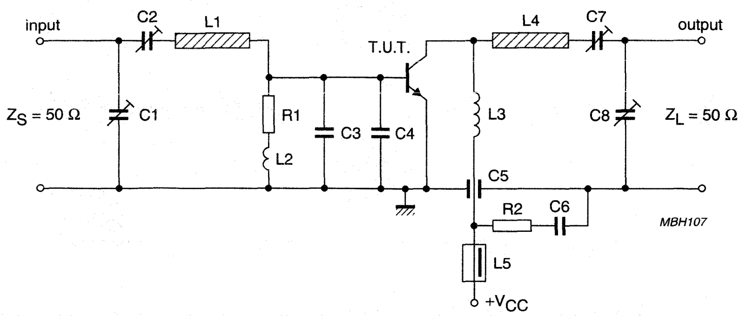


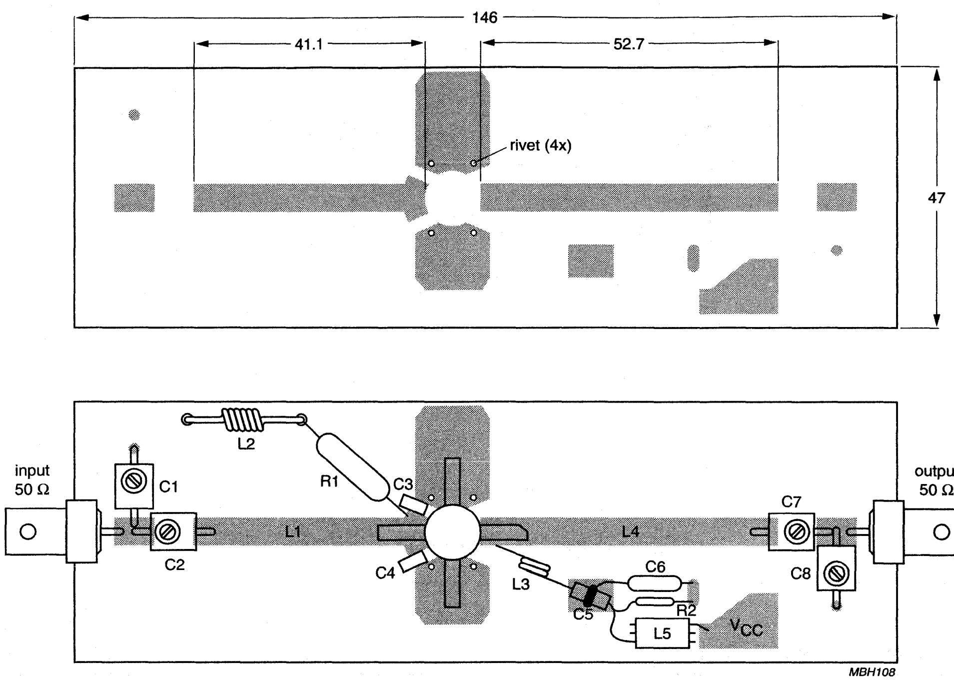
Fig.9 Class-B test circuit at f = 470 MHz.

List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7, C8	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3, C4	multilayer ceramic chip capacitor	15 pF		
C5	feed-through capacitor	100 pF		
C6	polyester capacitor	33 nF		
L1	stripline (note 1)	44 Ω	41.1 mm × 5 mm	
L2	13 turns closely wound enamelled 0.5 mm copper wire	320 nH	int. dia. 4 mm	
L3	2 turns enamelled 1 mm copper wire		int. dia. 4 mm; pitch 1.5 mm; leads 2 × 5 mm	
L4	stripline (note 1)	44 Ω	52.7 mm × 5 mm	
L5	grade 3B1 Ferroxcube wideband HF choke			4312 020 36640
R1	0.25 W carbon resistor	1 Ω, 5%		
R2	0.25 W carbon resistor	10 Ω, 5%		

Note

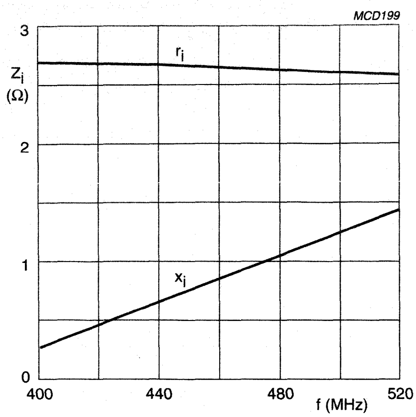
1. The striplines are mounted on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.74$); thickness $^1\!/_{16}$ inch.



The circuit and components are situated on one side of a copper-clad PTFE fibre-glass board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by means of hollow rivets.

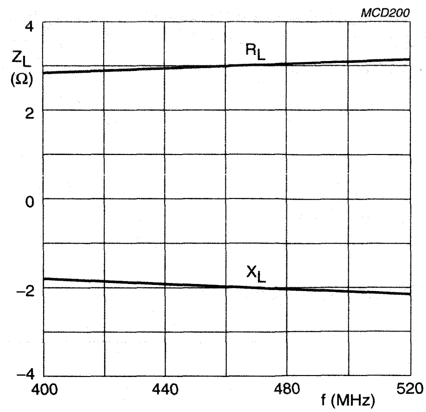
Dimensions in mm.

Fig.10 Component layout for 470 MHz class-B test circuit.



Class-B operation; V_{CE} = 7.5 V; P_L = 8 W.

Fig.11 Input impedance (series components) as a function of frequency, typical values.



Class-B operation; V_{CE} = 7.5 V; P_L = 8 W.

Fig.12 Load impedance (series components) as a function of frequency, typical values.

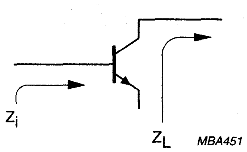
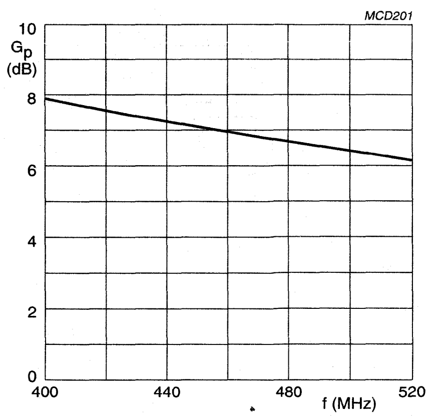


Fig.13 Definition of transistor impedance.



Class-B operation; V_{CE} = 7.5 V; P_L = 8 W.

Fig.14 Power gain as a function of frequency, typical values.

UHF power transistor | BLU30/12

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the 470 MHz communications band.

FEATURES:

- multi-base structure and emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability
- internal matching to achieve an optimum wideband capability and high power gain

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-119). All leads are isolated from the flange.

QUICK REFERENCE DATA

Envelope	SOT-119			
Mode of operation	class-B; c.w.			
Collector-emitter voltage (d.c.)	V_{CE}		12,5	V
Frequency	f		470	MHz
Load power	P_L		30	W
Power gain	G_P	>	6,0	dB
Collector efficiency	η_C	>	55	%
Heatsink temperature	T_h		25	°C

PIN CONFIGURATION

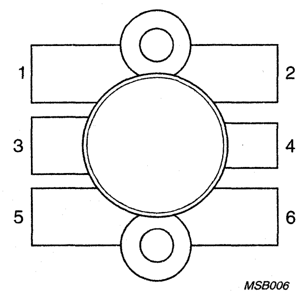


Fig.1 Simplified outline, SOT119A.

PINNING

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)				
peak value	V_{CBOM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	16,5	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current				
d.c. or average	I_C	max.	6	A
(peak value); f > 1 MHz	I_{CM}	max.	18	A
Total power dissipation				
f > 1 MHz; T_{mb} = 25 °C	P_{tot} (r.f.)	max.	65	W
Storage temperature	T_{stg}	–65 to + 150		°C
Operating junction temperature	T_j	max.	200	°C

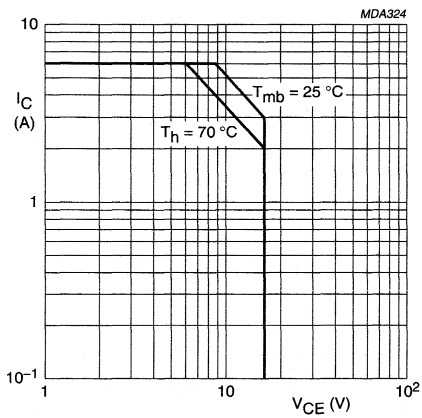
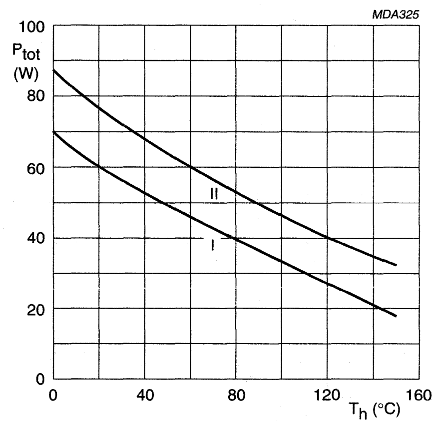


Fig.2 D.C. SOAR. $R_{th\ mb\text{-}h}$ = 0,2 K/W



I Continuous operation (f > 1 MHz)
II Short-time operation during mismatch; (f > 1 MHz.

Fig.3 Power/temperature derating curves

THERMAL RESISTANCE

(dissipation = 45 W; T_{mb} = 25 °C)

From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(r.f.)}$	max.	2,45	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max.	0,2	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage				
I_C = 50 mA; open emitter	$V_{(BR)CBO}$	>	36	V
Collector-emitter breakdown voltage				
I_C = 100 mA; open base	$V_{(BR)CEO}$	>	16,5	V
Emitter-base breakdown voltage				
I_E = 10 mA; open collector	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	22	mA
Second breakdown energy				
L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	>	8	mJ
D.C. current gain				
I_C = 4 A; V_{CE} = 10 V	h_{FE}	>	15	
		typ.	60	
Collector capacitance at f = 1 MHz(1)				
$I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	85	pF
Feed-back capacitance at f = 1 MHz(1)				
I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	52	pF
Collector-flange capacitance	C_{cf}	typ.	3	pF

Note

1. Device mounted in SOT-119 envelope without inputmatching.

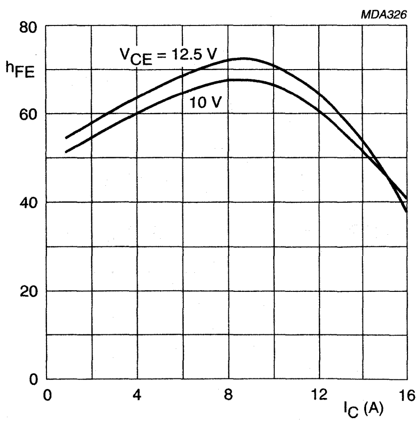


Fig.4 T_j = 25 °C; typ. values.

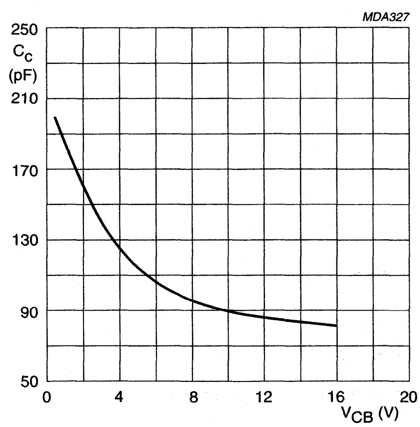


Fig.5 $I_E = i_e$ = 0; f = 1 MHz; typ. values.

APPLICATION INFORMATION

Mode of operation	In narrow-band test circuit; class-B; c.w.			
Collector-emitter voltage (d.c.)	V_{CE}		12,5	V
Frequency	f		470	MHz
Load power	P_L		30	W
Power gain	G_p	>	6,0	dB
		typ.	7,4	dB
Collector efficiency	η_C	>	55	%
		typ.	66	%
Heatsink temperature	T_h		25	°C

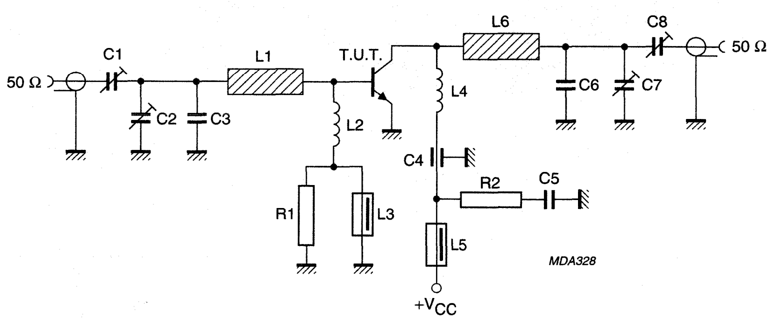


Fig.6 Class-B test circuit at f = 470 MHz.

List of components:

C1 = C2 = C7 = C8 = 2 to 9 pF film dielectric trimmer (cat. no. 2222 809 09002)
C3 = C6 = 3,9 pF ceramic capacitor (500 V)
C4 = 100 pF feed-through capacitor
C5 = 100 nF polyester film capacitor
L1 = stripline (24,0 mm × 6,7 mm)
L2 = 10 turns closely wound enamelled Cu-wire (0,4 mm); int. diam. 4 mm
L3 = 2 turns enamelled Cu-wire (0,6 mm); Ferroxcube tube core, grade 3B5 (cat. no. 4313 020 15170)
L4 = 12,6 nH; 2,5 turns enamelled Cu-wire (0,7 mm); int. diam. 4 mm; length 3 mm; leads 2 × 5 mm
L5 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)
L6 = stripline (28,4 mm × 6,7 mm)
R1 = R2 = 10 Ω carbon resistor

L1 and L6 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ε_r = 2,74); thickness 1/16 inch.

Component lay-out and printed-circuit board for 470 MHz test circuit are shown in Figs 7 and 8.

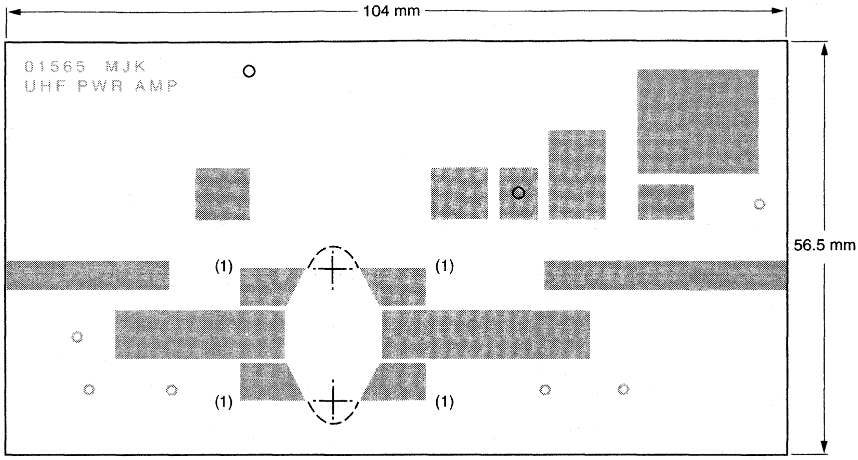
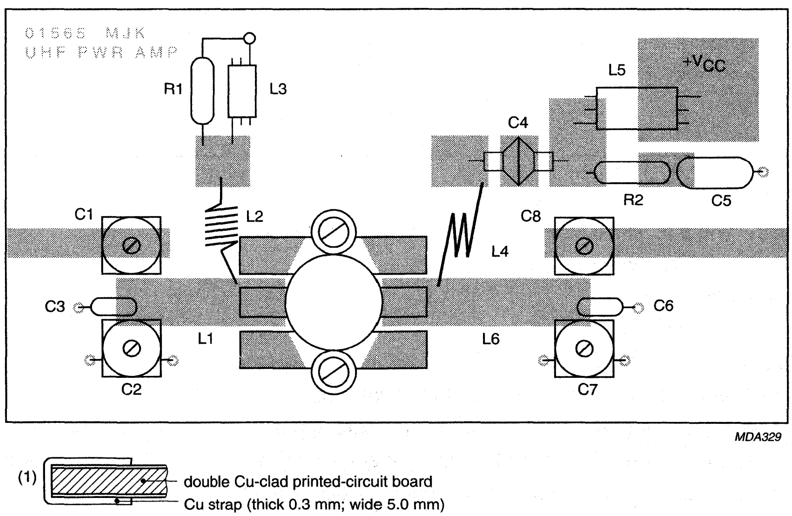
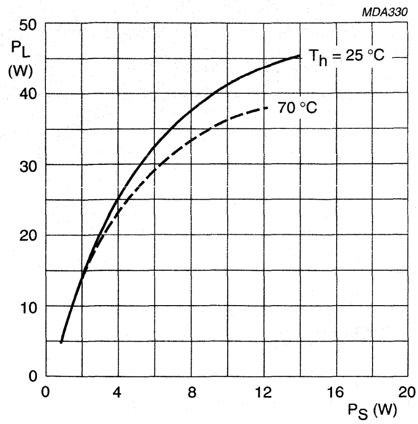


Fig.7 P.c. board for 470 MHz, class-B test circuit.



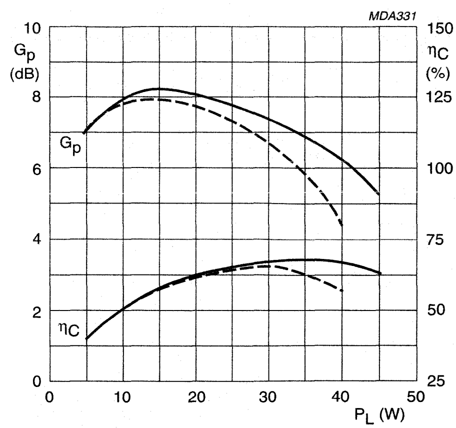
The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side fully metallized serving as groundplane. Earth connections are made by hollow rivets and also by copper straps under the emitter to provide a direct contact between the copper on the component side and the ground plane.

Fig.8 Component lay-out of 470 MHz, class-B test circuit.



V_{CE} = 12,5 V; f = 470 MHz; class-B operation;
T_h = 25 °C and 70 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W; typical values.

Fig.9 Load power vs. source power.

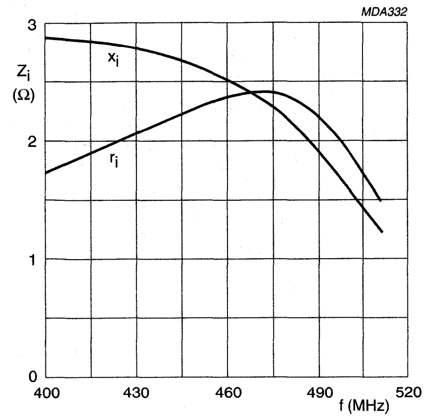


—— T_h = 25 °C;
- - - T_h = 70 °C.
V_{CE} = 12,5 V; f = 470 MHz; class-B operation;
T_h = 25 °C and 70 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W; typical values.

Fig.10 Power and gain and efficiency vs. load power.

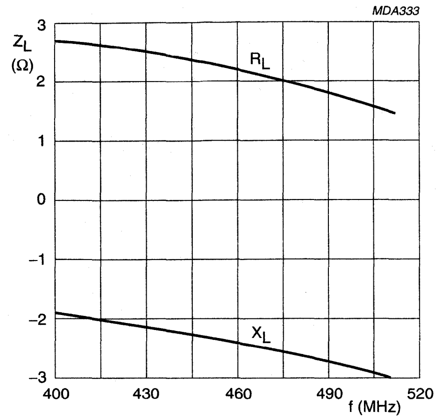
RUGGEDNESS

The device is capable of withstanding a full load mismatch (VSWR = 50; all phases) up to 38 W under the following conditions:
V_{CE} = 15,5 V; f = 470 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W.



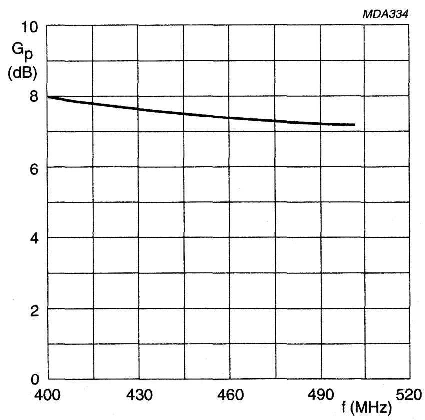
V_{CE} = 12,5 V; P_L = 30 W; f = 400–512 MHz; T_h = 25 °C; class-B operation; $R_{th\ mb\text{-}h}$ = 0,2 K/W; typical values.

Fig.11 Input impedance (series components).



V_{CE} = 12,5 V; P_L = 30 W; f = 400–512 MHz; T_h = 25 °C; class-B operation; $R_{th\ mb\text{-}h}$ = 0,2 K/W; typical values.

Fig.12 Load impedance (series components).



V_{CE} = 12,5 V; P_L = 30 W; f = 400–512 MHz; T_h = 25 °C; class-B operation; $R_{th\ mb\text{-}h}$ = 0,2 K/W; typical values.

Fig.13 Power gain versus frequency.

UHF power transistor

BLU99
BLU99/SL

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the u.h.f. band. The transistor is also very suitable for application in the 900 MHz mobile radio band.

FEATURES

- multi-base structure and diffused emitter-ballasting resistors for an optimum temperature profile;
- gold metallization ensures excellent reliability.

The BLU99 has a 4-lead stud envelope with a ceramic cap (SOT122A). All leads are isolated from the stud. The BLU99/SL is a studless version (SOT122D).

QUICK REFERENCE DATA

R.F. performance at T_h = 25 °C in a common-emitter class-B circuit.

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η_C %
narrow band; c.w.	12,5	470	5	> 10,5	> 60
	12,5	900	4	typ. 7,0	typ. 60

PIN CONFIGURATION

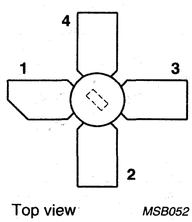


Fig.1 Simplified outline. SOT122A (BLU99).

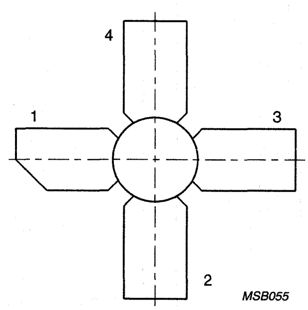


Fig.2 Simplified outline. SOT122D (BLU99/SL).

PINNING - SOT122A; SOT122D

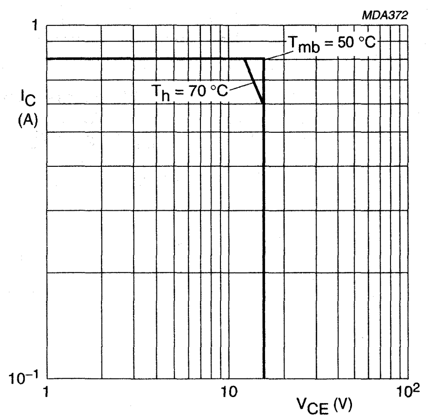
PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

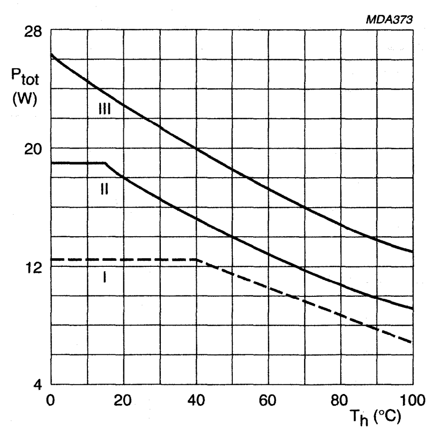
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3 V
Collector current			
d.c. or average	$I_C;I_{C(AV)}$	max.	0,8 A
peak value; f > 1 MHz	I_{CM}	max.	2,5 A
D.C. power dissipation up to T_{mb} = 50 °C	$P_{tot\ (d.c.)}$	max.	12,5 W
R.F. power dissipation			
f > 1 MHz; T_{mb} = 25 °C	$P_{tot\ (r.f.)}$	max.	19 W
Storage temperature	T_{stg}	−65 to + 150	°C
Operating junction temperature	T_j	max.	200 °C



$R_{th\ mb-h}$ = 0,6 K/W.

Fig.3 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation (f > 1 MHz).
III Short-time r.f. operation during mismatch (f > 1 MHz).

Fig.4 Power/temperature derating curves.

THERMAL RESISTANCE

(dissipation = 9 W; T_{mb} = 25 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j-mb(dc)}$	=	10 K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j-mb(rf)}$	=	7,5 K/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0,6 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage				
open emitter; I_C = 10 mA	$V_{(BR)CBO}$	>	36	V
Collector-emitter breakdown voltage				
open base; I_C = 20 mA	$V_{(BR)CEO}$	>	16	V
Emitter-base breakdown voltage				
open collector; I_E = 1 mA	$V_{(BR)EBO}$	>	3	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	5	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
R_{BE} = 10 Ω	E_{SBR}	>	1	mJ
D.C. current gain(2)				
I_C = 0,6 A; V_{CE} = 10 V	h_{FE}	>	25	
		typ.	100	
Transition frequency at f = 500 MHz(1)				
I_C = 0,6 A; V_{CE} = 12,5 V	f_T	typ.	4,0	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	7,5	pF
Feedback capacitance at f = 1 MHz				
I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	5	pF
Collector-stud capacitance	C_{cs}	typ.	1,2	pF

Notes

1. Measured under pulse conditions: t_p = 50 µs; $\delta < 0{,}01$.
2. Measured under pulse conditions: t_p = 300 µs; $\delta < 0{,}01$.

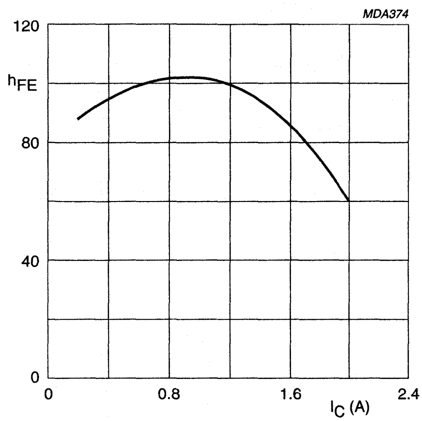


Fig.5 V_{CE} = 10 V; T_j = 25 °C; typ. values.

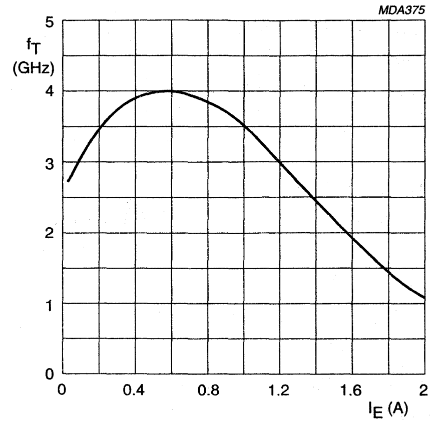


Fig.6 V_{CB} = 12,5 V; f = 500 MHz; T_j = 25 °C; typ. values.

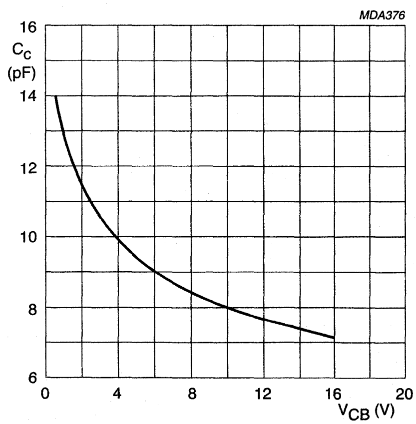


Fig.7 $I_E = i_e = 0$; f = 1 MHz; typ. values.

APPLICATION INFORMATION (PART I)

R.F. performance in c.w. operation (common-emitter class-B circuit) at f = 470 MHz; T_h = 25 °C.

MODE OF OPERATION	V_{CE} V	P_L W	P_S W	G_p dB	I_C A	η_C %
narrow band; c.w.	12,5	5	< 0,45 typ. 0,32	> 10,5 typ. 12	< 0,665 typ. 0,60	> 60 typ. 66

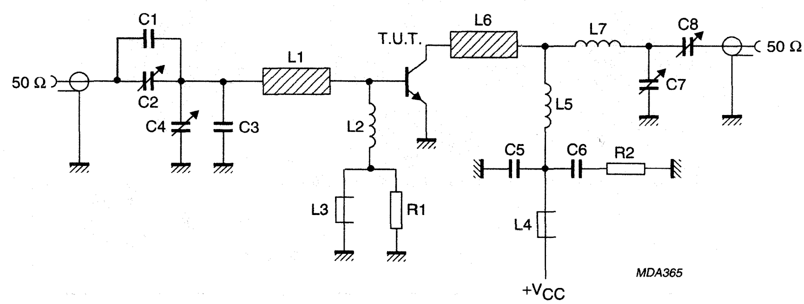


Fig.8 Class-B test circuit at f = 470 MHz.

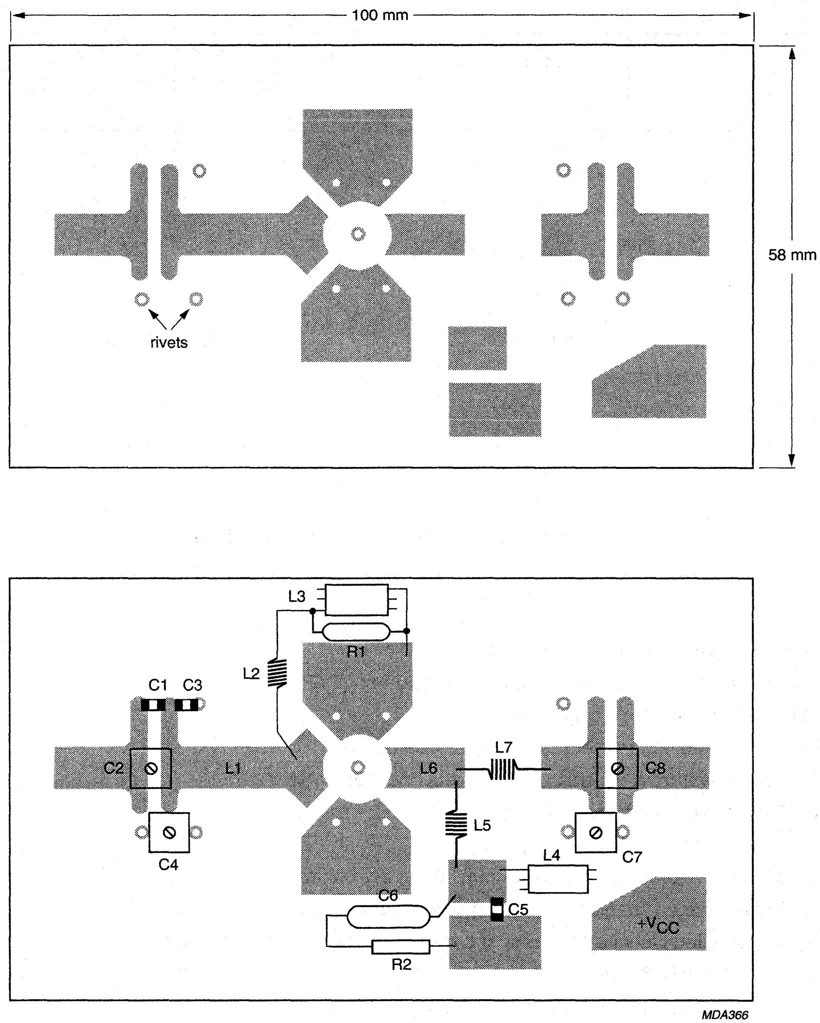
List of components:

C1 = 2,7 pF multilayer ceramic chip capacitor[1]
C2 = C7 = C8 = 1,4-5,5 pF film dielectric trimmer (cat.no. 2222 809 09001)
C3 = 7,5 pF multilayer ceramic chip capacitor[1]
C4 = 2-9 pF film dielectric trimmer (cat.no. 2222 809 09002)
C5 = 100 pF multilayer ceramic chip capacitor (cat. no. 2222 852 13101)
C6 = 100 nF metallized film capacitor (cat. no. 2222 352 45104)
L1 = stripline, 22,5 mm × 6,0 mm
L2 = 1 turn Cu-wire (1,0 mm), int. dia. 5,5 mm, leads 2 × 5 mm
L3 = L4 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)
L5 = 4 turns enamelled Cu-wire (1,0 mm), int. dia. 6 mm, length 7,5 mm, leads 2 × 5 mm
L6 = stripline, 10,0 mm × 6,0 mm
L7 = 1 turn Cu-wire (1,0 mm), int. dia. 5 mm, leads 2 × 5 mm
R1 = R2 = 10 Ω metal film resistor, 0,25 W

L1 and L6 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ε_r = 2,74) and a thickness of $^1\!/_{16}$ inch.

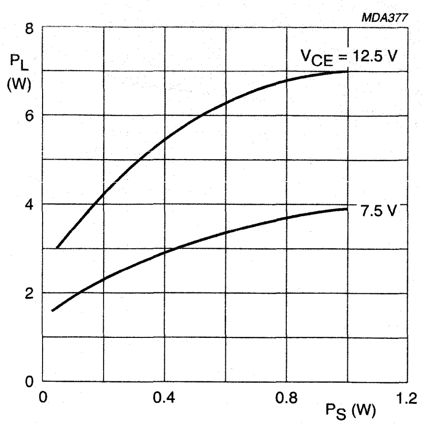
Note

1. American Technical Ceramics capacitor type 100 A or capacitor of same quality.



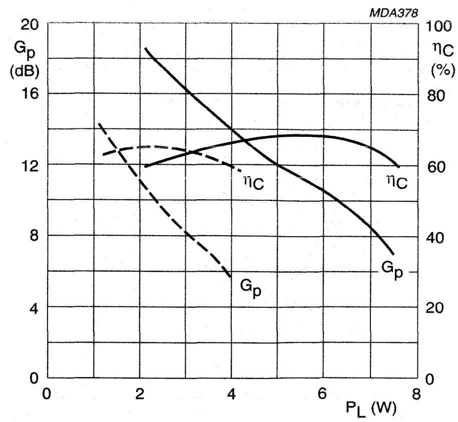
The circuits and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper to serve as ground plane. Earth connections are made by hollow rivets.

Fig.9 Printed circuit board and component layout for 470 MHz.



f = 470 MHz; class-B operation; T_h = 25 °C; typ. values.

Fig.10 Output power.

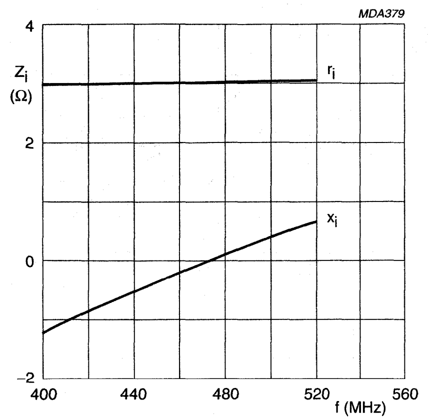


f = 470 MHz; class-B operation; T_h = 25 °C; typ. values.
——— : V_{CE} = 12,5 V;
- - - - : V_{CE} = 7,5 V.

Fig.11 Power gain and efficiency;

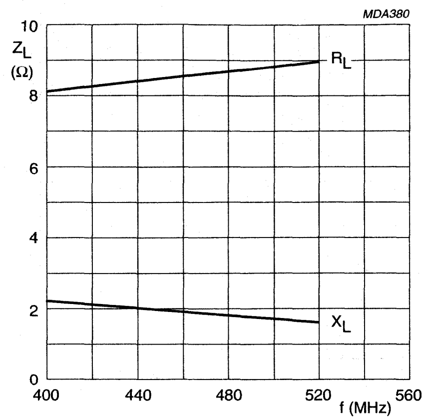
RUGGEDNESS:

The device is capable of withstanding a load mismatch with VSWR = 50 (all phases) up to a supply voltage of 15,5 V at rated load power.



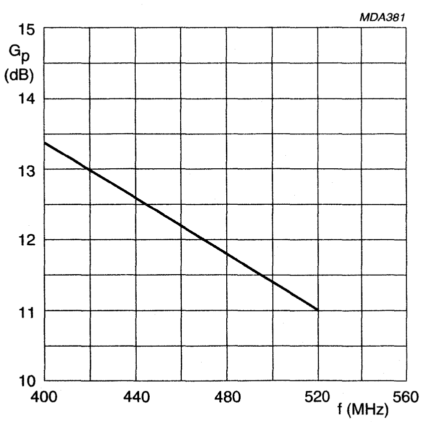
V_{CE} = 12,5 V; P_L = 5 W; T_h = 25 °C;
f = 400-520 MHz; typical values.

Fig.12 Input impedance (series components).



V_{CE} = 12,5 V; P_L = 5 W; T_h = 25 °C;
f = 400-520 MHz; typical values.

Fig.13 Load impedance (series components).



V_{CE} = 12,5 V; P_L = 5 W; T_h = 25 °C;
f = 400-520 MHz; typical values.

Fig.14 Power gain.

APPLICATION INFORMATION (PART II)

R.F. performance in c.w. operation (common-emitter class-B circuit) at f = 900 MHz; T_h = 25 °C

MODE OF OPERATION	V_{CE} V	P_L W	P_S W	G_P dB	I_C A	η_C %
narrow band; c.w.	12,5	4	typ. 0,8	typ. 7,0	typ. 0,54	typ. 60

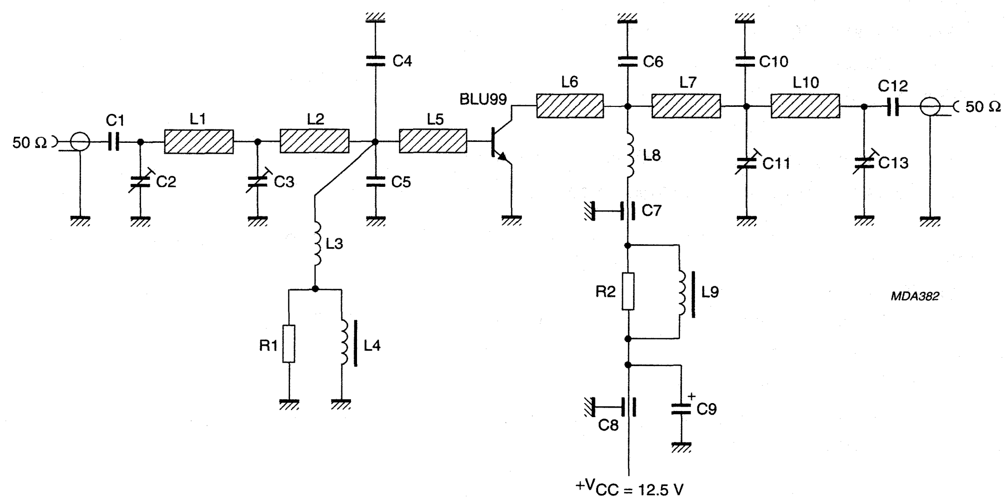


Fig.15 Class-B test circuit at f = 900 MHz.

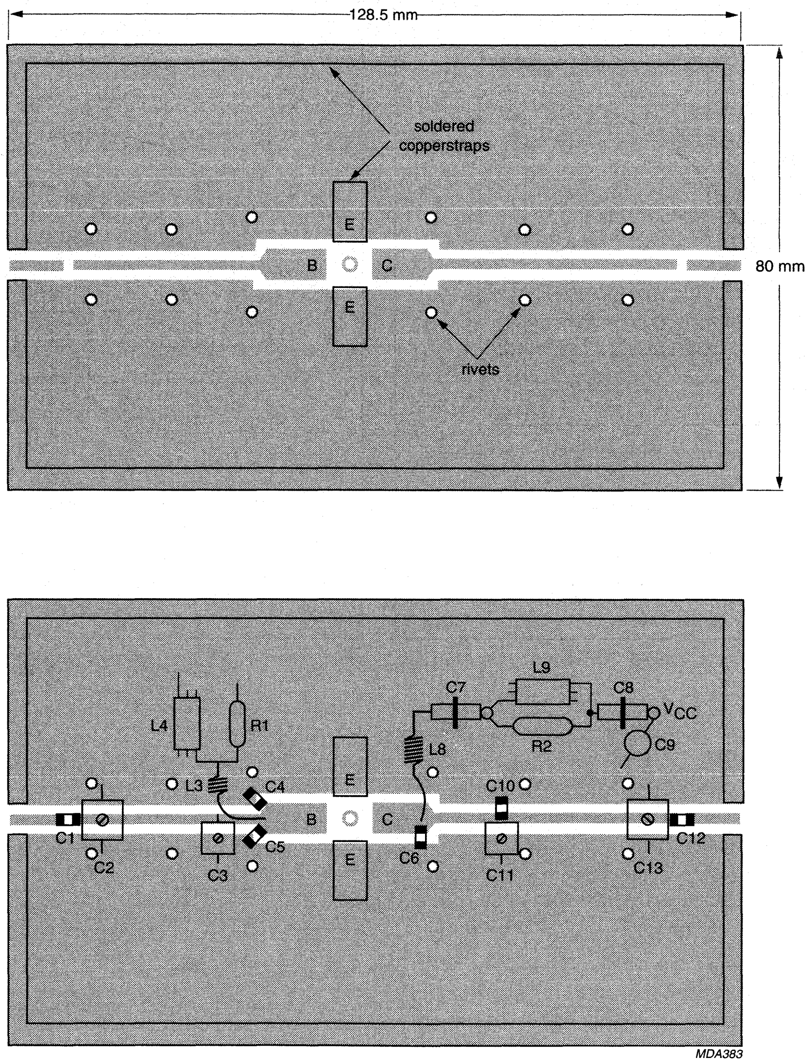
List of components:

C1	=	C12 = 33 pF multilayer ceramic chip capacitor(1)
C2	=	C13 = 1,4-5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C3	=	C11 = 1,2-3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)
C4	=	C5 = C10 = 6,2 pF multilayer ceramic chip capacitor(1)
C6	=	1 pF multilayer ceramic chip capacitor(1)
C7	=	10 pF ceramic feed-through capacitor
C8	=	330 pF ceramic feed-through capacitor
C9	=	2,2 μF tantalum electrolytic capacitor
L1	=	stripline, 21,0 mm × 1,85 mm
L2	=	stripline, 5,0 mm × 1,85 mm
L3	=	60 nH, 4 turns enamelled Cu-wire (0,4 mm), close wound, int. dia. 3 mm
L4	=	L9 = Ferroxcube wideband h.f. choke, grade 3B (cat. no 4312 020 36642)
L5	=	stripline, 11,3 mm × 6,0 mm
L6	=	stripline, 10,0 mm × 6,0 mm
L7	=	stripline, 15,9 mm × 1,85 mm
L8	=	280 nH, 15 turns enamelled Cu-wire (0,4 mm), close wound, int. dia. 3 mm
L10	=	stripline, 28,0 mm × 1,85 mm
R1	=	R2 = 10 Ω metal film resistor, 0,25 W

L1, L2, L5, L6, L7 and L10 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ε_r = 2,74) and thickness of $^1/_{32}$ inch.

Note

1. American Technical Ceramics capacitor type 100 A or capacitor of same quality.



The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper to serve as a ground plane. Earth connections are made by hollow rivets and also by fixing screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

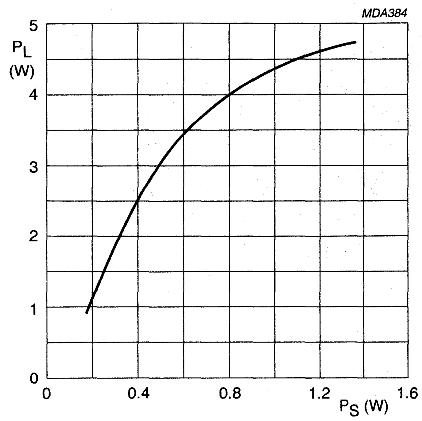
Fig.16 Printed circuit board and component layout for a 900 MHz test circuit.

RUGGEDNESS

The device is capable of withstanding a load mismatch with VSWR = 50 (all phases) up to a supply voltage of 15,5 V at rated load power.

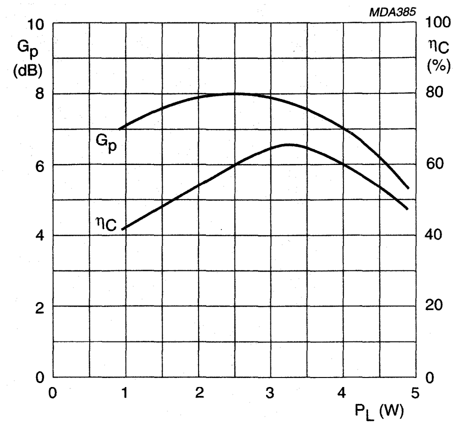
UHF power transistor

BLU99
BLU99/SL



f = 900 MHz; V_{CE} = 12,5 V; class-B operation;
T_h = 25 °C; typ. values.

Fig.17 Output power.

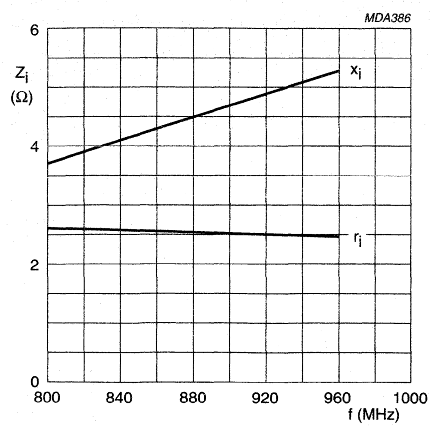


f = 900 MHz; V_{CE} = 12,5 V; class-B operation;
T_h = 25 °C; typ. values.

Fig.18 Power gain and efficiency.

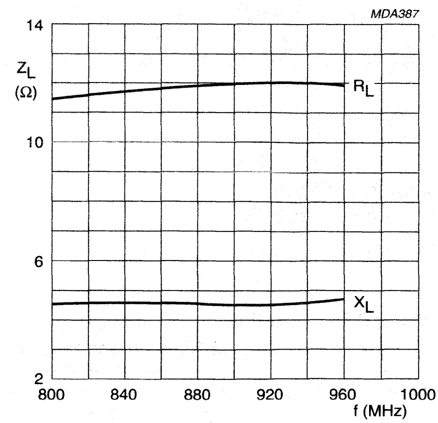
UHF power transistor

BLU99
BLU99/SL



f = 800-960 MHz; V_{CE} = 12,5 V; P_L = 4 W;
T_h = 25 °C; typ. values.

Fig.19 Input impedance (series components).



f = 800-960 MHz; V_{CE} = 12,5 V; P_L = 4 W;
T_h = 25 °C; typ. values.

Fig.20 Load impedance (series components).

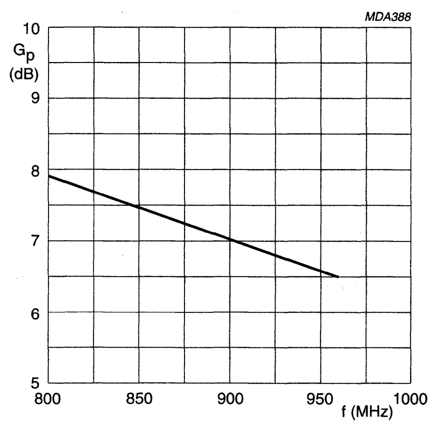


Fig.21 Power gain.

VHF power transistor

BLV10

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, B and C operated mobile, h.f. and v.h.f. transmitters with a nominal supply voltage of 13,5 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions with a supply over-voltage to 16,5 V.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in an unneautralized common-emitter class-B circuit

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_P dB	η %	$\bar{z}_i$ Ω	$\bar{Y}_L$ mS
c.w.	**13,5**	**175**	**8**	**> 9,0**	**> 70**	**2,8 + j1,2**	**76 − j16**
c.w.	12,5	175	8	typ. 10,5	typ. 75	–	–

PIN CONFIGURATION

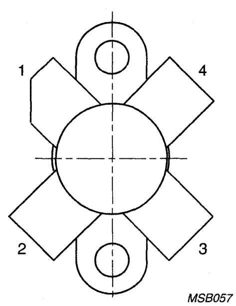


Fig.1 Simplified outline, SOT123.

PINNING

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	18	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	1,5	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	4,0	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	20	W
Storage temperature	T_{stg}	−65 to + 150		°C
Operating junction temperature	T_j	max.	200	°C

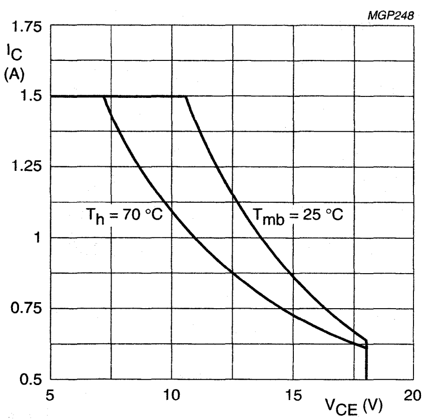
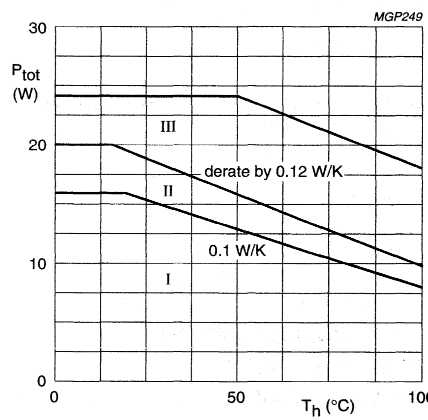


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \leq$ 16,5 V; f > 1 MHz.

THERMAL RESISTANCE

(dissipation = 8 W; T_{mb} = 72,4 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	10,7 K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	8,6 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3 K/W

CHARACTERISTICS

T_j = 25 °C

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 5 mA	$V_{(BR)\ CES}$	>	36	V
Collector-emitter breakdown voltage				
open base; I_C = 25 mA	$V_{(BR)\ CEO}$	>	18	V
Emitter-base breakdown voltage				
open collector; I_E = 1 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 18 V	I_{CES}	<	2	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	0,5	mJ
R_{BE} = 10 Ω	E_{SBR}	>	0,5	mJ
D.C. current gain(1)		typ.	40	
I_C = 0,75 A; V_{CE} = 5 V	h_{FE}		10 to 100	
Collector-emitter saturation voltage(1)				
I_C = 2 A; I_B = 0,4 A	V_{CEsat}	typ.	0,85	V
Transition frequency at f = 100 MHz(1)				
$-I_E$ = 0,75 A; V_{CB} = 13,5 V	f_T	typ.	950	MHz
$-I_E$ = 2 A; V_{CB} = 13,5 V	f_T	typ.	850	MHz
Collector capacitance at f = 1 MHz				
I_E = I_e = 0; V_{CB} = 13,5 V	C_c	typ.	16,5	pF
Feedback capacitance at f = 1 MHz				
I_C = 100 mA; V_{CE} = 13,5 V	C_{re}	typ.	12	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0,02$.

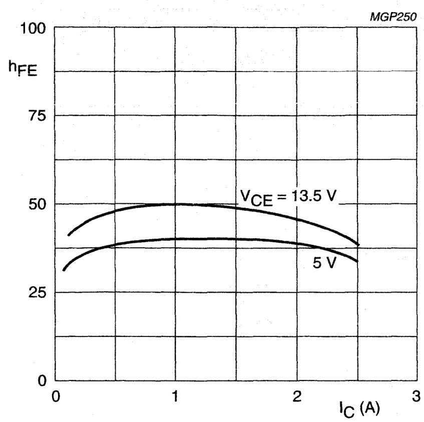


Fig.4 Typical values; T_j = 25 °C.

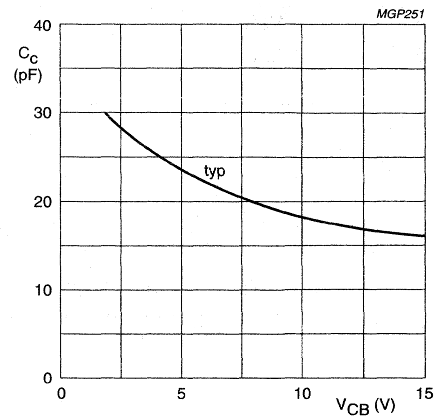


Fig.5 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

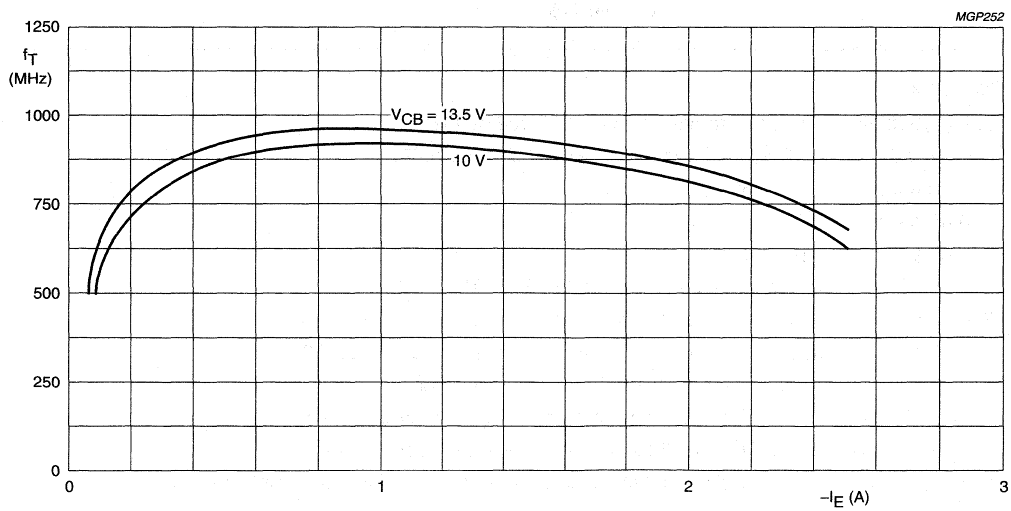


Fig.6 Typical values; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit)
T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_P (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
175	**13,5**	**8**	**< 1,0**	**> 9,0**	**< 0,85**	**> 70**	**2,8 + j1,2**	**76 − j16**
175	12,5	8	−	typ. 10,5	−	typ. 75	−	−

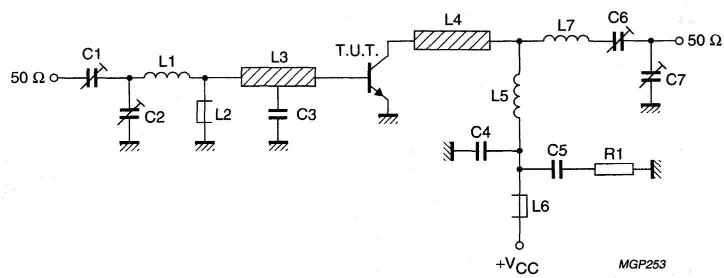


Fig.7 Test circuit; c.w. class-B.

List of components:

C1 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C2 = C6 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C3 = 47 pF ceramic capacitor (500 V)
C4 = 120 pF ceramic capacitor (500 V)
C5 = 100 nF polyester capacitor
C7 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
L1 = 2 turns Cu wire (1,6 mm); int. dia. 4,5 mm; length 5,7 mm; leads 2 × 5 mm
L2 = L6 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3 = L4 = strip (12 mm × 6 mm); tap for C3 at 5 mm from transistor
L5 = 3 turns Cu wire (1,6 mm); int. dia. 7,5 mm; length 7,5 mm; leads 2 × 5 mm
L7 = 3 turns Cu wire (1,6 mm); int. dia. 6,5 mm; length 7,4 mm; leads 2 × 5 mm
L3 and L4 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16".
R1 = 10 Ω carbon resistor

Component layout and printed-circuit board for 175 MHz test circuit see Fig.8.

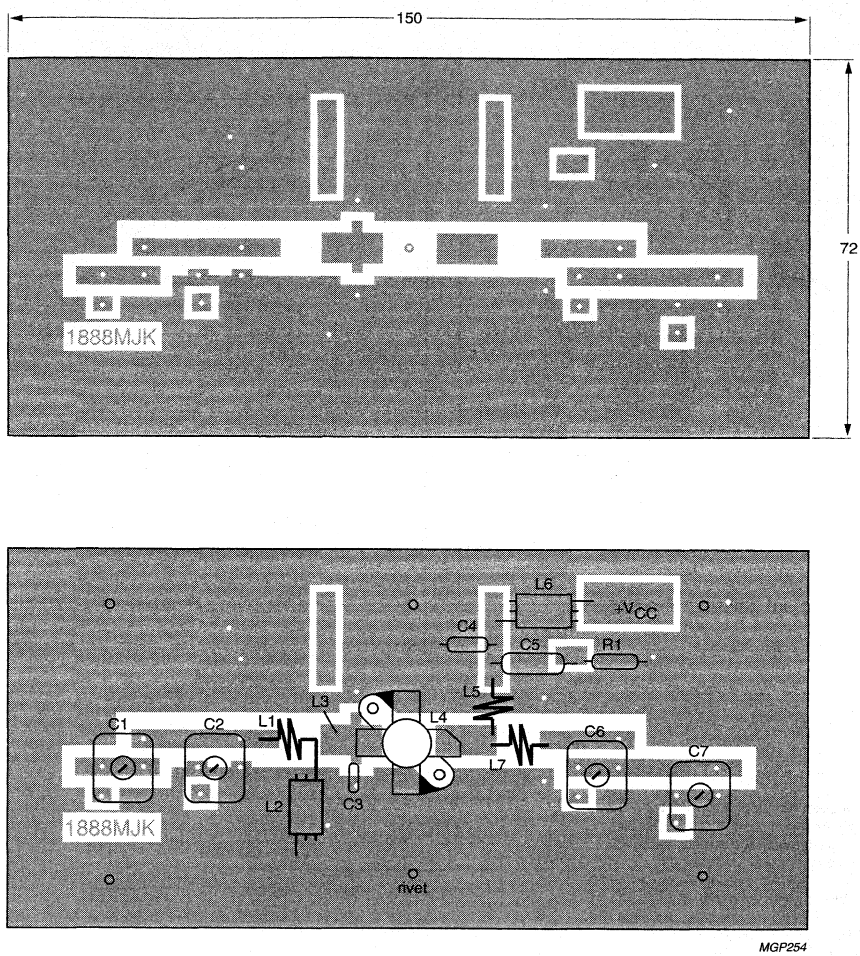
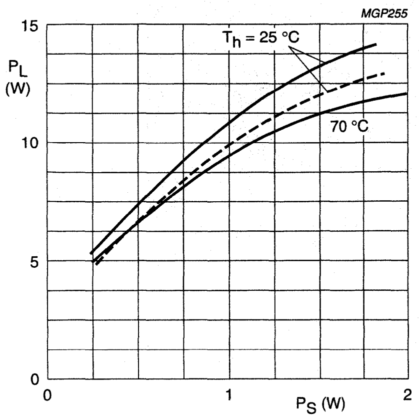


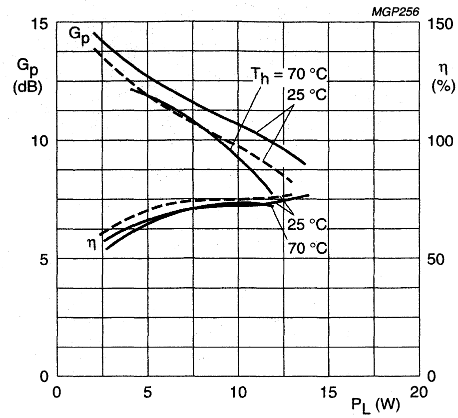
Fig.8 Component layout and printed-circuit board for 175 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.



—— V_{CE} = 13,5 V;
- - - V_{CE} = 12,5 V.

Fig.9 Typical values; f = 175 MHz;



—— V_{CE} = 13,5 V;
- - - V_{CE} = 12,5 V.

Fig.10 Typical values; f = 175 MHz;

The transistor has been developed for use with unstabilized supply voltages. As the output power and drive power increase with the supply voltage, the nominal output power must be derated in accordance with the graph for safe operation at supply voltages other than the nominal. The graph shows the permissible output power under nominal conditions (VSWR = 1), as a function of the expected supply over-voltage ratio with VSWR as parameter.

The graph applies to the situation in which the drive (P_S/P_{Snom}) increases linearly with supply over-voltage ratio.

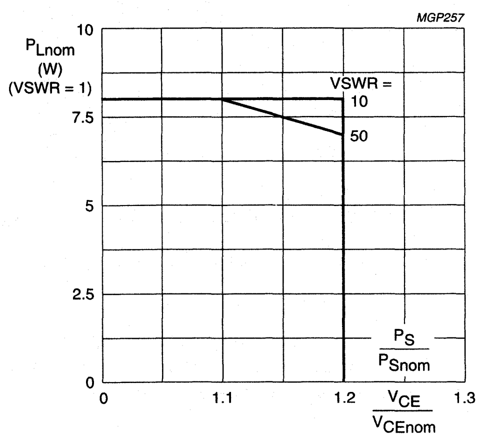
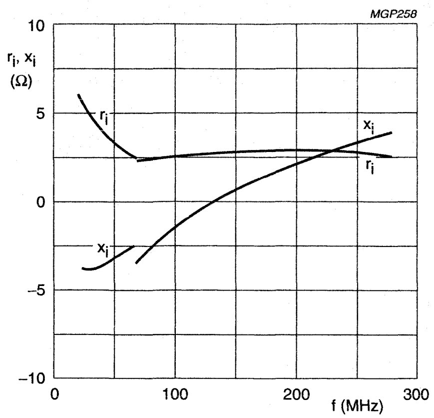
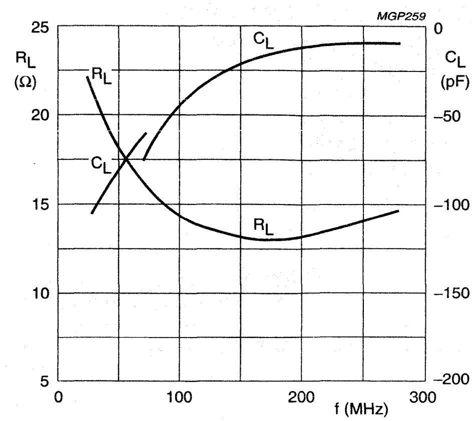


Fig.11 R.F. SOAR (short-time operation during mismatch); f = 175 MHz; T_h = 70 °C; $R_{th\ mb-h}$ = 0,3 K/W; V_{CEnom} = 13,5 V or 12,5 V; $P_S = P_{Snom}$ at V_{CEnom} and VSWR = 1.



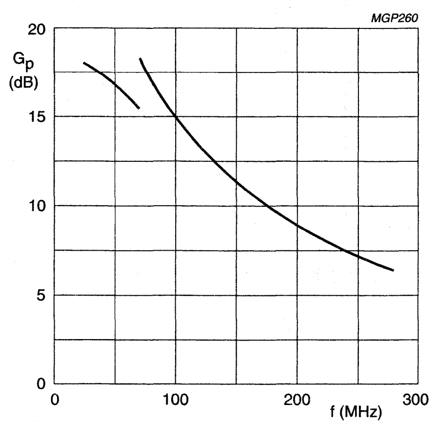
Typical values; V_{CE} = 13,5 V; P_L = 8 W;
T_h = 25 °C

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 13,5 V; P_L = 8 W;
T_h = 25 °C

Fig.13 Load impedance (parallel components).



Typical values; V_{CE} = 13,5 V; P_L = 8 W;
T_h = 25 °C

Fig.14

OPERATING NOTE

Below 70 MHz a base-emitter resistor of 10 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.

VHF power transistor

BLV11

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, B and C operated mobile, h.f. and v.h.f. transmitters with a nominal supply voltage of 13,5 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions with a supply over-voltage to 16,5 V.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in an unneutralized common-emitter class-B circuit

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	$\overline{z_i}$ Ω	$\overline{Y_L}$ mS
c.w.	**13,5**	**175**	**15**	> **8,0**	> **60**	**2,3 + j2,2**	**130 − j4,4**
c.w.	12,5	175	15	typ. 7,5	typ. 67	–	–

PIN CONFIGURATION

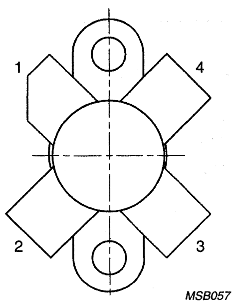


Fig.1 Simplified outline, SOT123.

PINNING

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage ($V_{BE} = 0$)				
peak value	V_{CESM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	18	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	3	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	8	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	36	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

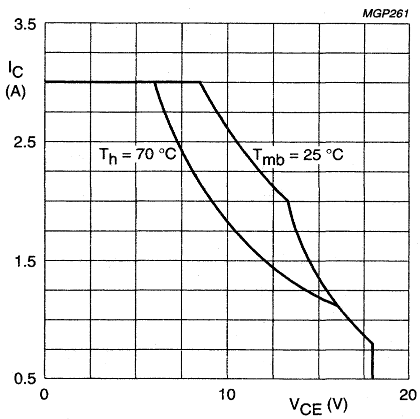
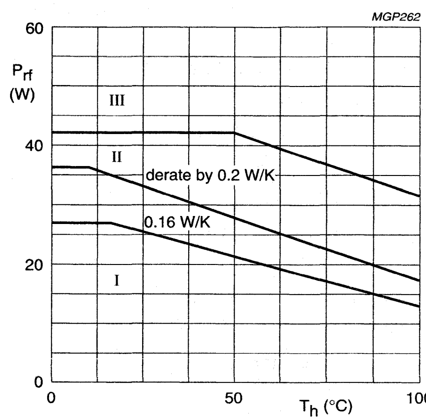


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \leq 16,5$ V; f > 1 MHz.

THERMAL RESISTANCE

(dissipation = 15 W; T_{mb} = 74,5 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j-mb(dc)}$	=	6,55	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j-mb(rf)}$	=	4,95	K/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0,3	K/W

CHARACTERISTICS

$T_j = 25\ °C$

Collector-emitter breakdown voltage					
$V_{BE} = 0$; $I_C = 10$ mA	$V_{(BR)CES}$	>		36	V
Collector-emitter breakdown voltage					
open base; $I_C = 50$ mA	$V_{(BR)CEO}$	>		18	V
Emitter-base breakdown voltage					
open collector; $I_E = 4$ mA	$V_{(BR)EBO}$	>		4	V
Collector cut-off current					
$V_{BE} = 0$; $V_{CE} = 18$ V	I_{CES}	<		4	mA
Second breakdown energy; L = 25 mH; f = 50 Hz					
open base	E_{SBO}	>		2,5	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>		2,5	mJ
D.C. current gain (1)		typ.		40	
$I_C = 1,5$ A; $V_{CE} = 5$ V	h_{FE}		10 to	100	
Collector-emitter saturation voltage (1)					
$I_C = 4,5$ A; $I_B = 0,9$ A	V_{CEsat}	typ.		1,0	V
Transition frequency at f = 100 MHz (1)					
$-I_E = 1,5$ A; $V_{CB} = 13,5$ V	f_T	typ.		850	MHz
$-I_E = 4,5$ A; $V_{CB} = 13,5$ V	f_T	typ.		800	MHz
Collector capacitance at f = 1 MHz					
$I_E = I_e = 0$; $V_{CB} = 13,5$ V	C_c	typ.		32	pF
Feedback capacitance at f = 1 MHz					
$I_C = 200$ mA; $V_{CE} = 13,5$ V	C_{re}	typ.		23	pF
Collector-flange capacitance	C_{cf}	typ.		2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0,02$.

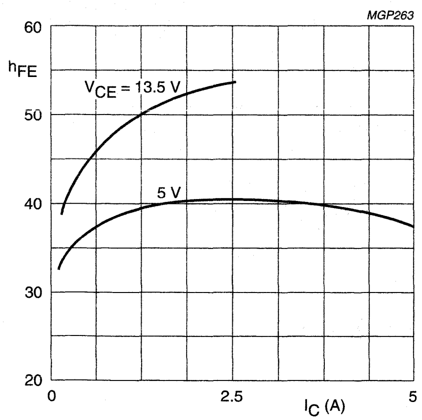


Fig.4 Typical values; T_j = 25 °C.

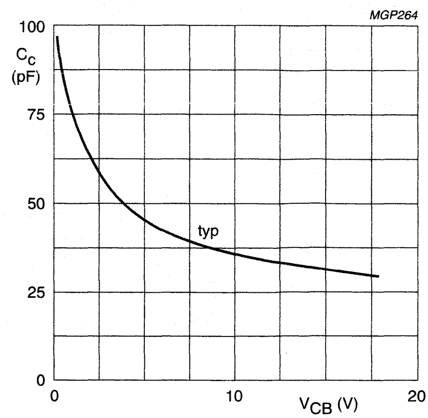


Fig.5 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

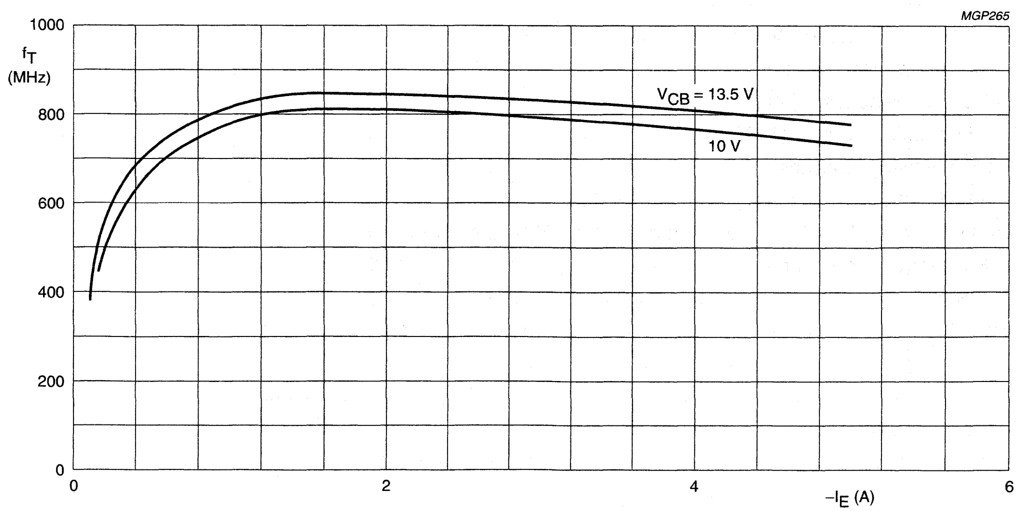


Fig.6 Typical values; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R. F. performance in c.w. operation (unneutralized common-emitter class-B circuit)
T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_p (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
175	**13,5**	**15**	**< 2,4**	**> 8,0**	**< 1,85**	**> 60**	**2,3 + j2,2**	**130 − j4,4**
175	12,5	15	−	typ. 7,5	−	typ. 67	−	−

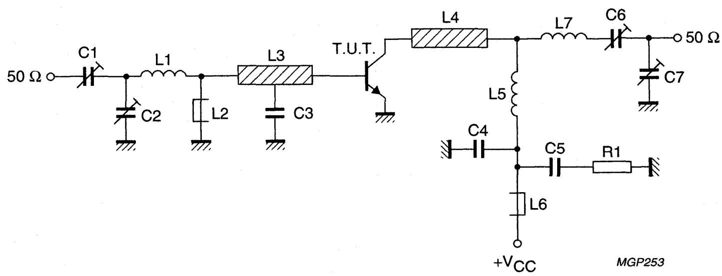


Fig.7 Test circuit; c.w. class-B.

List of components:

C1 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C2 = C6 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C3 = 47 pF ceramic capacitor (500 V)
C4 = 120 pF ceramic capacitor (500 V)
C5 = 100 nF polyester capacitor
C7 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
L1 = 2 turns Cu wire (1,6 mm); int. dia. 4,5 mm; length 5,7 mm; leads 2 × 5 mm
L2 = L6 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3 = L4 = strip (12 mm × 6 mm); tap for C3 at 5 mm from transistor
L5 = 3 turns Cu wire (1,6 mm); int. dia. 7,5 mm; length 7,5 mm; leads 2 × 5 mm
L7 = 3 turns Cu wire (1,6 mm); int. dia. 6,5 mm; length 7,4 mm; leads 2 × 5 mm
L3 and L4 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16".
R1 = 10 Ω carbon resistor
Component layout and printed-circuit board for 175 MHz test circuit see Fig.8.

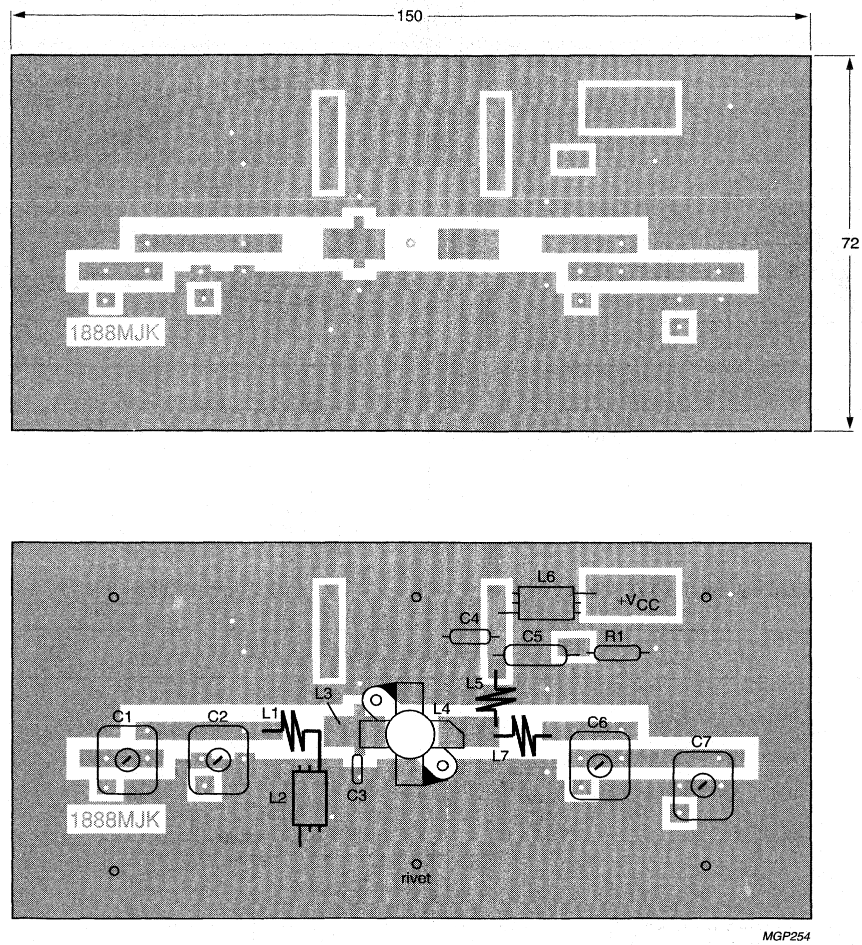
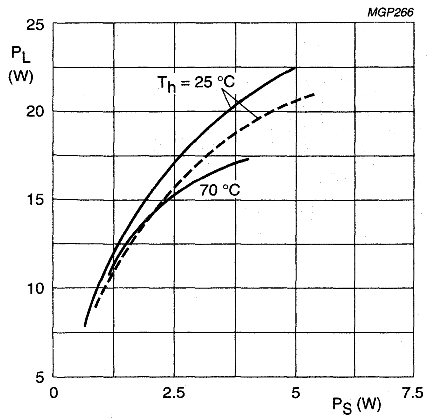


Fig.8 Component layout and printed-circuit board for 175 MHz test circuit.

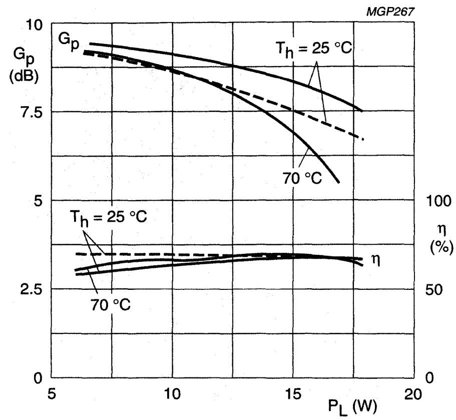
The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

VHF power transistor BLV11



—— V_{CE} = 13,5 V;
- - - V_{CE} = 12,5 V.

Fig.9 Typical values; f = 175 MHz;



—— V_{CE} = 13,5 V;
- - - V_{CE} = 12,5 V.

Fig.10 Typical values; f = 175 MHz.

The transistor has been developed for use with unstabilized supply voltages. As the output power and drive power increase with the supply voltage, the nominal output power must be derated in accordance with the graph for safe operation at supply voltages other than the nominal. The graph shows the permissible output power under nominal conditions (VSWR = 1), as a function of the expected supply over-voltage ratio with VSWR as parameter.

The graph applies to the situation in which the drive (P_S/P_{Snom}) increases linearly with supply over-voltage ratio.

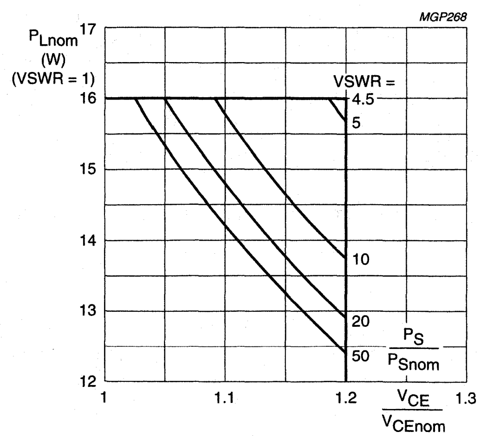
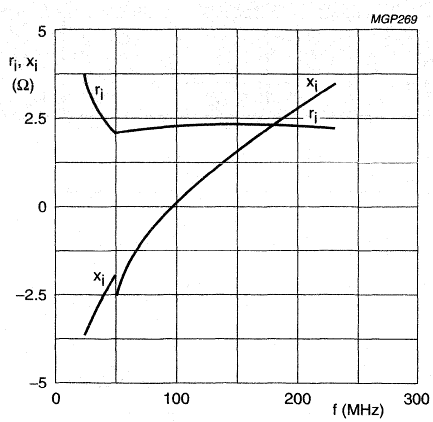
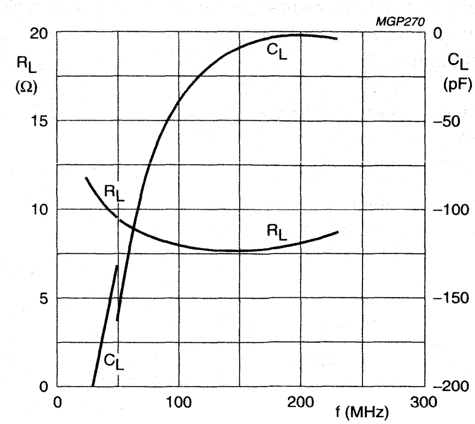


Fig.11 R.F. SOAR (short-time operation during mismatch); f = 175 MHz; T_h = 70 °C; $R_{th\ mb\text{-}h}$ = 0,3 K/W; V_{CEnom} = 13,5 V or 12,5 V; $P_S = P_{Snom}$ at V_{CEnom} and VSWR = 1.



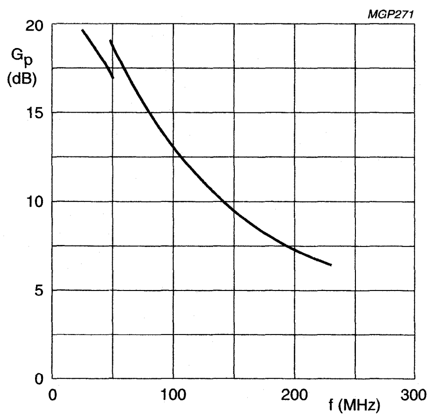
Typical values: V_{CE} = 13,5 V;
P_L = 15 W;
T_h = 25 °C

Fig.12 Input impedance (series components).



Typical values: V_{CE} = 13,5 V;
P_L = 15 W;
T_h = 25 °C

Fig.13 Load impedance (parallel components).



Typical values: V_{CE} = 13,5 V;
P_L = 15 W;
T_h = 25 °C

Fig.14

OPERATING NOTE

Below 50 MHz a base-emitter resistor of 10 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.

VHF power transistor BLV20

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, B and C operated h.f. and v.h.f. transmitters with a nominal supply voltage of 28 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT123

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in an unneutralized common-emitter class-B circuit

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	$\bar{z}_i$ Ω	$\bar{Y}_L$ mS
c.w.	28	175	8	> 12	> 65	1,8 + j0,7	18 − j20

PIN CONFIGURATION

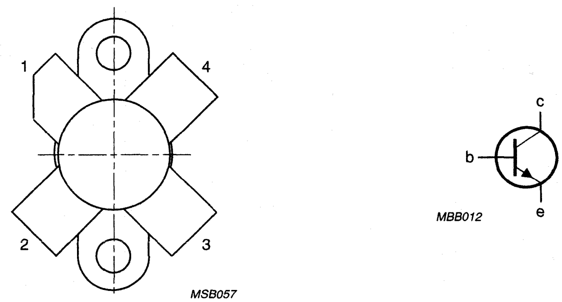


Fig.1 Simplified outline and symbol.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage ($V_{BE} = 0$)			
peak value	V_{CESM}	max.	65 V
Collector-emitter voltage (open base)	V_{CEO}	max.	36 V
Emitter-base voltage (open collector)	V_{EBO}	max.	4 V
Collector current (average)	$I_{C(AV)}$	max.	0,9 A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	2,5 A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	20 W
Storage temperature	T_{stg}		−65 to + 150 °C
Operating junction temperature	T_j	max.	200 °C

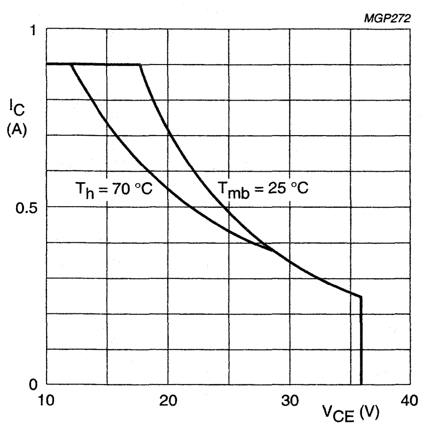
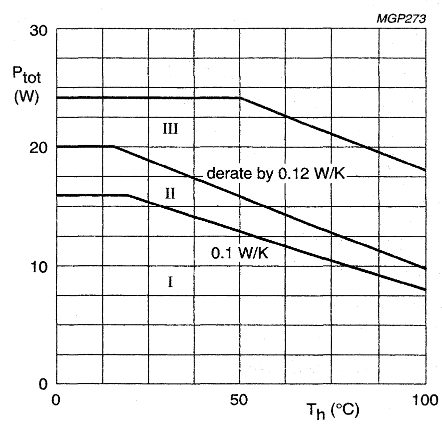


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \le 28$ V; f > 1 MHz.

THERMAL RESISTANCE

(dissipation = 8 W; T_{mb} = 72,4 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j-mb(dc)}$	=	10,7 K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j-mb(rf)}$	=	8,6 K/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0,3 K/W

CHARACTERISTICS

$T_j = 25\ °C$

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 2$ mA	$V_{(BR)CES}$	>	65	V
Collector-emitter breakdown voltage				
open base; $I_C = 10$ mA	$V_{(BR)CEO}$	>	36	V
Emitter-base breakdown voltage				
open collector; $I_E = 1$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 36$ V	I_{CES}	<	1	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	0,5	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>	0,5	mJ
D.C. current gain (1)	h_{FE}	typ.	50	
$I_C = 0,4$ A; $V_{CE} = 5$ V		10 to	100	
Collector-emitter saturation voltage (1)				
$I_C = 1,25$ A; $I_B = 0,25$ A	V_{CEsat}	typ.	0,8	V
Transition frequency at f = 100 MHz (1)				
$-I_E = 0,4$ A; $V_{CB} = 28$ V	f_T	typ.	600	MHz
$-I_E = 1,25$ A; $V_{CB} = 28$ V	f_T	typ.	520	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 28$ V	C_c	typ.	10	pF
Feedback capacitance at f = 1 MHz				
$I_C = 50$ mA; $V_{CE} = 28$ V	C_{re}	typ.	7,1	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0,02$.

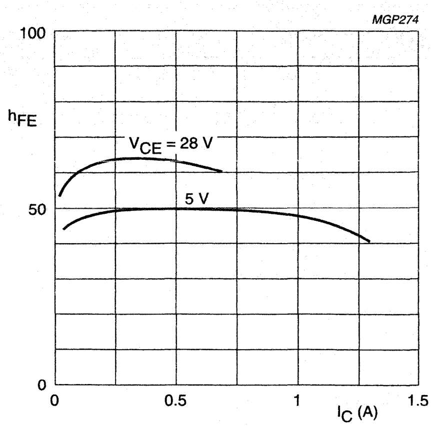


Fig.4 Typical values; T_j = 25 °C.

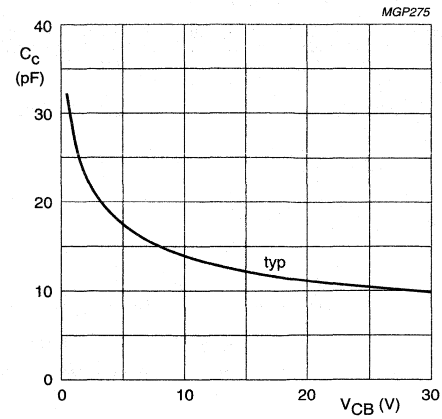


Fig.5 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

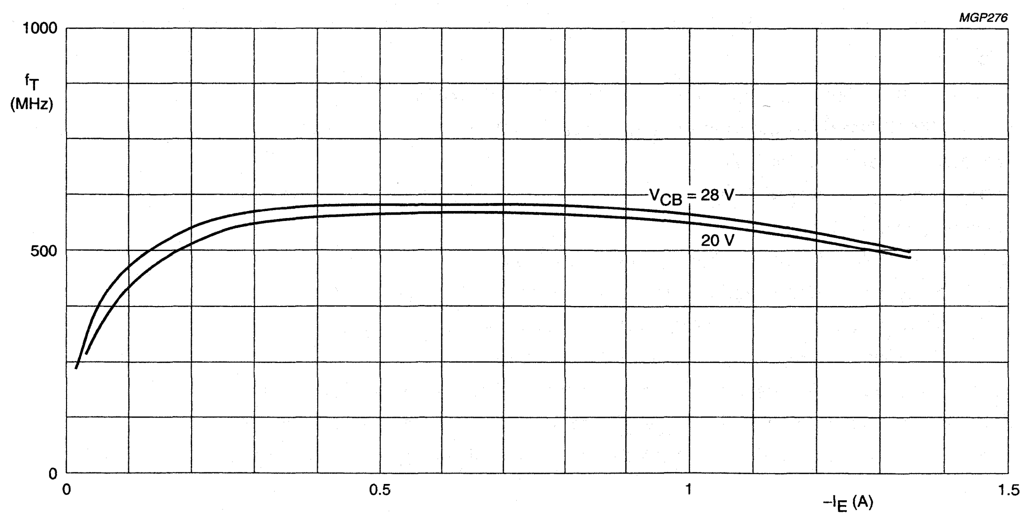


Fig.6 Typical values; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R. F. performance in c.w. operation (unneutralized common-emitter class-B circuit)
T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_p (dB)	I_C (A)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mS)
175	28	8	< 0,5	> 12	< 0,44	> 65	1,8 + j0,7	18 – j20

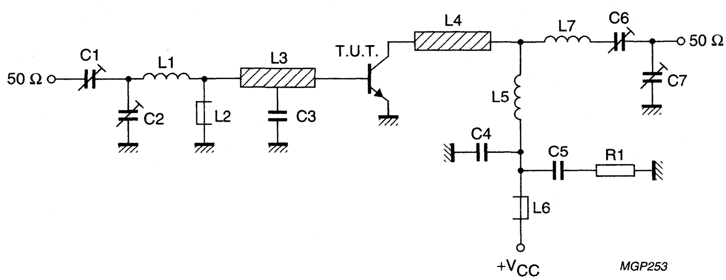


Fig.7 Test circuit; c.w. class-B.

List of components:

C1 = C7 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C2 = C6 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
C3 = 27 pF ceramic capacitor (500 V)
C4 = 120 pF ceramic capacitor (500 V)
C5 = 100 nF polyester capacitor
L1 = 1 turn Cu wire (1,6 mm); int. dia. 8,4 mm; leads 2 × 5 mm
L2 = 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 × 5 mm
L3 = L8 = Ferroxcube wide band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4 = L5 = strip (12 mm × 6 mm); tap for C3 at 5 mm from transistor
L6 = 3 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 9,0 mm; leads 2 × 5 mm
L7 = 3 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 8,2 mm; leads 2 × 5 mm
L4 and L5 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16".
R1 = R2 = 10 Ω carbon resistor
Component layout and printed-circuit board for 175 MHz test circuit see Fig.8.

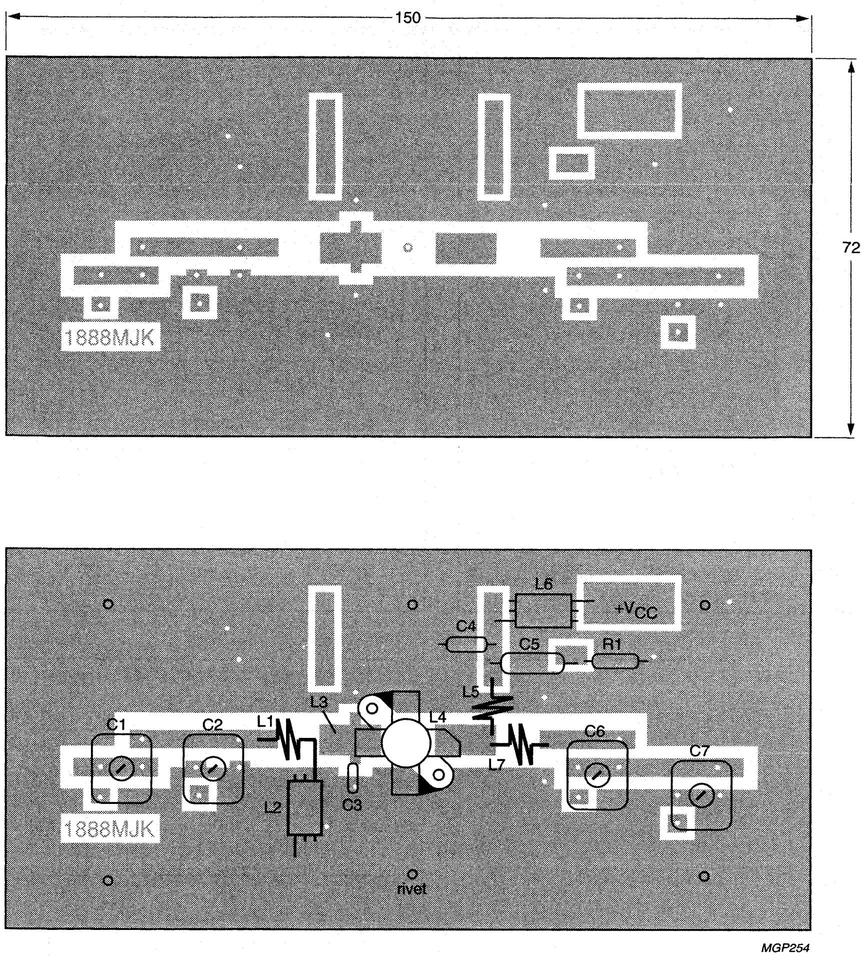


Fig.8 Component layout and printed-circuit board for 175 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

VHF power transistor BLV20

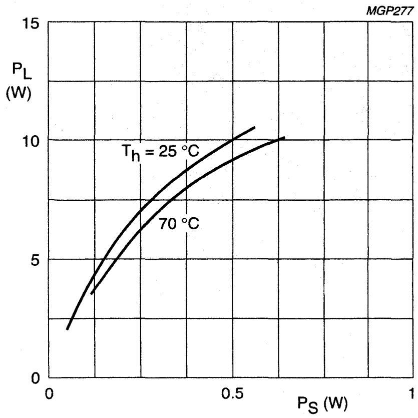


Fig.9 Typical values; V_{CE} = 28 V; f = 175 MHz.

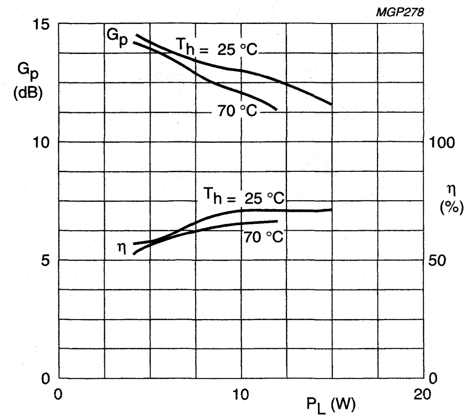


Fig.10 Typical values; V_{CE} = 28 V; f = 175 MHz.

The graph shows the permissible output power under nominal conditions (VSWR = 1) as a function of the expected VSWR during short-time mismatch conditions with heatsink temperatures as parameter.

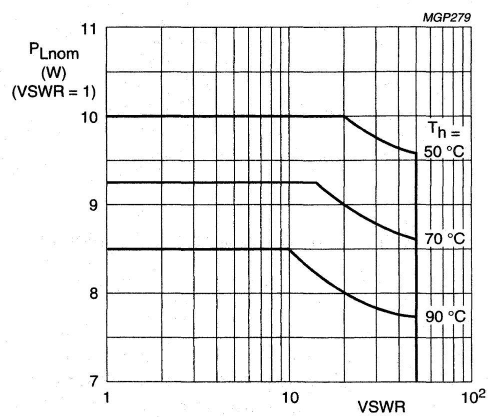
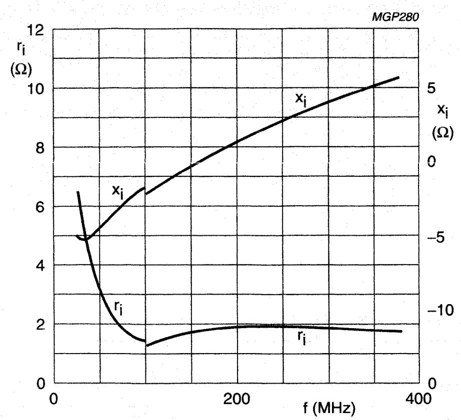
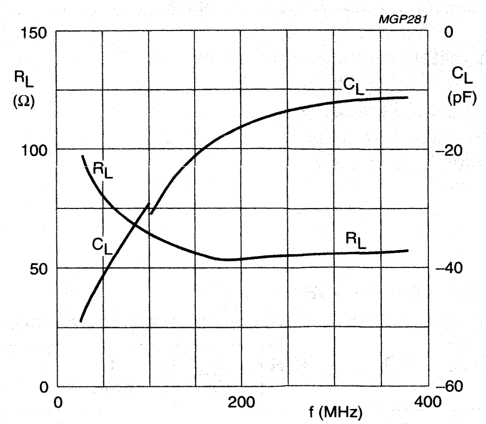


Fig.11 R.F. SOAR; c.w. class-B operation; f = 175 MHz; V_{CE} = 28 V; $R_{th\ mb-h}$ = 0,3 K/W.



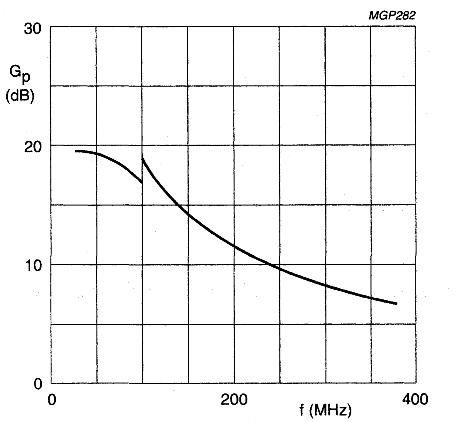
Typical values; V_{CE} = 28 V;
P_L = 8 W;
T_h = 25 °C

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 28 V;
P_L = 8 W;
T_h = 25 °C

Fig.13 Load impedance (parallel components).



Typical values; V_{CE} = 28 V;
P_L = 8 W;
T_h = 25 °C

Fig.14

OPERATING NOTE

Below 100 MHz a base-emitter resistor of 10 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.

VHF power transistor — BLV21

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, B and C operated h.f. and v.h.f. transmitters with a nominal supply voltage of 28 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in an unneautralized common-emitter class-B circuit

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	$\bar{z}_i$ Ω	$\bar{Y}_L$ mS
c.w.	28	175	15	> 10	> 65	1,4 + j1,85	33 – j27,5

PIN CONFIGURATION

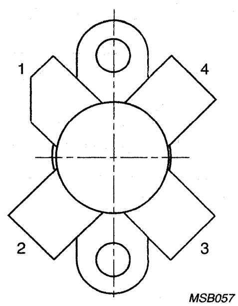


Fig.1 Simplified outline, SOT123.

PINNING

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage ($V_{BE} = 0$)				
peak value	V_{CESM}	max.	65	V
Collector-emitter voltage (open base)	V_{CEO}	max.	36	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	1,75	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	5,0	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	36	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

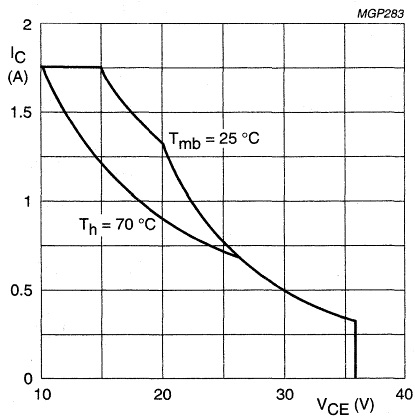
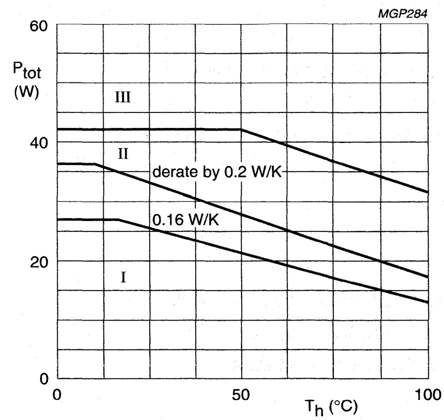


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \leq 28$ V; f > 1 MHz.

THERMAL RESISTANCE

(dissipation = 15 W; T_{mb} = 74,5 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	6,55	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	4,95	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3	K/W

CHARACTERISTICS

$T_j = 25\ °C$				
Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 5$ mA	$V_{(BR)\,CES}$	>	65	V
Collector-emitter breakdown voltage				
open base; $I_C = 25$ mA	$V_{(BR)\,CEO}$	>	36	V
Emitter-base breakdown voltage				
open collector; $I_E = 2$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 36$ V	I_{CES}	<	2	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	2,5	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>	2,5	mJ
D.C. current gain(1)		typ.	50	
$I_C = 0,7$ A; $V_{CE} = 5$ V	h_{FE}	10 to 100		
Collector-emitter saturation voltage(1)				
$I_C = 2$ A; $I_B = 0,4$ A	V_{CEsat}	typ.	0,65	V
Transition frequency at f = 100 MHz(1)				
$-I_E = 0,7$ A; $V_{CB} = 28$ V	f_T	typ.	650	MHz
$-I_E = 2$ A; $V_{CB} = 28$ V	f_T	typ.	625	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 28$ V	C_c	typ.	18	pF
Feedback capacitance at f = 1 MHz				
$I_C = 100$ mA; $V_{CE} = 28$ V	C_{re}	typ.	12,8	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0,02$.

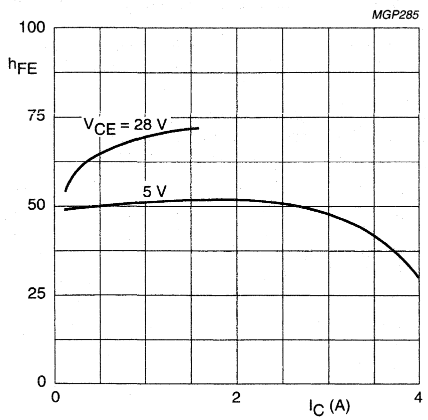


Fig.4 Typical values; T_j = 25 °C.

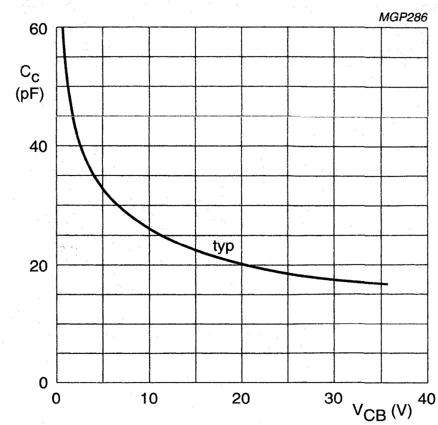


Fig.5 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

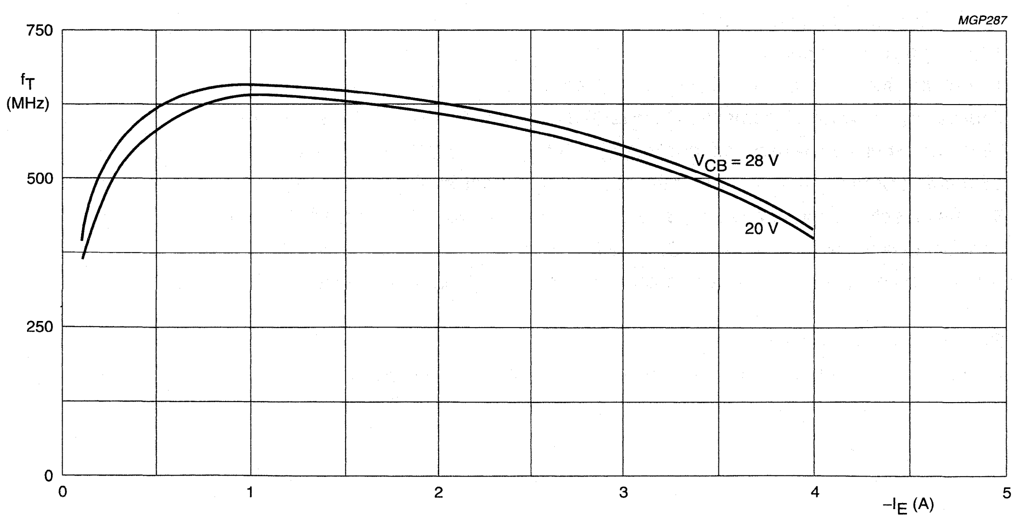


Fig.6 Typical values; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit) T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_P (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
175	28	15	< 1,5	> 10	< 0,83	> 65	1,4 + j1,85	33 – j27,5

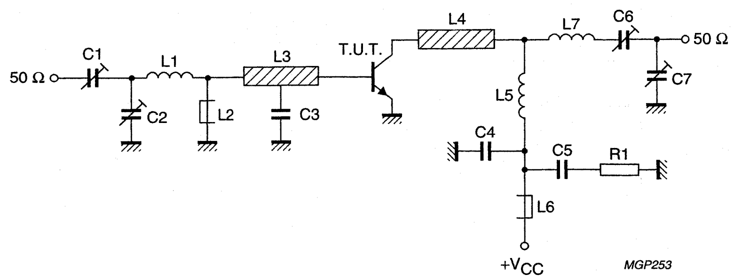


Fig.7 Test circuit; c.w. class-B.

List of components:

C1 = C7 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C2 = C6 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
C3 = 27 pF ceramic capacitor (500 V)
C4 = 120 pF ceramic capacitor (500 V)
C5 = 100 nF polyester capacitor
L1 = 1 turn Cu wire (1,6 mm); int. dia. 8,4 mm; leads 2 × 5 mm
L2 = 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 × 5 mm
L3 = L8 = Ferroxcube wide band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4 = L5 = strip (12 mm × 6 mm); tap for C3 at 5 mm from transistor
L6 = 3 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 9,0 mm; leads 2 × 5 mm
L7 = 3 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 8,2 mm; leads 2 × 5 mm

L4 and L5 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16".

R1 = R2 = 10 Ω carbon resistor

Component layout and printed-circuit board for 175 MHz test circuit see Fig.8.

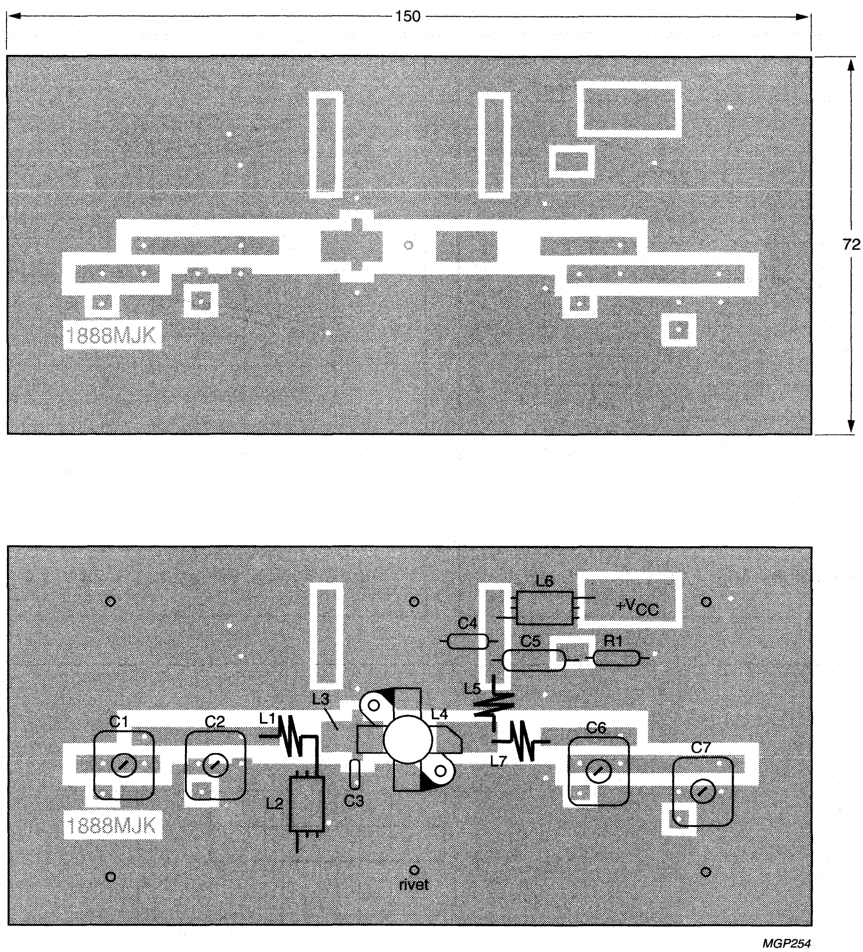


Fig.8 Component layout and printed-circuit board for 175 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

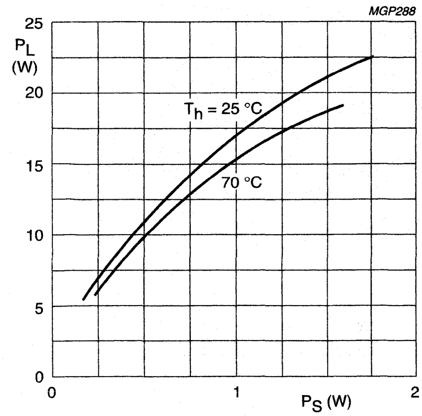


Fig.9 Typical values; V_{CE} = 28 V; f = 175 MHz.

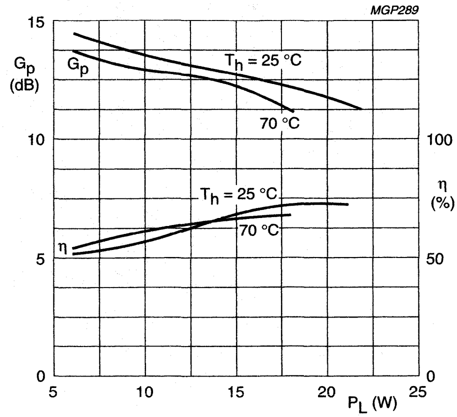
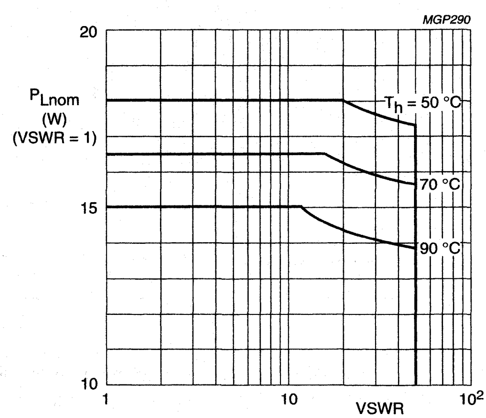
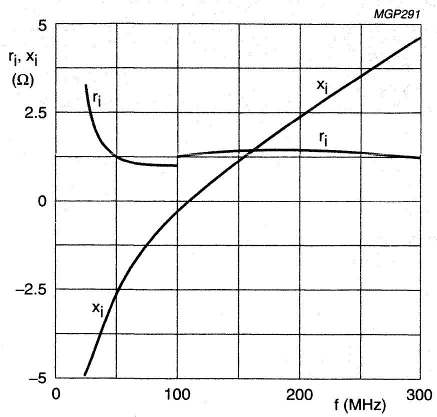


Fig.10 Typical values; V_{CE} = 28 V; f = 175 MHz.



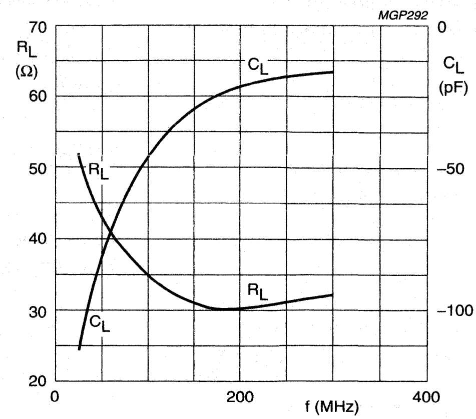
The graph shows the permissible output power under nominal conditions (VSWR = 1) as a function of the expected VSWR during short-time mismatch conditions with heatsink temperatures as parameter.

Fig.11 R.F. SOAR; c.w. class-B operation; f = 175 MHz; V_{CE} = 28 V; $R_{th\ mb\text{-}h}$ = 0,3 K/W



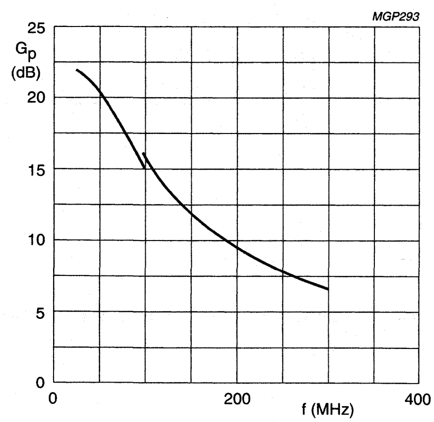
Typical values; V_{CE} = 28 V;
P_L = 15 W; T_h = 25 °C

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 28 V;
P_L = 15 W; T_h = 25 °C

Fig.13 Load impedance (parallel components).



Typical values; V_{CE} = 28 V;
P_L = 15 W; T_h = 25 °C

Fig.14

OPERATING NOTE

Below 100 MHz a base-emitter resistor of 10 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.

VHF power transistor BLV25

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily for use in v.h.f.-f.m. broadcast transmitters.

FEATURES

- internally matched input for wideband operation and high power gain;
- multi-base structure and diffused emitter ballasting resistors for an optimum temperature profile;
- gold-metallization ensures excellent reliability.

The transistor has a ½in 6-lead flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in an unneutralized common-emitter class-B circuit.

MODE OPERATION	V_{CE} V	f MHz	P_L W	P_S W	G_p dB	η %
narrow band; c.w.	28	108	175	< 17,5	> 10,0	> 65

PIN CONFIGURATION

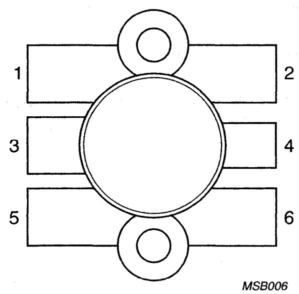


Fig.1 Simplified outline, SOT119A.

PINNING

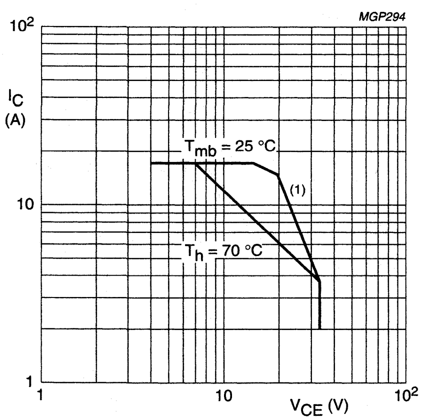
PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

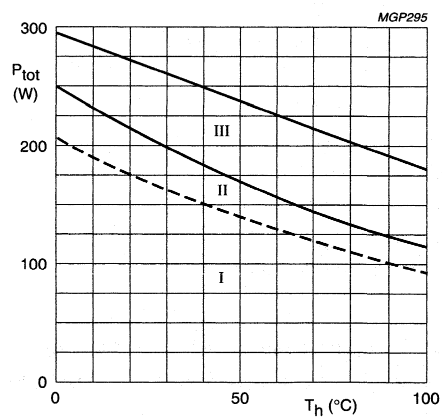
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage						
(peak value); $V_{BE} = 0$	V_{CESM}	max.			65	V
open base	V_{CEO}	max.			33	V
Emitter-base voltage (open collector)	V_{EBO}	max.			4	V
Collector current						
d.c. or average	I_C; $I_{C(AV)}$	max.			17, 5	A
(peak value); f > 1 MHz	I_{CM}	max.			35	A
Total power dissipation at $T_{mb} = 25$ °C	$P_{tot\ (d.c.)}$	max.			220	W
R.F. power dissipation (f > 1 MHz); $T_{mb} = 25$ °C	$P_{tot\ (r.f.)}$	max.			270	W
R.F. power dissipation (f > 1 MHz); $T_h = 70$ °C	$P_{tot\ (r.f.)}$	max.			146	W
Storage temperature	T_{stg}		−65	to	+150	°C
Operating junction temperature	T_j	max.			200	°C



(1) Second breakdown limit.

Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation (f > 1 MHz)
III Short-time operation during mismatch; (f > 1 MHz).

Fig.3 Power derating curves vs. temperature.

THERMAL RESISTANCE

(dissipation = 150 W; $T_{mb} = 72$ °C, i.e. $T_h = 42$ °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	max	0,85	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	max	0,60	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	max	0,2	K/W

CHARACTERISTICS

$T_j = 25$ °C

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 50$ mA	$V_{(BR)CES}$	>	65	V
open base; $I_C = 200$ mA	$V_{(BR)CEO}$	>	33	V
Emitter-base breakdown voltage				
open collector; $I_E = 20$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 33$ V	I_{CES}	<	25	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	20	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>	20	mJ
D.C. current gain(1)				
$I_C = 8{,}5$ A; $V_{CE} = 25$ V	h_{FE}	typ.	50	
			15 to 100	
Collector-emitter saturation voltage(1)				
$I_C = 20$ A; $I_B = 4{,}0$ A	V_{CEsat}	typ.	1,6	V
Transition frequency at f = 100 MHz(2)				
$-I_E = 8{,}5$ A; $V_{CB} = 25$ V	f_T	typ.	600	MHz
$-I_E = 20$ A; $V_{CB} = 25$ V	f_T	typ.	600	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 25$ V	C_c	typ.	275	pF
Feedback capacitance at f = 1 MHz				
$I_C = 100$ mA; $V_{CE} = 25$ V	C_{re}	typ.	155	pF
Collector-flange capacitance	C_{cf}	typ.	3	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300\ \mu s$; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50\ \mu s$; $\delta \leq 0{,}01$.

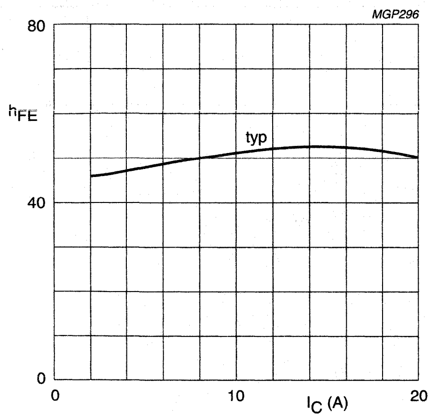


Fig.4 V_{CE} = 25 V; T_j = 25 °C.

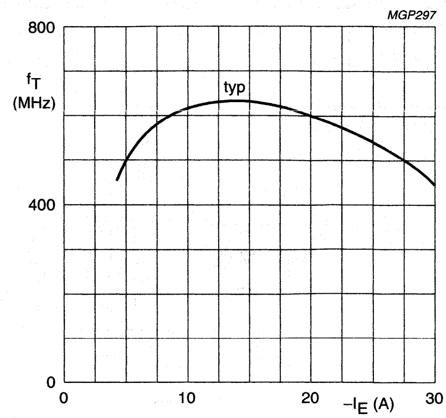


Fig.5 V_{CB} = 25 V; f = 100 MHz; T_j = 25 °C.

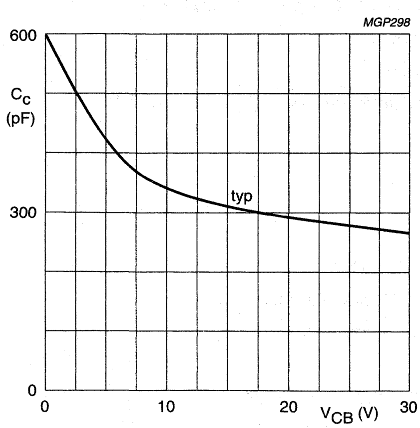


Fig.6 I_E = I_e = 0; f = 1 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in narrow band c.w. operation (common-emitter class-B circuit) T_h = 25 °C

f MHz	V_{CE} V	P_L W	P_S W	G_p dB	I_C A	η %
108	28	175	< 17,5	> 10,0	< 9,6	> 65
			typ. 13,9	typ. 11,0	typ. 8,9	typ. 70

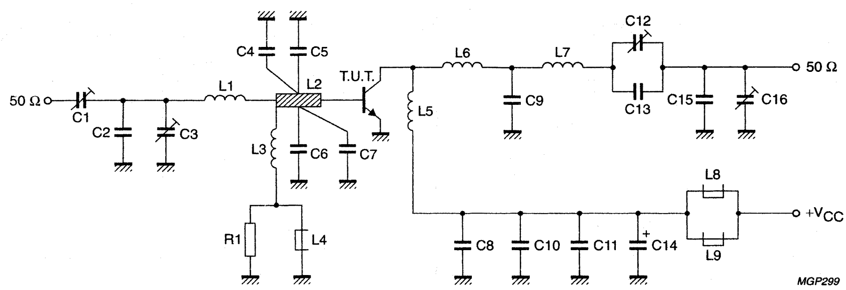


Fig.7 Class-B test circuit at f = 108 MHz.

List of components

C1 = C3 = 7 to 100 pF film dielectric trimmer (cat. no. 2222 809 07015)

C2 = C4 = C5 = C6 = C7 = 100 pF (500 V) multilayer ceramic chip capacitor (ATC[1]); except for C2 these capacitors are placed 7 mm from transistor edge

C8 = C10 = 470 pF multilayer ceramic chip capacitor (cat. no. 2222 856 13471)

C9 = C15 = 40 pF, parallel connection of 4 x 10 pF lead feed-through capacitors (cat. no. 2222 702 05109)

C11 = 100 nF multilayer ceramic chip capacitor (cat. no. 2222 852 59104)

C12 = C16 = 7 to 47 pF precision tuning capacitor (cat. no. 2222 805 00174)

C13 = 19 pF, parallel connection of 4 x 4,7 pF lead feed-through capacitors (cat. no. 2222 702 04478)

C14 = 6,8 µF/63 V electrolytic capacitor

L1 = Cu strip (10 mm × 4 mm × 0,5 mm)

L2 = strip on printed-circuit board

L3 = 7 turns closely wound enamelled Cu wire (0,3 mm); int. dia. 3,0 mm; leads 2 × 6 mm

L4 = L8 = L9 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)

L5 = 3 turns enamelled Cu wire (1,6 mm); int. dia. 8 mm; length 9 mm; leads 2 × 5 mm

L6 = Cu strip (27 mm × 9 mm × 0,5 mm)

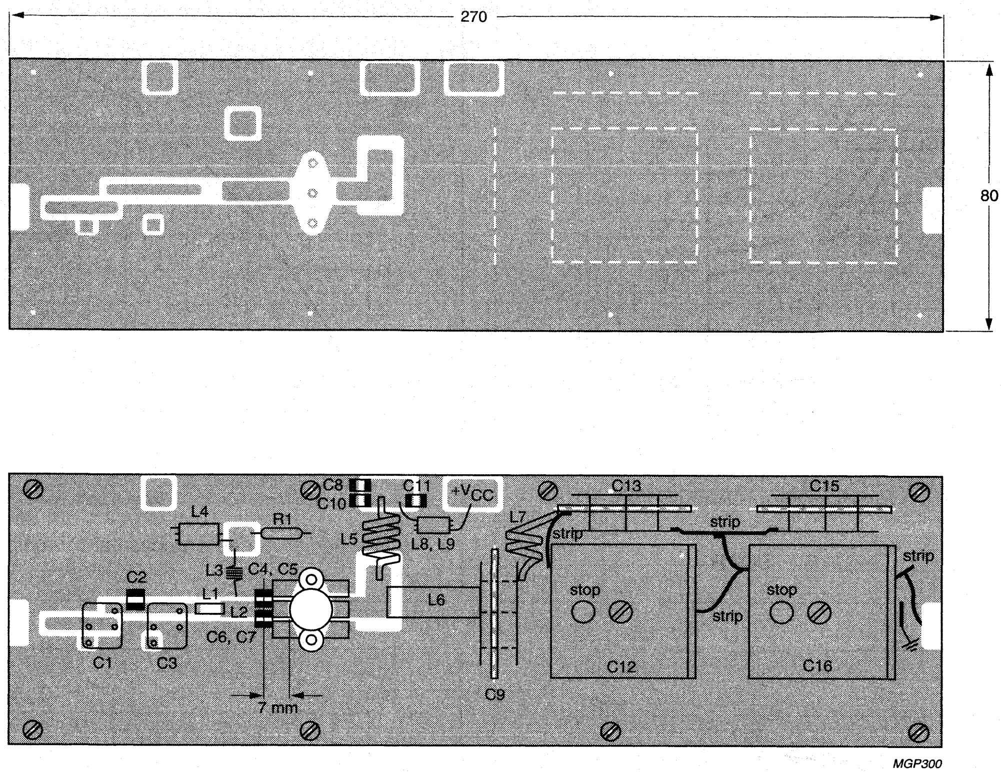
L7 = 2 turns enamelled Cu wire (1,6 mm); int. dia. 8 mm; length 9 mm; leads 2 × 10 mm

L2 is strip on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16 in.

R1 = 10 Ω carbon resistor

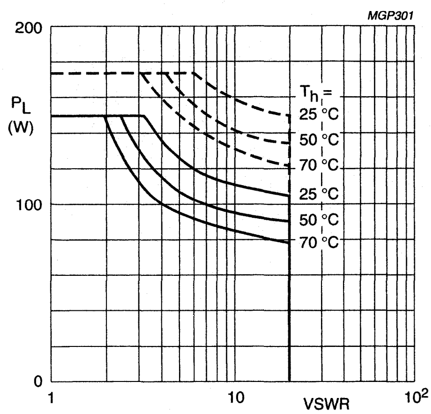
Note

1. ATC means American Technical Ceramics.



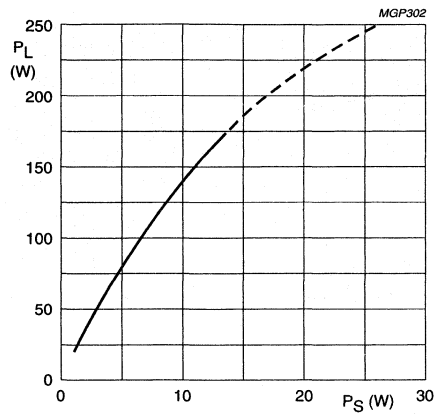
The circuit and the components are on one side of the epoxy fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by means of fixing screws. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

Fig.8 Component layout and printed-circuit board for 108 MHz class-B test circuit.



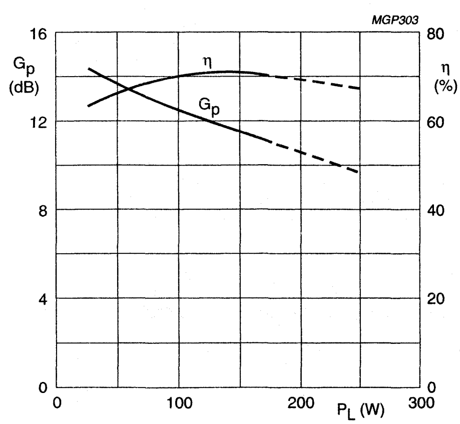
——— f > 1 MHz (continuous);
– – – – short time operation during mismatch (f > 1 MHz).

Fig.9 R.F. SOAR.



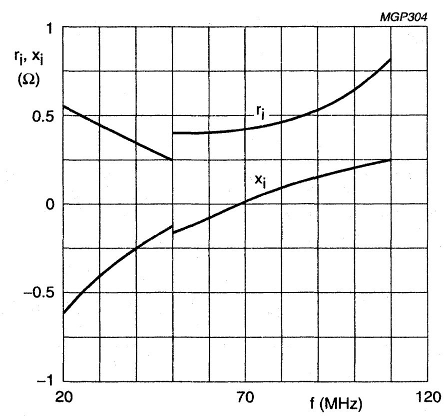
Test circuit tuned for each power level; typical values;
V_{CE} = 28 V; f = 108 MHz; T_h = 25 °C; class-B operation.

Fig.10 Load power as a function of source power.



Test circuit tuned for each power level; typical values;
V_{CE} = 28 V; f = 108 MHz; T_h = 25 °C; class-B operation.

Fig.11 Power gain and efficiency as a function of source power.

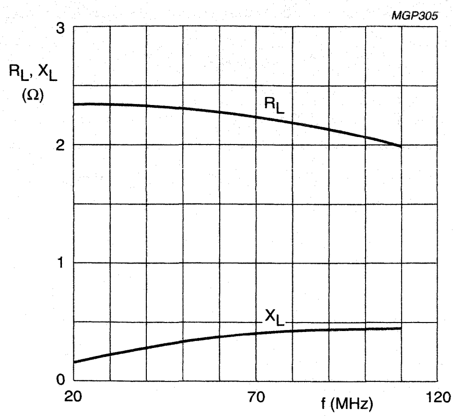


Typical values; V_{CE} = 28 V; P_L = 175 W;
T_h = 25 °C; class-B operation.

Fig.12 Input impedance (series components).

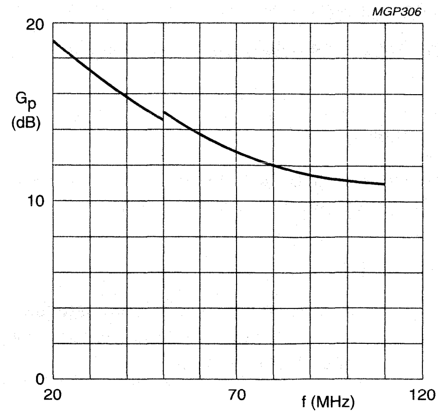
VHF power transistor

BLV25



Typical values; V_{CE} = 28 V; P_L = 175 W;
T_h = 25 °C; class-B operation.

Fig.13 Load impedance (series components).



Typical values; V_{CE} = 28 V; P_L = 175 W;
T_h = 25 °C; class-B operation.

Fig.14 Power gain as a function of frequency.

OPERATING NOTE for Figs 12, 13 and 14:
Below 50 MHz a base-emitter resistor of 4,7 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.

VHF linear power transistor — BLV33

FEATURES

- Diffused emitter ballasting resistors for an optimum temperature profile
- Gold sandwich metallization ensures excellent reliability.

APPLICATIONS

- Primarily intended for use in linear VHF amplifiers for television transmitters and transposers.

DESCRIPTION

NPN silicon planar epitaxial transistor encapsulated in a 1⁄16" 4 fslead SOT147 capstan package with ceramic cap. All leads are isolated from the stud.

PINNING - SOT147

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	e	emitter
3	b	base
4	e	emitter

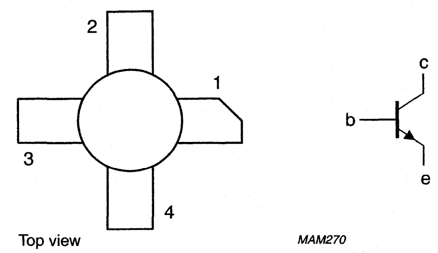


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance in a common emitter push-pull test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_C, $I_{C(ZS)}$ (A)	T_h (°C)	d_{im}(1) (dB)	$P_{o\ sync}$(1) (W)	G_P (dB)	sync compr.(2) sync in/sync out (%)
CW, class-A	224.25	25	3.2	70	−55	>16.5	>9	
				25	−55	typ. 26	typ. 9.7	
CW, class-AB	224.25	28	0.1	70		typ. 90	typ. 6.5	30/25

Notes

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
2. Television service (negative modulation, C.C.I.R. system).

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

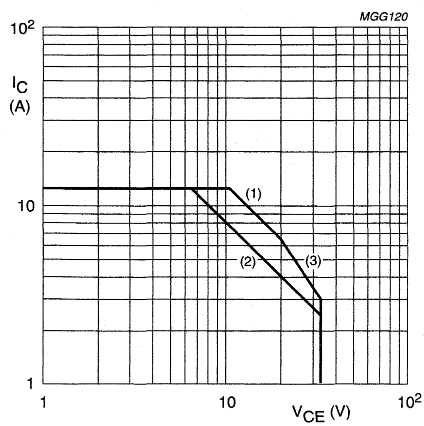
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter voltage	$V_{BE} = 0$	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	33	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current (DC)		–	12.5	A
$I_{C(AV)}$	average collector current		–	12.5	A
I_{CM}	peak collector current	f > 1 MHz	–	20	A
P_{tot}	total power dissipation (DC)	$T_{mb} = 25$ °C	–	132	W
P_{rf}	RF power dissipation	f > 1 MHz; $T_{mb} = 25$ °C	–	165	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

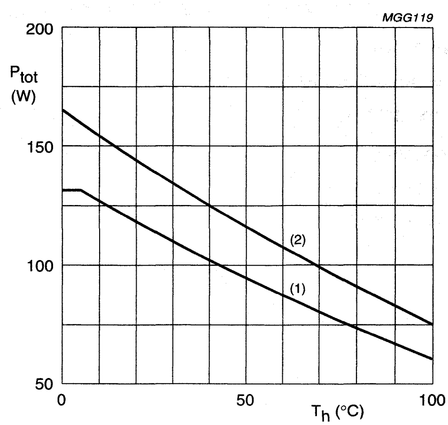
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb(dc)}$	thermal resistance from junction to mounting base (DC dissipation)	$P_{diss} = 80$ W; $T_{mb} = 82$ °C; $T_h = 70$ °C	1.46	K/W
$R_{th\ j\text{-}mb(rf)}$	thermal resistance from junction to mounting base (RF dissipation)	$P_{diss} = 80$ W; $T_{mb} = 82$ °C; $T_h = 70$ °C	1.17	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	$P_{diss} = 80$ W; $T_{mb} = 82$ °C; $T_h = 70$ °C	0.15	K/W



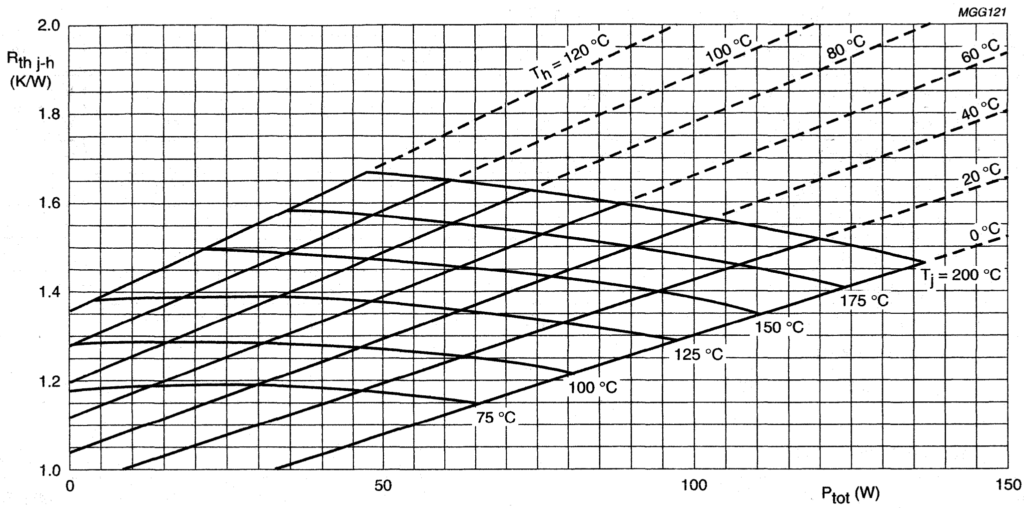
(1) $T_{mb} = 25$ °C.
(2) $T_h = 70$ °C.
(3) Second breakdown limit (independent of temperature).

Fig.2 DC SOAR.



(1) Continuous DC (including RF class-A) operation.
(2) Continuous RF operation.

Fig.3 Power derating curves.



$R_{th\ mb\text{-}h}$ = 0.15 K/W.

Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters.

Example

Nominal class-A operation: V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Figure 4 shows:

$R_{th\ j\text{-}h}$ = max. 1.60 K/W

T_j = max. 198 °C.

Typical device:

$R_{th\ j\text{-}h}$ = typ.1.50 K/W

T_j = typ. 190 °C.

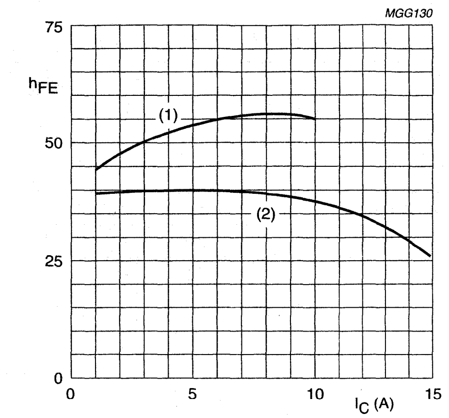
CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	collector-emitter breakdown voltage	$V_{BE} = 0$; $I_C = 25$ mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; $I_C = 100$ mA	33	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 10$ mA	4	–	–	V
I_{CES}	collector cut-off current	$V_{BE} = 0$; $V_{CE} = 30$ V	–	–	1	mA
h_{FE}	DC current gain	$V_{CE} = 25$ V; $I_C = 3$ A; note 1	15	50	100	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 6$ A; $I_B = 0.6$ A; note 1	–	0.75	–	V
f_T	transition frequency	$V_{CB} = 25$ V; $I_E = -3$ A; f = 100 MHz; note 2	–	680	–	MHz
	transition frequency	$V_{CB} = 25$ V; $I_E = -6$ A; f = 100 MHz; note 2	–	750	–	MHz
C_c	collector capacitance	$V_{CB} = 25$ V; $I_E = i_e = 0$; f = 1 MHz	–	155	–	pF
C_{re}	feedback capacitance	$I_C = 100$ mA; $V_{CE} = 25$ V; f = 1 MHz	–	88	–	pF
C_{cs}	collector-stud capacitance		–	3	–	pF

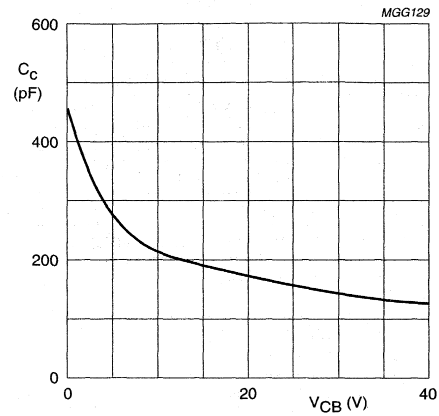
Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0.02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0.01$.



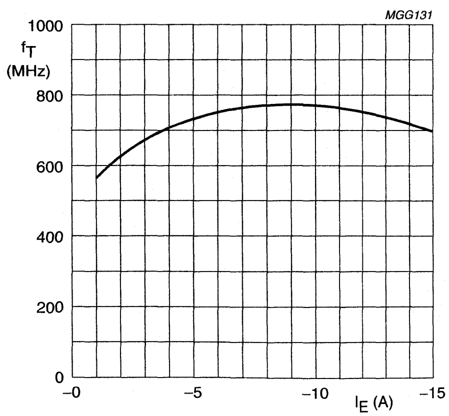
T_j = 25 °C.
(1) V_{CE} = 25 V.
(2) V_{CE} = 5 V.

Fig.5 DC current gain as a function of collector current; typical values.



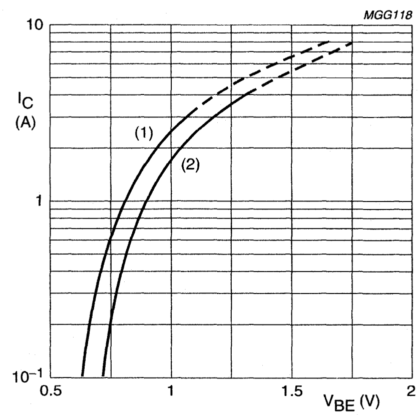
$I_E = i_e = 0$; f = 1 MHz; T_j = 25 °C.

Fig.6 Collector capacitance as a function of collector-base voltage; typical values.



V_{CB} = 25 V; f = 100 MHz; T_j = 25 °C.

Fig.7 Transition frequency as a function of emitter current; typical values.



V_{CE} = 25 V.
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.8 Collector current as a function of base-emitter voltage; typical values.

APPLICATION INFORMATION

RF performance in VHF class-A operation (linear power amplifier)

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_C (A)	T_h (°C)	d_{im}[(1)] (dB)	$P_{o\ sync}$[(1)] (W)	G_P (dB)
CW, class-A	224.25	25	3.2	70	−55	>16.5	>9
				70	−55	typ. 17.5	typ. 9.3
				70	−52	typ. 26.5	typ. 9.3
				25	−55	typ. 23	typ. 9.7

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

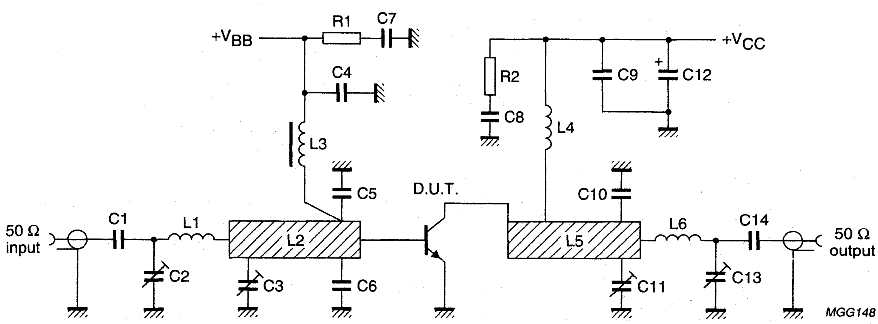


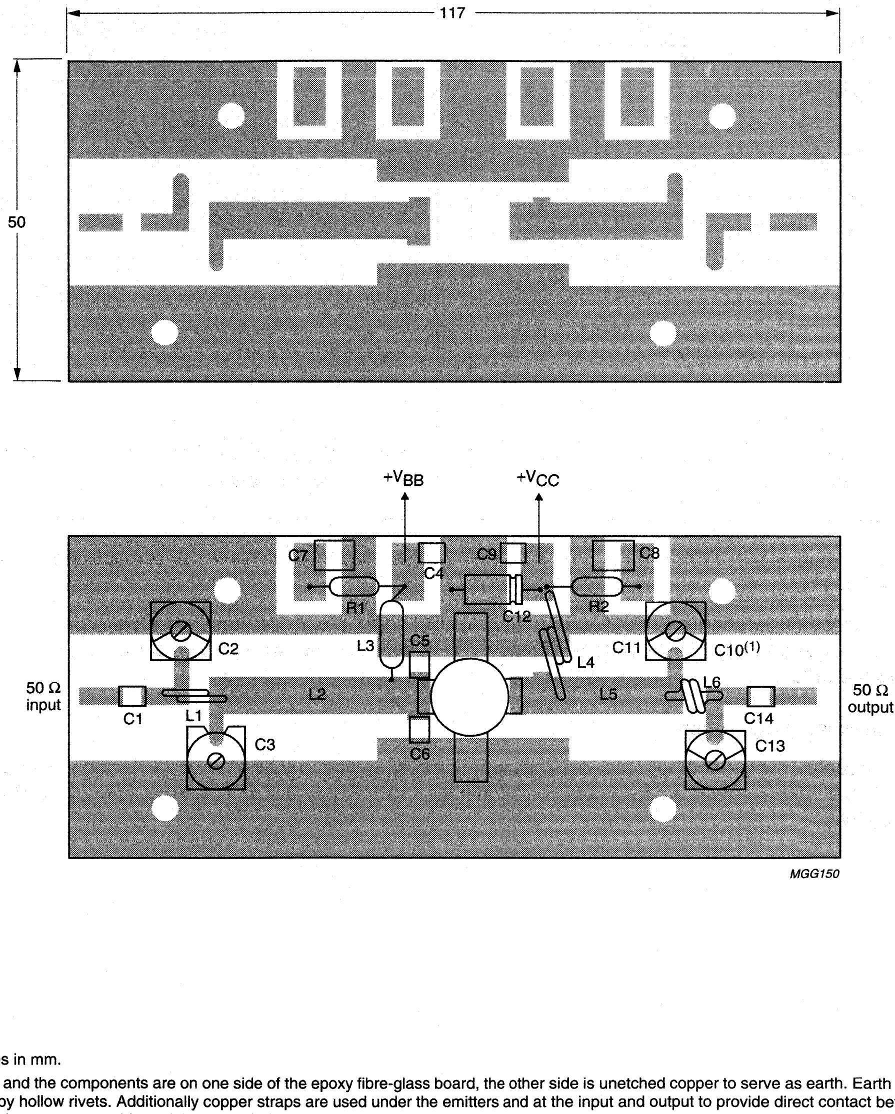
Fig.9 Class-A test circuit at f_{vision} = 224.25 MHz.

List of components used in test circuit (see Figs 9 and 10).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C14	multilayer ceramic chip capacitor; note 1	680 pF, 500 V		
C2, C11, C13	film dielectric trimmer	4 to 40 pF		2222 809 08002
C3	film dielectric trimmer	2 to 18 pF		2222 809 09003
C4, C9	multilayer ceramic chip capacitor	680 pF, 50 V		2222 852 13681
C5, C6	multilayer ceramic chip capacitor; note 1	68 pF, 500 V	placed 2 mm from transistor edge	
C7, C8	multilayer ceramic chip capacitor	470 nF, 50 V		2222 856 48474
C10	multilayer ceramic chip capacitor; note 1	24 pF, 500 V		
C12	solid aluminium electrolytic capacitor	10 μF, 40 V		
L1	1½ turns of closely wound 1.6 mm enamelled Cu wire		int. diameter 4.5 mm leads 2 × 3 mm	
L2	stripline	30 Ω	6 mm × 32.7 mm	
L3	microchoke	1 μH		4322 057 01080
L4	2 turns of 1.1 mm enamelled Cu wire	27 nH	int. diameter 4.5 mm length 2.9 mm leads 2 × 5 mm	
L5	stripline	30 Ω	6 mm × 24 mm	
L6	2 turns of 1.1 mm enamelled Cu wire	19 nH	int. diameter 3.5 mm length 3.5 mm leads 2 × 5 mm	
L2, L5	stripline; note 2			
R1, R2	carbon resistor	10 Ω		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double Cu-clad printed-circuit board, with epoxy fibre-glass dielectric ($\varepsilon_r = 4.5$); thickness $^1/_{16}$".

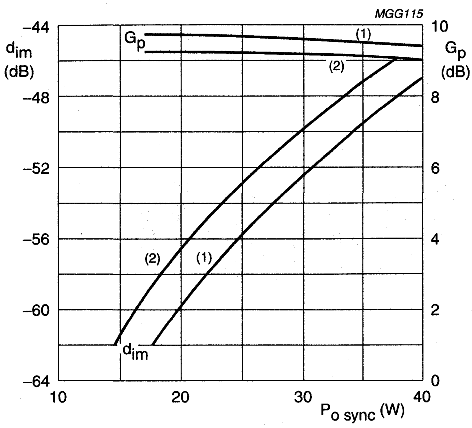


Dimensions in mm.

The circuit and the components are on one side of the epoxy fibre-glass board, the other side is unetched copper to serve as earth. Earth connections are made by hollow rivets. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

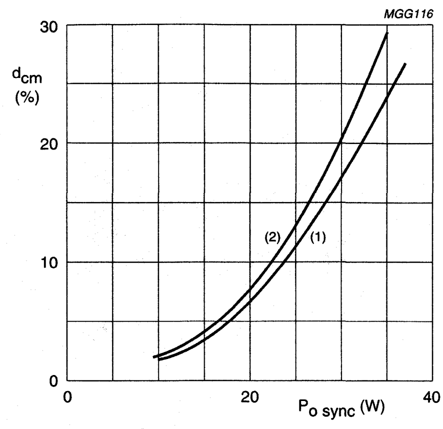
(1) C10 positioned under C11.

Fig.10 Component layout and printed-circuit board for 224.25 MHz class-A test circuit.



V_{CE} = 25 V; I_C = 3.2 A; f_{vision} = 224.25 MHz.
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.11 Intermodulation distortion and power gain as a functions of output power.



V_{CE} = 25 V; I_C = 3.2 A; f_{vision} = 224.25 MHz.
(1) T_h = 25 °C.
(2) T_h = 70 °C.

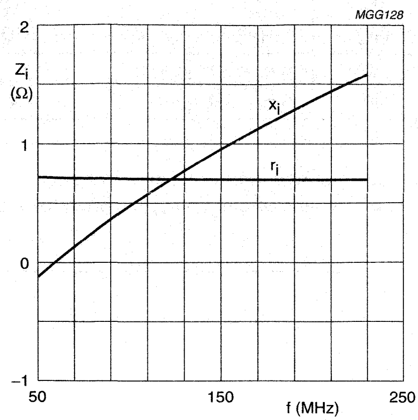
Fig.12 Cross-modulation distortion as a function of output power.

Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level (see Fig.11).

Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level. Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB (see Fig.12).

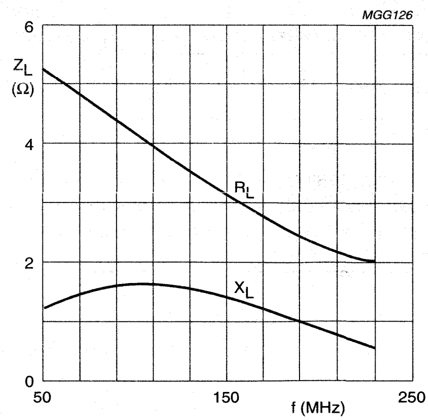
Ruggedness in class-A operation

The BLV33 is capable of withstanding a full load mismatch corresponding to VSWR = 50 : 1 through all phases up to 30 W (RMS) or 40 W (PEP) under the following conditions: V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C; f = 224.25 MHz; $R_{th\ mb\text{-}h}$ = 0.15 K/W.



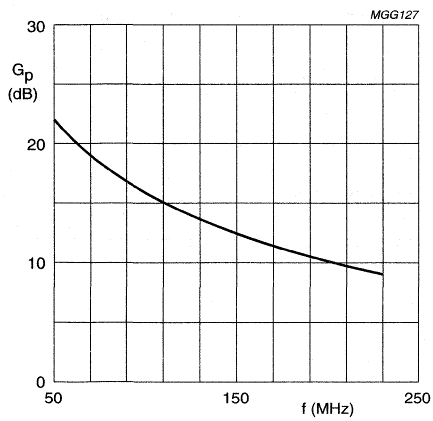
Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.13 Input impedance as a function of frequency (series components); typical values.



Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.14 Load impedance as a function of frequency (series components); typical values.



Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.15 Power gain as a function of frequency; typical values.

RF performance in VHF class-AB operation (C.W)

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_C, $I_{C(ZS)}$ (A)	T_h (°C)	P_L (W)	I_C (A)	η_C (%)	G_P (dB)[1]
CW, class-AB	224.25	28	0.1	70	40	typ. 2.60	typ. 55	typ. 7.5
					90	typ. 4.46	typ. 72	typ. 6.5

Note

1. Gain compression point of 1 dB is at typical 90 W (minimum 80 W). Using a 3rd-order amplitude transfer characteristic, 1 dB compression corresponds with 30 % sync input / 25 % sync output compression in television service (negative modulation, C.C.I.R. system).

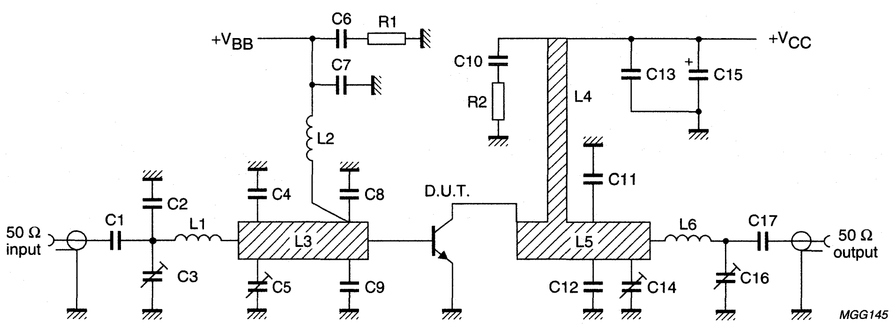


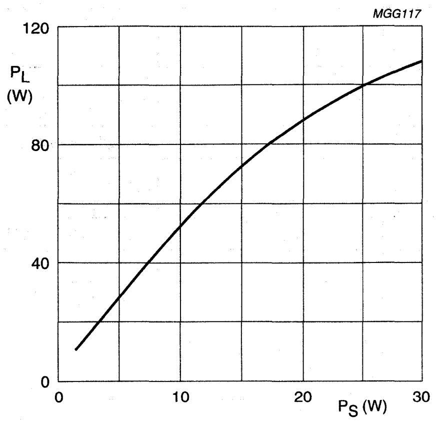
Fig.16 Class-AB test circuit at f_{vision} = 224.25 MHz.

List of components used in test circuit (see Fig.16).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C17	multilayer ceramic chip capacitor; note 1	680 pF, 500 V		
C2	multilayer ceramic chip capacitor; note 1	39 pF, 500 V		
C3, C16	film dielectric trimmer	2 to 18 pF		2222 809 09003
C4	multilayer ceramic chip capacitor; note 1	43 pF, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C10	polyester capacitor	330 nF		
C7, C13	multilayer ceramic chip capacitor	680 pF, 50 V		2222 852 13681
C8, C9	multilayer ceramic chip capacitor; note 1	68 pF, 500 V	placed 2.5 mm from transistor edge	
C11, C12	multilayer ceramic chip capacitor; note 1	27 pF, 500 V	placed 7 mm from transistor edge	
C14	film dielectric trimmer	5 to 60 pF		2222 809 08003
C15	solid aluminium electrolytic capacitor	10 μF, 40 V		
L1	2 turns of 1.6 mm enamelled Cu wire	25 nH	int. diameter 4.3 mm length 3.4 mm leads 2 × 5 mm	
L2	4 turns closely wound 1.1 mm enamelled Cu wire	120 nH	int. diameter 6 mm leads 2 × 5 mm	
L3	stripline; note 2	30 Ω	6 mm × 48.8 mm	
L4	stripline; note 2	48 Ω	3 mm × 27 mm at 3 mm from transistor edge	
L5	stripline; note 2	30 Ω	6 × 42.9 mm	
L6	2 turns of 1.6 mm enamelled Cu wire	24 nH	int. diameter 4 mm length 3.4 mm leads 2 × 5 mm	
R1, R2	carbon resistor	10 Ω		

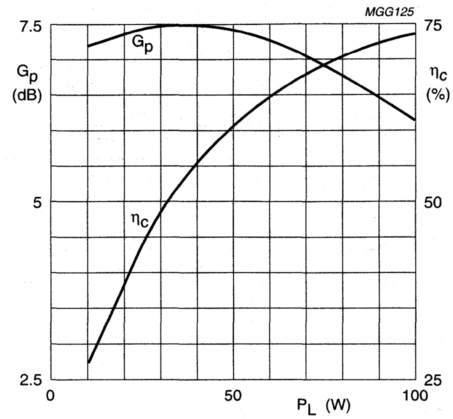
Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double Cu-clad printed-circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5); thickness $^1/_{16}$".



V_{CE} = 28 V; $I_{C(ZS)}$ = 0.1 A; T_h = 70 °C; f_{vision} = 224.25 MHz.

Fig.17 Load power as a function of source power; typical values.

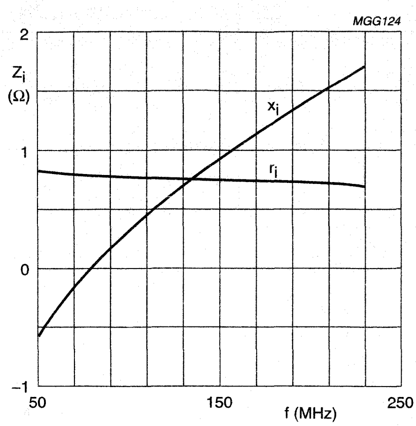


V_{CE} = 28 V; $I_{C(ZS)}$ = 0.1 A; T_h = 70 °C; f_{vision} = 224.25 MHz.

Fig.18 Power gain and efficiency as functions of load power; typical values.

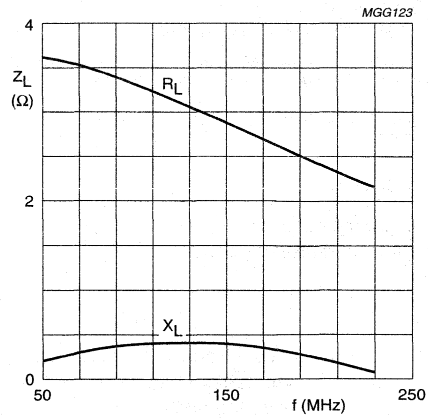
Ruggedness in class-AB operation

The BLV33 is capable of withstanding a full load mismatch corresponding to VSWR ≤ 2 through all phases) up to 60 W (RMS) and 90 W (PEP) under the following conditions: V_{CE} = 28 V; T_h = 70 °C; f = 224.25 MHz; $R_{th\ mb-h}$ = 0.15 K/W.



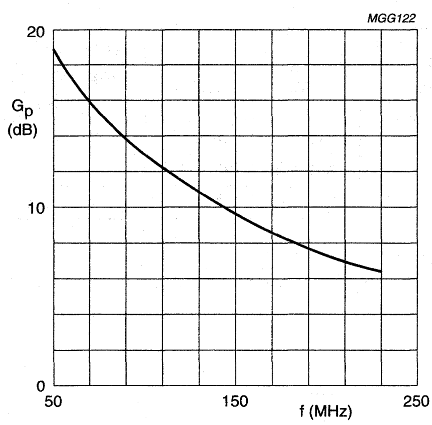
Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.19 Input impedance (series components); typical values.



Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.20 Load impedance (series components); typical values.



Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.21 Power gain as a function of frequency; typical values.

VHF linear power transistor | BLV33F

FEATURES

- Internally matched input for wideband operation and high power gain
- Diffused emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Primarily intended for use in linear VHF amplifiers for television transmitters and transposers.

DESCRIPTION

NPN silicon planar epitaxial transistor encapsulated in a ½" 6 lead SOT119A capstan package with ceramic cap. All leads are isolated from the flange.

PINNING - SOT119A

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	b	base
4	c	collector
5	e	emitter
6	e	emitter

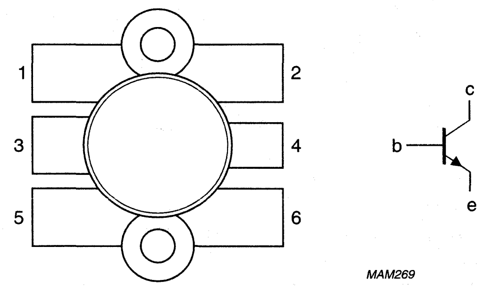


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance in a common emitter push-pull test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_C, $I_{C(ZS)}$ (A)	T_h (°C)	d_{im}(1) (dB)	$P_{o\ sync}$ (1) (W)	G_P (dB)	sync compr.(2) sync in/sync out (%)
CW, class-A	224.25	25	3.2	70	−55	>13	>13.5	
				25	−55	typ. 19	typ. 14.8	
CW, class-AB	224.25	28	0.2	70	−	typ. 85	typ. 10.5	30/25

Notes

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
2. Television service (negative modulation, C.C.I.R. system).

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

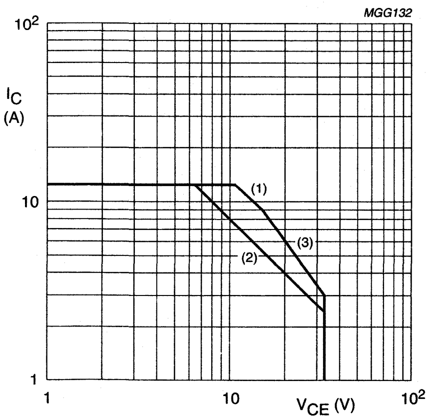
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter voltage	$V_{BE} = 0$	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	33	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current (DC)		–	12.5	A
$I_{C(AV)}$	average collector current		–	12.5	A
I_{CM}	peak collector current	f > 1 MHz	–	20	A
P_{tot}	total power dissipation (DC)	$T_{mb} = 25$ °C	–	133	W
P_{rf}	RF power dissipation	f > 1 MHz; $T_{mb} = 25$ °C	–	162	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

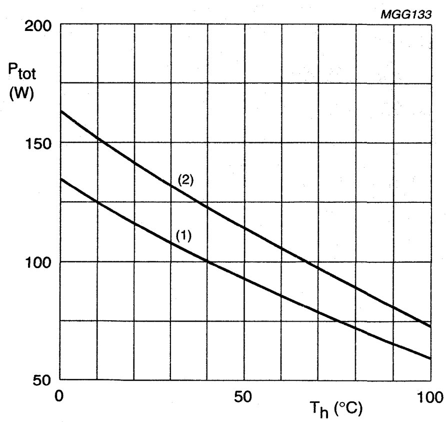
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb(dc)}$	thermal resistance from junction to mounting base (DC dissipation)	$P_{diss} = 80$ W; $T_{mb} = 82$ °C; $T_h = 70$ °C	1.43	K/W
$R_{th\ j\text{-}mb(rf)}$	thermal resistance from junction to mounting base (RF dissipation)	$P_{diss} = 80$ W; $T_{mb} = 82$ °C; $T_h = 70$ °C	1.17	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	$P_{diss} = 80$ W; $T_{mb} = 82$ °C; $T_h = 70$ °C	0.2	K/W



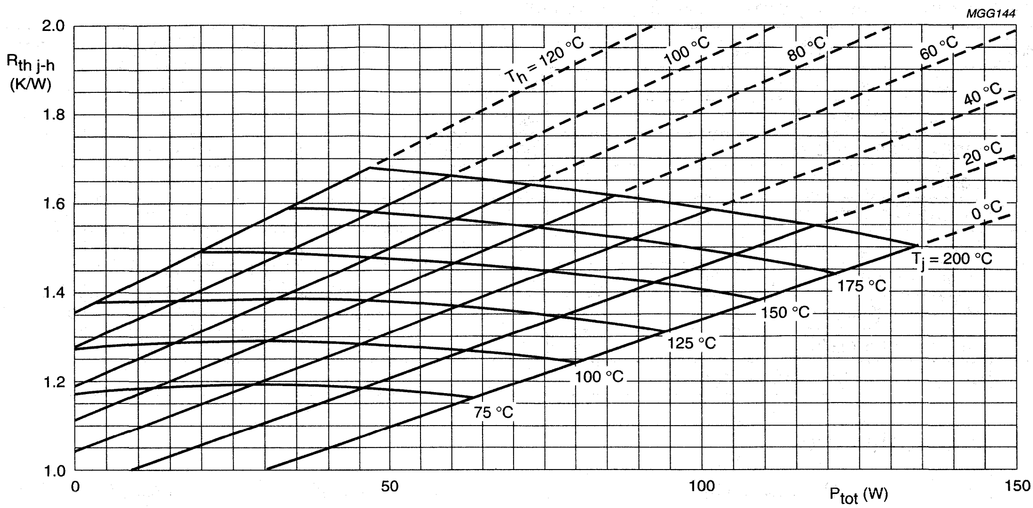
(1) $T_{mb} = 25$ °C.
(2) $T_h = 70$ °C.
(3) Second breakdown limit (independent of temperature).

Fig.2 DC SOAR.



(1) Continuous DC (including RF class-A) operation.
(2) Continuous RF operation.

Fig.3 Power derating curves.



$R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters.

Example

Nominal class-A operation (without RF signal): V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Figure 4 shows:

$R_{th\ j\text{-}h}$ = max. 1.63 K/W

T_j = max. 200 °C.

Typical device:

$R_{th\ j\text{-}h}$ = typ.1.53 K/W

T_j = typ. 192 °C.

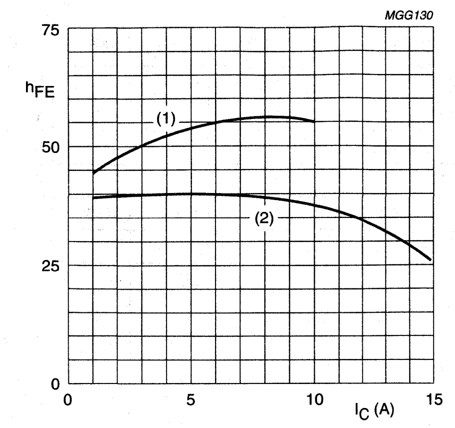
CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	collector-emitter breakdown voltage	V_{BE} = 0; I_C = 25 mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 100 mA	33	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	4	–	–	V
I_{CES}	collector cut-off current	V_{BE} = 0; V_{CE} = 30 V	–	–	1	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 3 A; note 1	15	50	100	
V_{CEsat}	collector-emitter saturation voltage	I_C = 6 A; I_B = 0.6 A; note 1	–	0.75	–	V
f_T	transition frequency	V_{CB} = 25 V; I_E = −3 A; f = 100 MHz; note 2	–	680	–	MHz
		V_{CB} = 25 V; I_E = −6 A; f = 100 MHz; note 2	–	750	–	MHz
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	155	–	pF
C_{re}	feedback capacitance	I_C = 50 mA; V_{CE} = 25 V; f = 1 MHz	–	88	–	pF
C_{cf}	collector-flange capacitance		–	3	–	pF

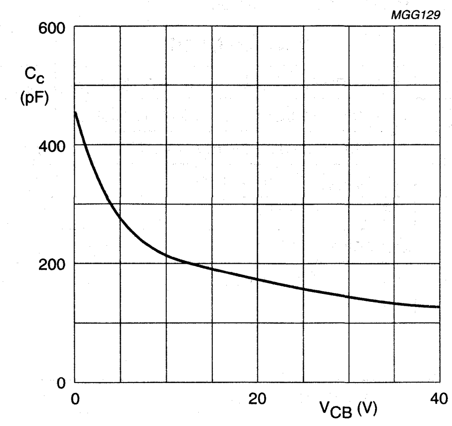
Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0.02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0.01$.



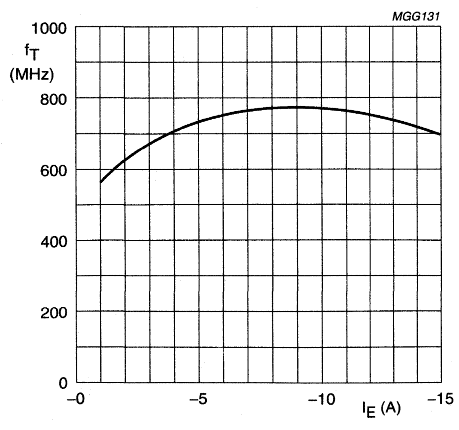
T_j = 25 °C.
(1) V_{CE} = 25 V.
(2) V_{CE} = 5 V.

Fig.5 DC current gain as a function of collector current; typical values.



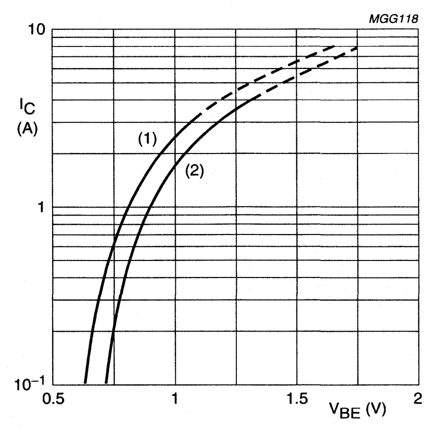
$I_E = i_e = 0$; f = 1 MHz; T_j = 25 °C.

Fig.6 Collector capacitance as a function of collector-base voltage; typical values.



V_{CB} = 25 V; f = 100 MHz; T_j = 25 °C.

Fig.7 Transition frequency as a function of emitter current; typical values.



V_{CE} = 25 V.
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.8 Collector current as a function of base-emitter voltage; typical values.

APPLICATION INFORMATION

RF performance in VHF class-A operation (linear power amplifier)

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_C (A)	T_h (°C)	d_{im}(1) (dB)	$P_{o\ sync}$(1) (W)	G_P (dB)
CW, class-A	224.25	25	3.2	70	−55	>13	>13.5
				70	−55	typ. 14.5	typ. 14.5
				70	−52	typ. 22	typ. 14.5
				25	−55	typ. 19	typ. 14.8

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

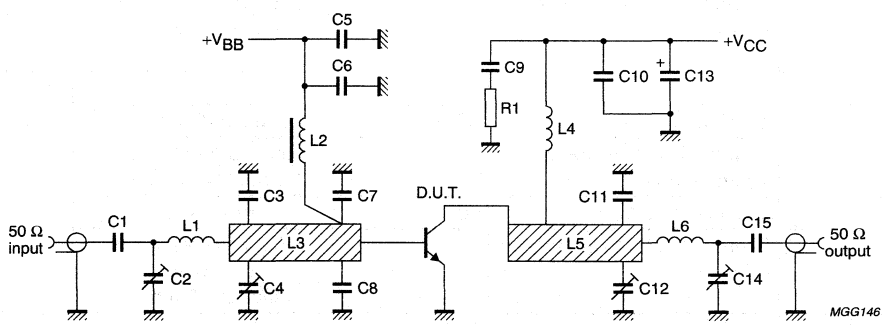


Fig.9 Class-A test circuit at f_{vision} = 224.25 MHz.

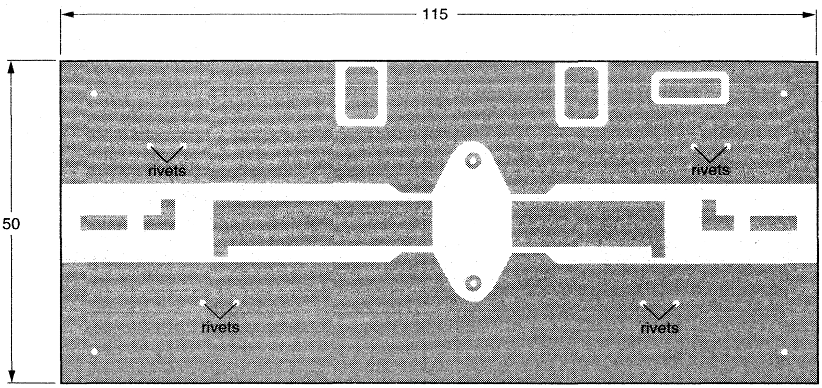
List of components used in test circuit (see Figs 9 and 10).

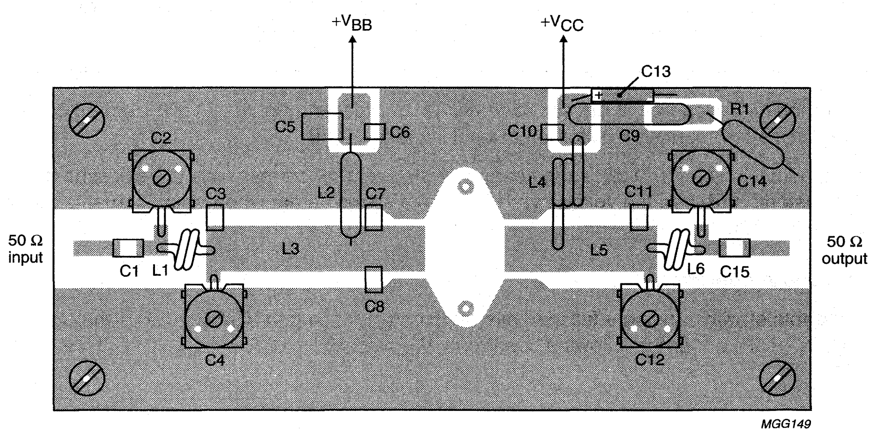
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C15	multilayer ceramic chip capacitor; note 1	560 pF, 500 V		
C2, C4, C12, C14	film dielectric trimmer	4 to 40 pF		2222 809 08002
C3	multilayer ceramic chip capacitor; note 1	10 pF, 500 V		
C5	multilayer ceramic chip capacitor	470 nF, 50 V		2222 856 48474
C6, C10	multilayer ceramic chip capacitor	680 pF, 50 V		2222 852 13681
C7, C8	multilayer ceramic chip capacitor; note 1	47 pF, 500 V	placed 8 mm from transistor edge	
C9	polyester capacitor	330 nF		
C11	multilayer ceramic chip capacitor; note 1	68 pF, 500 V		
C13	solid tantalum capacitor	6.8 μF, 35 V		
L1	2 turns of 1.6 mm enamelled Cu wire		int. diameter 5 mm length 5 mm leads 2 × 3 mm	
L2	microchoke	1 μH		4322 057 01080
L3	stripline; note 2	30 Ω	6 mm × 32.7 mm	
L4	2 turns of closely wound 1 mm enamelled Cu wire		int. diameter 5 mm leads 2 × 10 mm	
L5	stripline; note 2	30 Ω	6 mm × 24 mm	
L6	2 turns of 1.6 mm enamelled Cu wire		int. diameter 4 mm length 4.5 mm leads 2 × 3 mm	
R1	carbon resistor	10 Ω		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double Cu-clad printed-circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5); thickness $^1\!/_{16}$".

VHF linear power transistor BLV33F

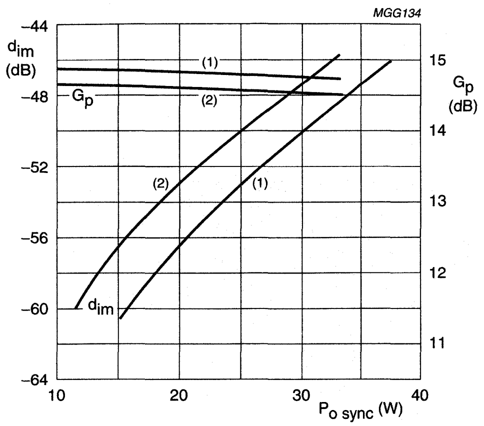




Dimensions in mm.

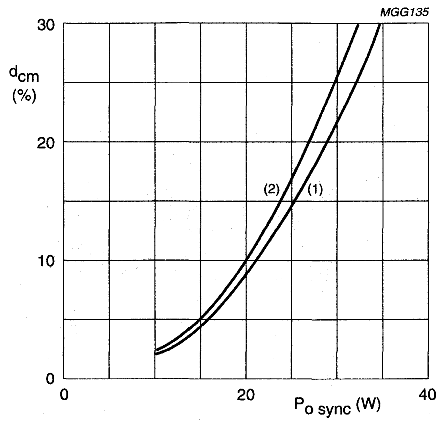
The circuit and the components are on one side of the epoxy fibre-glass board, the other side is unetched copper to serve as earth. Earth connections are made by hollow rivets. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

Fig.10 Component layout and printed-circuit board for 224.25 MHz class-A test circuit.



V_{CE} = 25 V; I_C = 3.2 A; f_{vision} = 224.25 MHz.
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.11 Intermodulation distortion and power gain as a functions of output power.



V_{CE} = 25 V; I_C = 3.2 A; f_{vision} = 224.25 MHz.
(1) T_h = 25 °C.
(2) T_h = 70 °C.

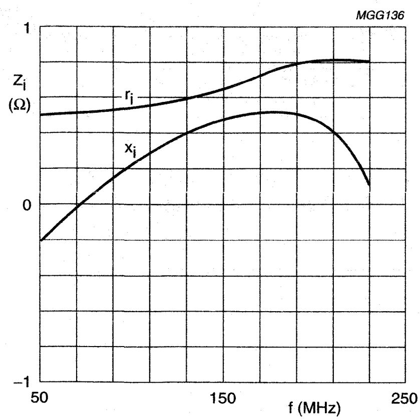
Fig.12 Cross-modulation distortion as a function of output power.

Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level (see Fig.11). Intermodulation distortion of input signal ≤−70 dB.

Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level. Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB (see Fig.12).

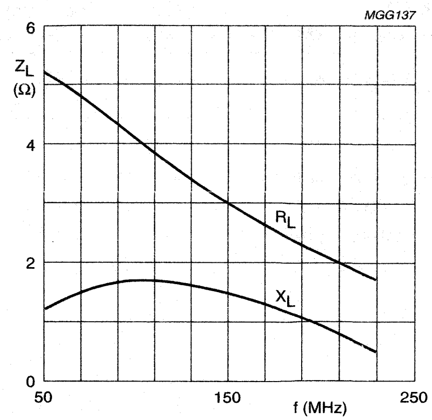
Ruggedness in class-A operation

The BLV33F is capable of withstanding a full load mismatch corresponding to VSWR = 50 : 1 through all phases up to 30 W (RMS) or 40 W (PEP) under the following conditions: V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C; f = 224.25 MHz; $R_{th\ mb\text{-}h}$ = 0.2 K/W.



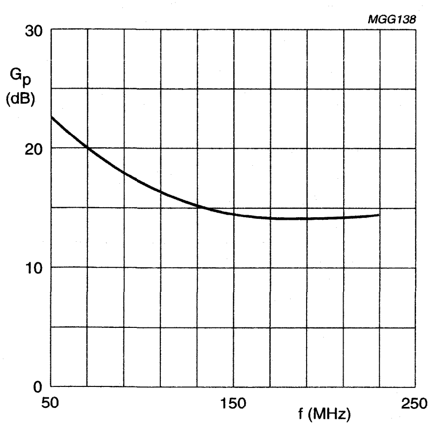
Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.13 Input impedance as a function of frequency (series components); typical values.



Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.14 Load impedance as a function of frequency (series components); typical values.



Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.15 Power gain as a function of frequency; typical values.

RF performance in VHF class-AB operation (C.W.).

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_C, $I_{C(ZS)}$ (A)	T_h (°C)	P_L (W)	I_C (A)	η_C (%)	G_P (dB)(1)
CW, class-AB	224.25	28	0.2	70	40	typ. 2.75	typ. 52	typ. 11.5
					85	typ. 4.25	typ. 71	typ. 10.5

Note

1. Gain compression point of 1 dB is at typical 85 W (minimum 75 W). Using a 3rd-order amplitude transfer characteristic, 1 dB compression corresponds with 30 % sync input / 25 % sync output compression in television service (negative modulation, C.C.I.R. system).

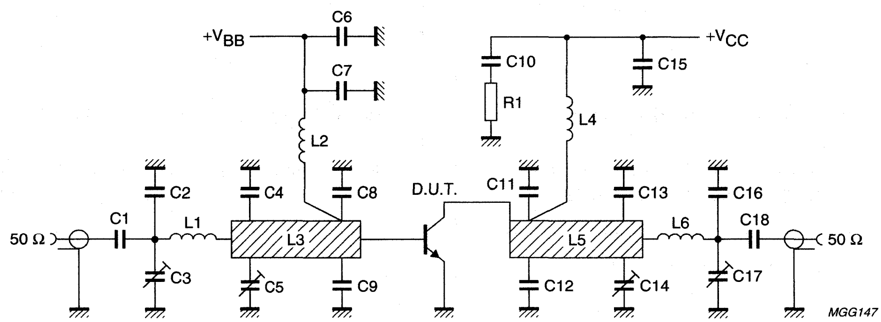


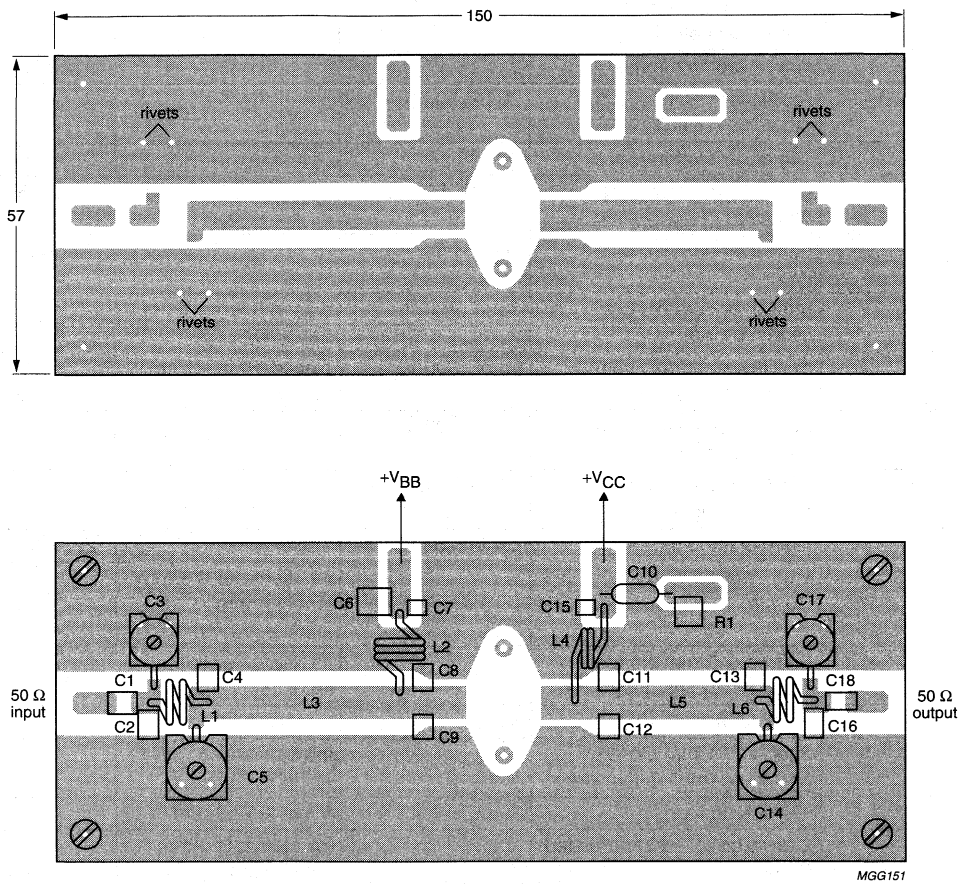
Fig.16 Class-AB test circuit at f_{vision} = 224.25 MHz.

List of components used in test circuit (see Figs 16 and 17).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C18	multilayer ceramic chip capacitor; note 1	620 pF, 100 V		
C2	multilayer ceramic chip capacitor; note 1	27 pF, 500 V		
C3	film dielectric trimmer	2 to 18 pF		2222 809 09003
C4	multilayer ceramic chip capacitor; note 1	30 pF, 500 V		
C5, C14	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C10	multilayer ceramic chip capacitor	470 nF, 50 V		2222 856 48474
C7, C15	multilayer ceramic chip capacitor	680 pF, 50 V		2222 852 13681
C8, C9	multilayer ceramic chip capacitor; note 1	68 pF, 500 V	placed 6.4 mm from transistor edge	
C11, C12	multilayer ceramic chip capacitor; note 1	43 pF, 500 V	placed 10 mm from transistor edge	
C13	multilayer ceramic chip capacitor; note 1	39 pF, 500 V		
C16	multilayer ceramic chip capacitor; note 1	3.3 pF, 500 V		
C17	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
L1	2 turns of 1.6 mm enamelled Cu wire		int. diameter 4.5 mm length 4 mm leads 2 × 4 mm	
L2	3 turns of 1 mm closely wound enamelled Cu wire		int. diameter 5 mm leads 2 × 7 mm	
L3	stripline; note 2	30 Ω	6 mm × 47.8 mm	
L4	2 turns of 1 mm closely wound enamelled Cu wire		int. diameter 5 mm leads 2 × 8 mm	
L5	stripline; note 2	30 Ω	6 mm × 42.9 mm	
L6	2 turns of 1.6 mm enamelled Cu wire		int. diameter 4 mm length 4 mm leads 2 × 3 mm	
R1	carbon resistor	10 Ω		

Notes

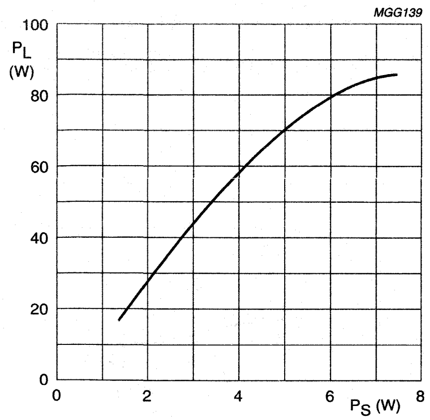
1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double Cu-clad printed-circuit board, with epoxy fibre-glass dielectric ($\varepsilon_r = 4.5$); thickness $1/16$".



Dimensions in mm.

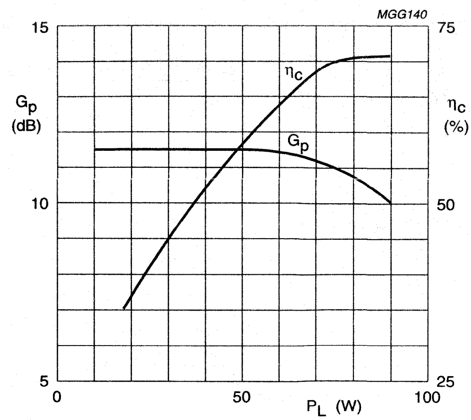
The circuit and the components are on one side of the epoxy fibre-glass board, the other side is unetched copper to serve as earth. Earth connections are made by hollow rivets. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

Fig.17 Component layout and printed-circuit board for 224.25 MHz class-AB test circuit.



V_{CE} = 28 V; $I_{C(ZS)}$ = 0.2 A; T_h = 70 °C; f_{vision} = 224.25 MHz.

Fig.18 Load power as a function of source power; typical values.



V_{CE} = 28 V; $I_{C(ZS)}$ = 0.2 A; T_h = 70 °C; f_{vision} = 224.25 MHz.

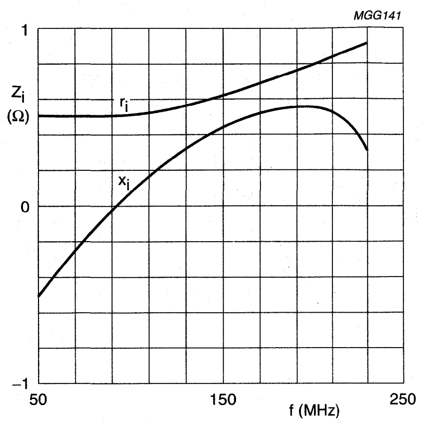
Fig.19 Power gain and efficiency as functions of load power; typical values.

Ruggedness in class-AB operation

The BLV33F is capable of withstanding a full load mismatch corresponding to VSWR ≤2 through all phases) up to 60 W (RMS) and 85 W (PEP) under the following conditions:V_{CE} = 28 V; T_h = 70 °C; f = 224.25 MHz; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

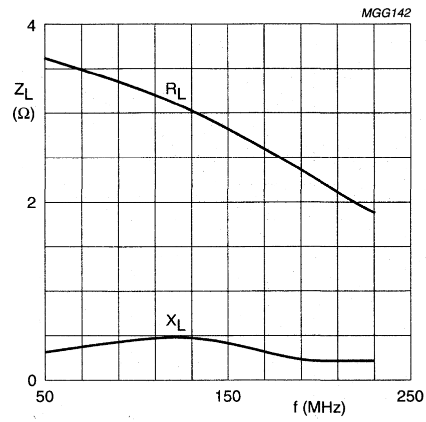
VHF linear power transistor

BLV33F



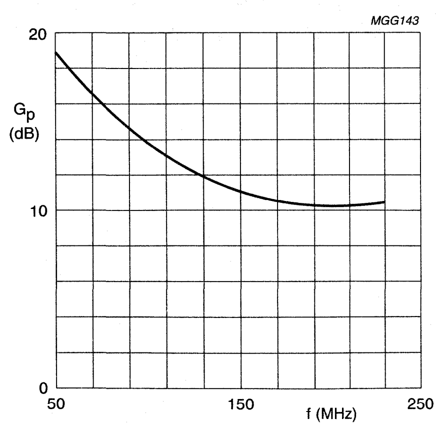
Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.20 Input impedance as a function of frequency (series components); typical values.



Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.21 Load impedance as a function of frequency (series components); typical values.



Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.22 Power gain as a function of frequency; typical values.

UHF linear push-pull power transistor BLV57

FEATURES

- internally matched input for wideband operation and high power gain
- internal midpoint (r.f. ground) reduces negative feedback and improves power gain
- increased input and output impedances (compared with single-ended transistors) simplify wideband matching
- length of the external emitter leads is not critical
- diffused emitter ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability.

DESCRIPTION

Two n-p-n silicon planar epitaxial transistor sections in one package to be used as push-pull amplifier, primarily intended for use in linear u.h.f. television transmitters and transposers.

The package is an 8-lead flange type with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT161A

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	c2	collector 2
4	b2	base 2
5	c1	collector 1
6	b1	base 1
7	e	emitter
8	e	emitter

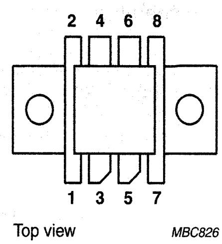


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

R.F. performance in linear amplifier

MODE OF OPERATION	f_{vision} MHz	V_{CE} V	$I_{C1} = I_{C2}$ A	$I_{C(ZS)}$ A	T_h °C	d_{im} (1) dB	$P_{o\ sync}$ (1) W	P_L W	G_p dB
class-A	860	25	0,85	–	70 25	–60 –55	〉 6 typ. 12	–	〉 8,0 typ. 9,0
class-AB	860	25	1,25	2 × 0,1	25	–	–	typ. 38(2)	typ. 6,5(2)

Notes

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak sync level.
2. Power gain compression is 1 dB.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

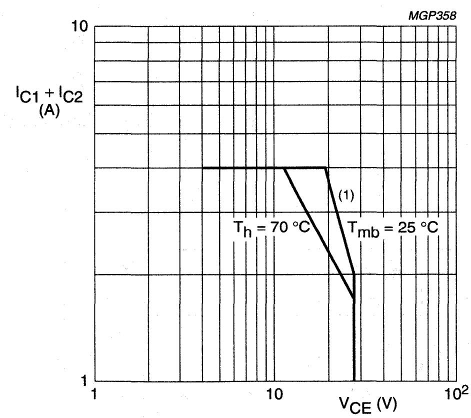
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage				
(peak value); $V_{BE} = 0$	V_{CESM}	max.	50	V
open base	V_{CEO}	max.	27	V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5	V
Collector current per transistor section				
d.c. or average	I_C; $I_{C(AV)}$	max.	2	A
(peak value); f 〉 1 MHz	I_{CM}	max.	4	A
Total power dissipation at $T_{mb} = 25$ °C(1)	P_{tot}	max.	77	W(1)
R.F. power dissipation (f 〉 1 MHz); $T_{mb} = 25$ °C(1)	P_{rf}	max.	93	W(1)
Storage temperature	T_{stg}	−65 to + 150		°C
Operating junction temperature	T_j	max.	200	°C

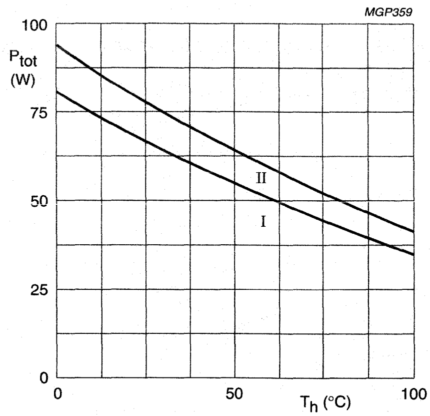
Note

1. Dissipation of either transistor section should not exceed half rated dissipation.



(1) Second breakdown limit (independent of temperature).

Fig.2 D.C. SOAR.(1)



I Continuous d.c. (including r.f. class-A) operation
II Continuous r.f. operation
Dissipation of either transistor section should not exceed half rated dissipation.

Fig.3 Power derating curves vs. temperature.(1)

THERMAL RESISTANCE

(dissipation = 42 W; T_{mb} = 80,5 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j-mb(dc)}$	=	2,43	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j-mb(rf)}$	=	1,91	K/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0,25	K/W

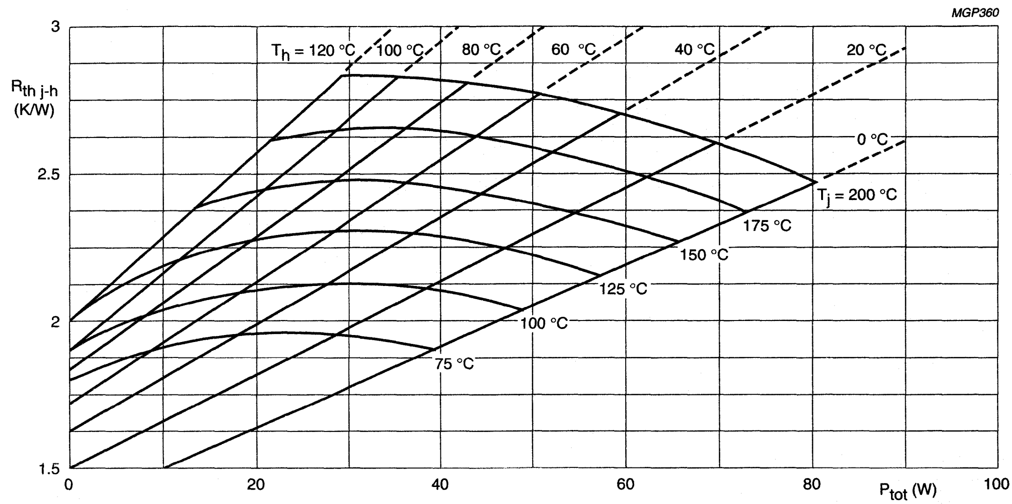


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb\text{-}h}$ = 0,25 K/W.)

Example

Nominal class-A push-pull operation (without r.f. signal): V_{CE} = 25 V; $I_{C1} = I_{C2}$ = 0,85 A; T_h = 70 °C.

Fig.4 shows:	$R_{th\ j\text{-}h}$	max.	2,68	K/W
	T_j	max.	184	°C
Typical device:	$R_{th\ j\text{-}h}$	typ.	2,28	K/W
	T_j	typ.	167	°C

CHARACTERISTICS apply to either transistor section unless otherwise specified

$T_j = 25°C$

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 10$ mA	$V_{(BR)CES}$	⟩	50	V
open base; $I_C = 25$ mA	$V_{(BR)CEO}$	⟩	27	V
Emitter-base breakdown voltage				
open collector; $I_E = 5$ mA	$V_{(BR)EBO}$	⟩	3,5	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 27$ V	I_{CES}	⟨	10	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	⟩	2	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	⟩	2	mJ
D.C. current gain(1)				
$I_C = 0{,}85$ A; $V_{CE} = 25$ V	h_{FE}	⟩ typ.	15 40	
D.C. current gain ratio of transistor sections				
$I_C = 0{,}85$ A; $V_{CE} = 25$ V			0,67 to 1,5	
Collector-emitter saturation voltage(1)				
$I_C = 1{,}7$ A; $I_B = 0{,}17$ A	V_{CEsat}	typ.	0,75	V
Transition frequency at f = 100 MHz(2)				
$-I_E = 0{,}85$ A; $V_{CB} = 25$ V	f_T	typ.	2,5	GHz
$-I_E = 1{,}7$ A; $V_{CB} = 25$ V	f_T	typ.	2,5	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 25$ V	C_c	typ. ⟨	24 30	pF pF
Feedback capacitance at f = 1 MHz				
$I_C = 50$ mA; $V_{CE} = 25$ V	C_{re}	typ.	15	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300\ \mu s$; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50\ \mu s$; $\delta \leq 0{,}01$.

The graphs apply to either transistor section.

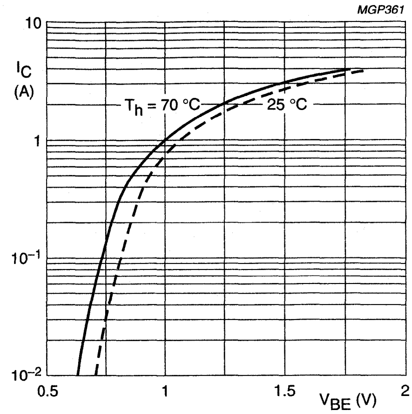


Fig.5 Typical values; V_{CE} = 25 V.

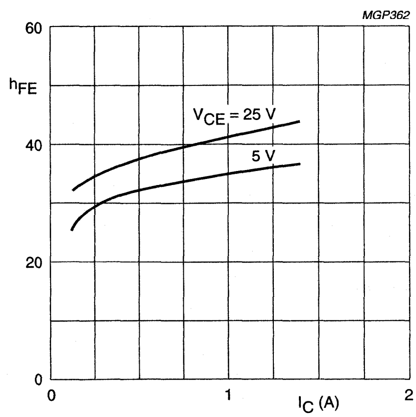


Fig.6 Typical values; T_j = 25 °C.

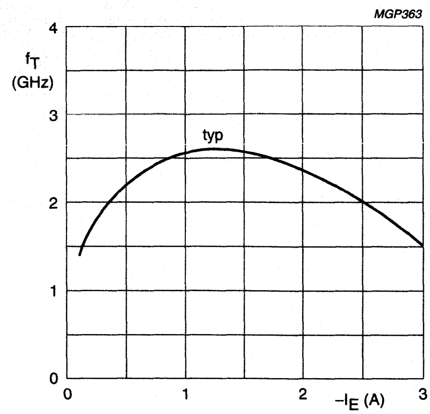


Fig.7 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C.

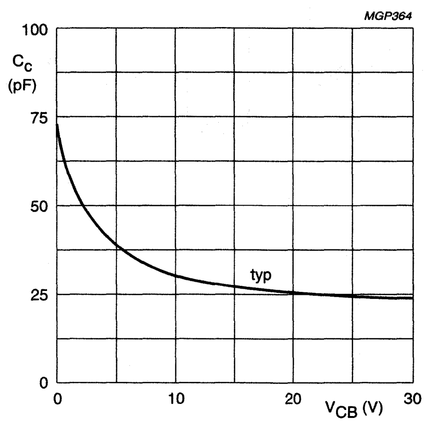


Fig.8 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in u.h.f. class-A operation (linear push-pull power amplifier)

f_{vision} (MHz)	V_{CE} (V)	$I_{C1} = I_{C2}$ (A)	T_h (°C)	d_{im} (1) (dB)	$P_{o\ sync}$ (1) (W)	G_p (dB)
860	25	0,85	70	−60	> 6	> 8,0
			70	−60	typ. 7,5	typ. 8,5
			70	−55	typ. 10	typ. 8,5
			25	−55	typ. 12	typ. 9,0

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

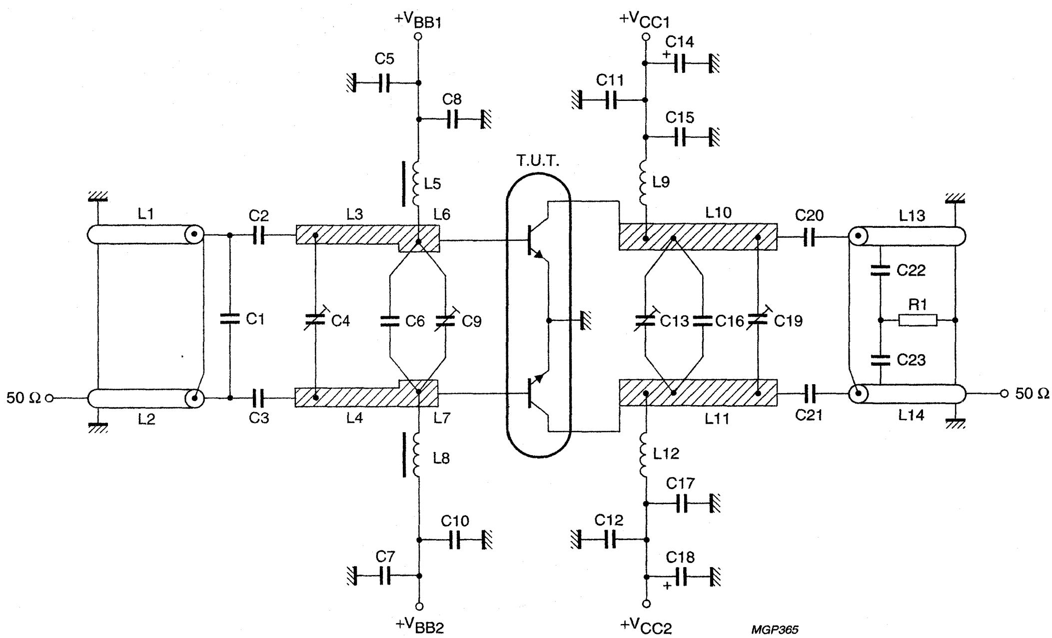


Fig.9 Class-A test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C6 = C16 = 4,7 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C2 = C3 = C20 = C21 = 33 pF multilayer ceramic chip capacitor (cat. no. 2222 851 13339)

C4 = C9 = C13 = C19 = 1,2 to 3,5 pF film dielectric trimmer (cat.no. 2222 809 05001)

C5 = C7 = C15 = C17 = 100 nF multilayer ceramic chip capacitor (cat. no. 2222 852 59104)

C8 = C10 = C11 = C12 = 220 pF multilayer ceramic chip capacitor (cat. no. 2222 852 13221)

C14 = C18 = 6,8 μF/40 V solid aluminium electrolytic capacitor

C22 = C23 = 1 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C9 and C13 are placed 8,0 and 14,0 mm from transistor edge, respectively.

L1 = L2 = L13 = L14 = 50 Ω semi-rigid cable; outer diameter 2,2 mm; length 29,0 mm. These cables are soldered on 75 Ω striplines (1,1 mm × 28,0 mm). The centre conductors of the cables L1 and L13 are not connected.

L3 = L4 = 52 Ω stripline (2,0 mm × 16,5 mm)

L5 = L8 = 470 nH microchoke

L6 = L7 = 39 Ω stripline (3,1 mm × 8,0 mm)

L9 = L12 = 1 turn Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 × 3,5 mm

L10 = L11 = 39 Ω stripline (3,1 mm × 34,0 mm)

L3, L4, L6, L7, L10 and L11 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,74); thickness 1/32".

R1 = 10 Ω carbon resistor

Note

1. ATC means American Technical Ceramics.

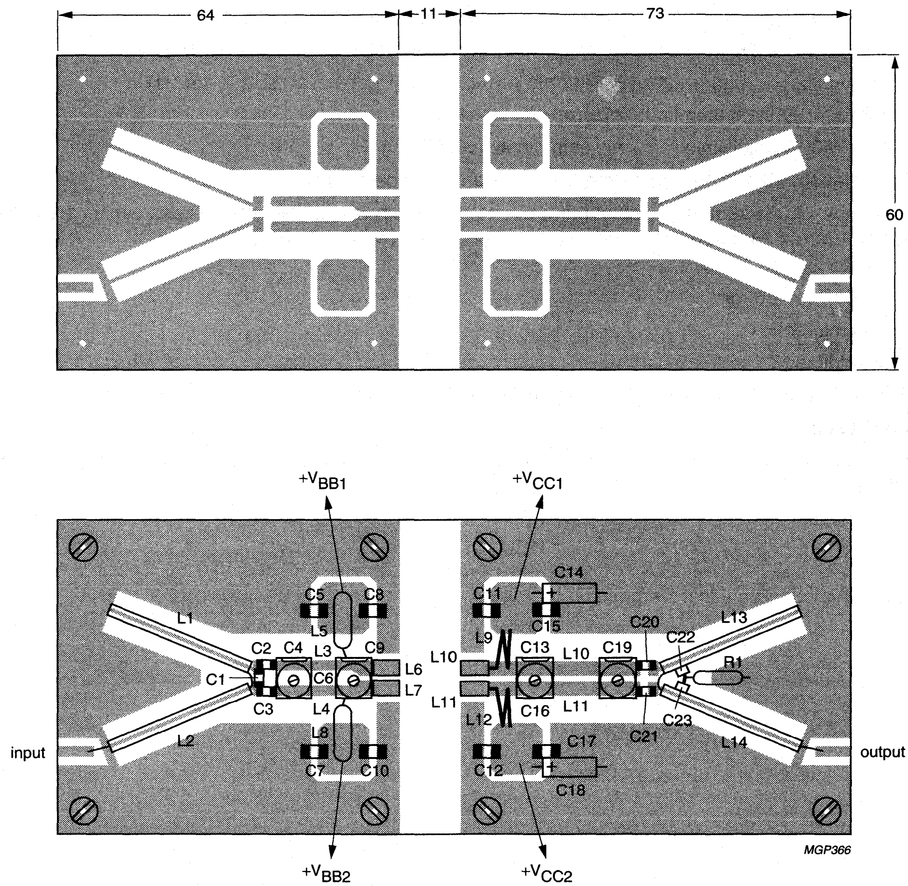


Fig.10 Component layout and printed-circuit board for 860 MHz class-A test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by means of bolts. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

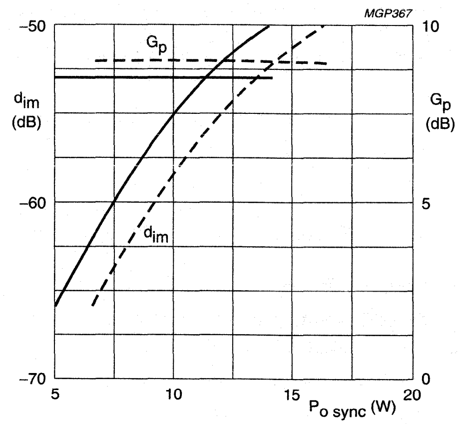


Fig.11 Intermodulation distortion (d_{im})(1) and power gain as a function of output power.

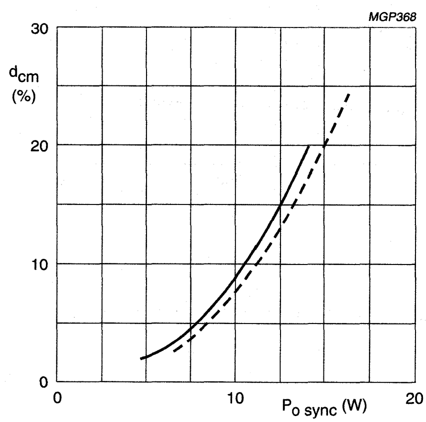


Fig.12 Cross-modulation distortion (d_{cm})(2) as a function of output power.

Conditions for Figs 11and 12:

Typical values; V_{CE} = 25 V; I_C = 2 × 0,85 A; - - - T_h = 25 °C; —— T_h = 70 °C; f_{vision} = 860 MHz.

Ruggedness in push-pull class-A operation

The BLV57 is capable of withstanding full load mismatch (VSWR = 50 through all phases) under the following conditions:

V_{CE} = 25 V; I_C = 2 × 0,85 A; T_h = 70 °C; $P_{o\ sync}$(1) ≤ 12,5 W; f = 860 MHz; $R_{th\ mb\text{-}h}$ = 0,25 K/W.

At any other composition of the output signal: P_L (r.m.s. value) ≤ 5 W.

Notes

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
   Intermodulation distortion of input signal ≤ −70 dB.
2. Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level. Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB.

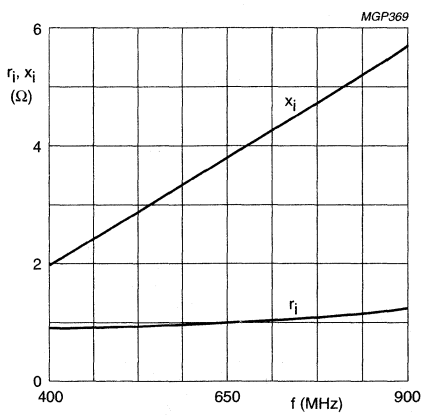


Fig.13 Input impedance (series components).

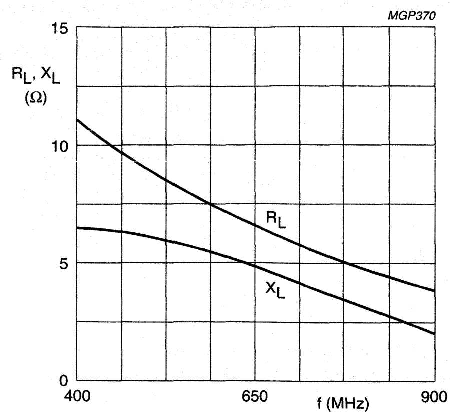


Fig.14 Load impedance (series components).

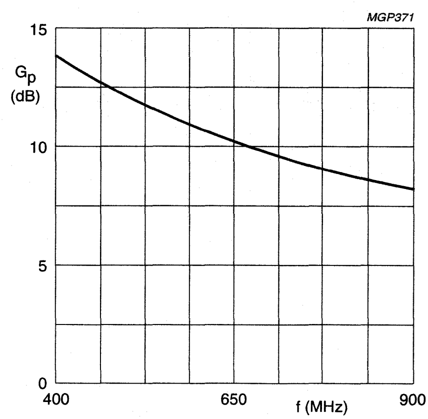


Fig.15

Conditions for Figs 13, 14 and 15:

The graphs apply to either transistor section assuming class-A push-pull operation.
Typical values; V_{CE} = 25 V; I_C = 0,85 A; T_h = 70 °C.

APPLICATION INFORMATION

R.F. performance in u.h.f. class-AB operation (c.w.)

f_{vision} (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (A)	T_h (°C)	P_L (W)	$I_{C1} = I_{C2}$ (A)	η (%)	G_p[1] (dB)
860	25	2 × 0,1	25	12,5			typ. 7,5
				38	typ. 1,25	typ. 60	typ. 6,5
860	25	2 × 0,1	70	12,5			typ. 7,0
				30	typ. 1,10	typ. 55	typ. 6,0

Note

1. Typical values are based on 1 dB gain compression. Using a 3rd order amplitude transfer characteristic, 1 dB compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

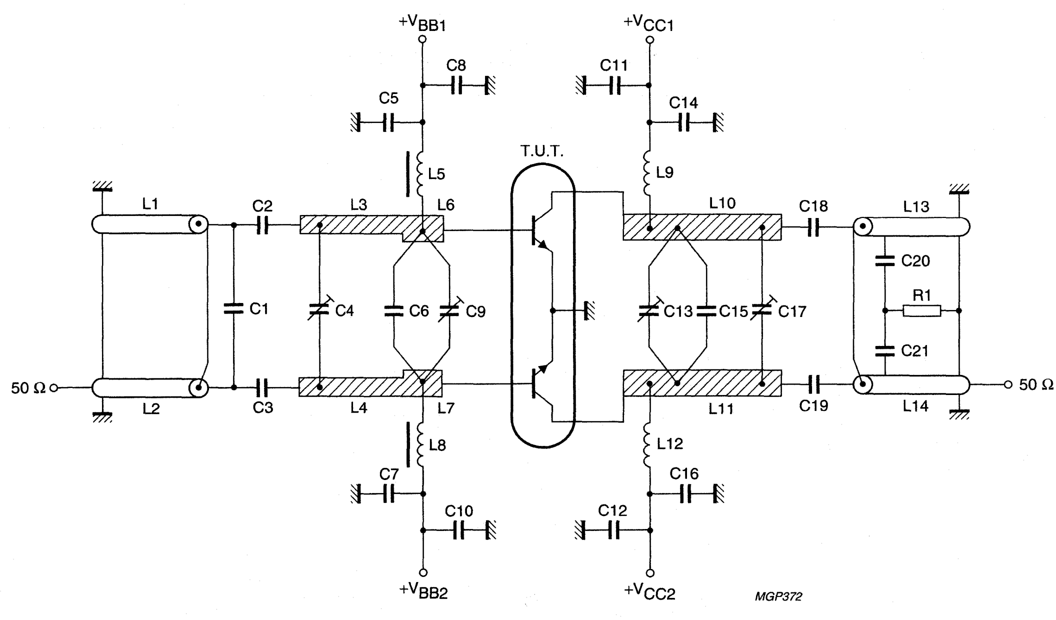


Fig.16 Class-AB test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C6 = C15 = 4,7 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C2 = C3 = C18 = C19 = 33 pF multilayer ceramic chip capacitor (cat. no. 2222 851 13339)

C4 = C9 = C13 = C17 = 1,2 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)

C5 = C7 = C14 = C16 = 100 nF multilayer ceramic chip capacitor (cat. no. 2222 852 59104)

C8 = C10 = C11 = C12 = 220 pF multilayer ceramic chip capacitor (cat. no. 2222 852 13221)

C20 = C21 = 1 pF (500 V) multilayer ceramic chip capacitor (ATC[1])

C9 and C13 are placed 8,0 and 14,0 mm from transistor edge, respectively.

L1 = L2 = L13 = L14 = 50 Ω semi-rigid cable; outer diameter 2,2 mm; length 29,0 mm. These cables are soldered on 75 Ω striplines (1,1 mm × 28,0 mm). The centre conductors of the cables L1 and L13 are not connected.

L3 = L4 = 52 Ω stripline (2,0 mm × 16,5 mm)

L5 = L8 = 470 nH microchoke

L6 = L7 = 39 Ω stripline (3,1 mm × 8,0 mm)

L9 = L12 = 1 turn Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 × 3,5 mm

L10 = L11 = 39 Ω stripline (3,1 mm × 34,0 mm)

L3, L4, L6, L7, L10 and L11 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,74); thickness 1/32"

R1 = 10 Ω carbon resistor.

Note

1. ATC means American Technical Ceramics.

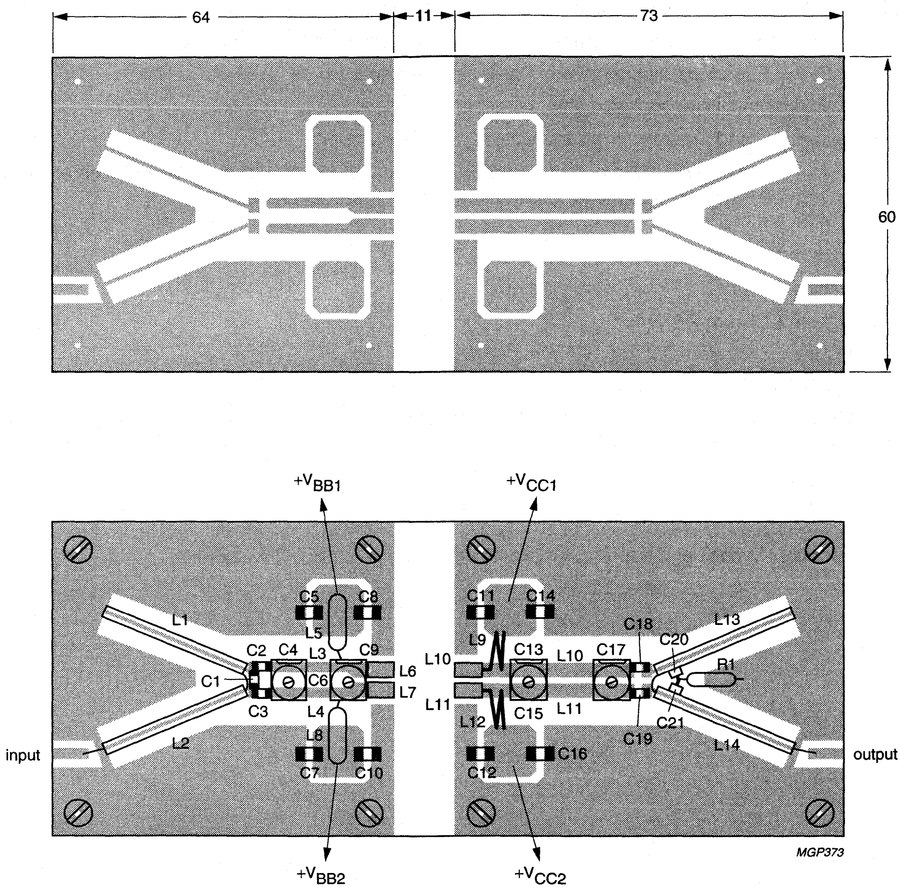


Fig.17 Component layout and printed-circuit board for 860 MHz class-AB test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by means of bolts. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

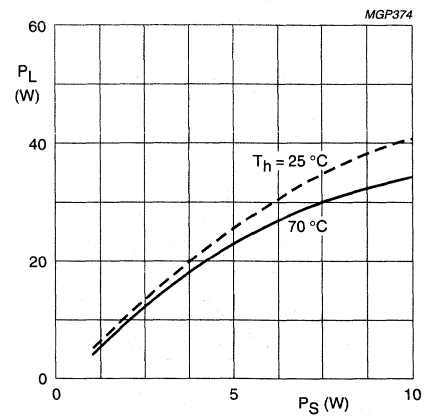


Fig.18 Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 2 × 0,1 A; f_{vision} = 860 MHz.

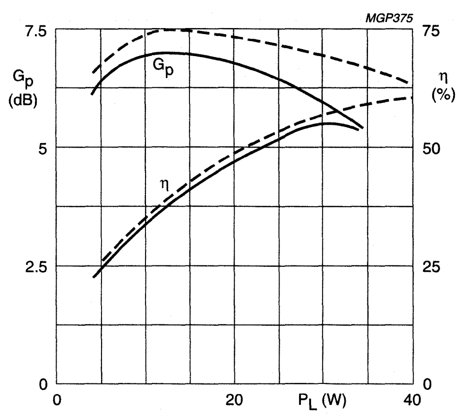


Fig.19 Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 2 × 0,1 A; – – – T_h = 25 °C; ——— T_h = 70°C; f_{vision} = 860 MHz.

Ruggedness in class-AB operation

The BLV57 is capable of withstanding a load mismatch (VSWR ≤ 2 through all phases) up to 30 W (r.m.s. value) or (VSWR ≤ 50 through all phases) up to 19 W under the following conditions:
V_{CE} = 25 V; T_h = 70 °C; f = 860 MHz; $R_{th\ mb\text{-}h}$ = 0,25 K/W.

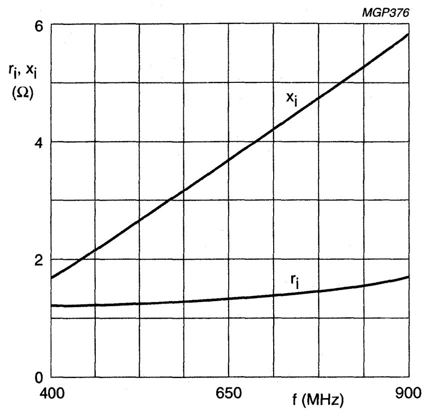


Fig.20 Input impedance (series components).

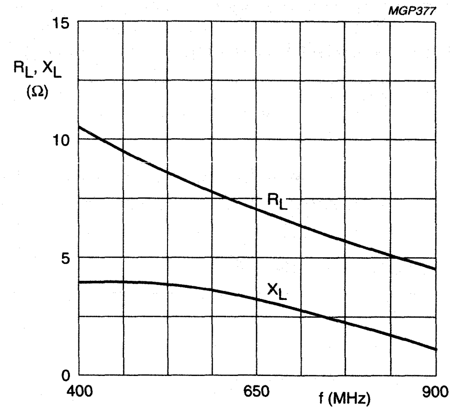


Fig.21 Load impedance (series components).

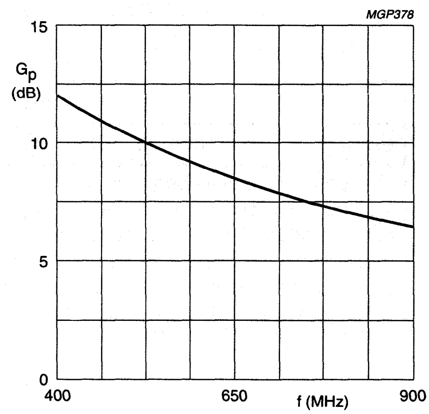


Fig.22

Conditions for Figs 20; 21 and 22:

The graphs apply to either transistor section assuming class-AB push-pull operation.
Typical values; V_{CE} = 25 V; $I_{C(ZS)}$ = 0,1 A; P_L = 17,5 W (P.E.P); T_h = 70 °C.

UHF linear push-pull power transistor | BLV58

FEATURES

- High power gain
- Double stage internal input matching for high input impedance
- Diffused emitter-ballasting resistors enhances ruggedness
- Gold metallization for high reliability.

DESCRIPTION

The BLV58 is a common emitter epitaxial npn silicon planar transistor designed for high linearity class-A operation in UHF (bands 4 and 5) TV transmitters and transposers.

The device is incorporated in a push-pull SOT289 flange envelope with a ceramic cap, which is utilized with the emitters connected to the flange.

PINNING - SOT289

PIN	DESCRIPTION
1	collector 1
2	collector 2
3	base 1
4	base 2
5	emitter

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB) (note 1)
c.w. class-A	860	25	2×1.6	25	>10	< −45

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB); zero dB corresponds to peak sync level.

PIN CONFIGURATION

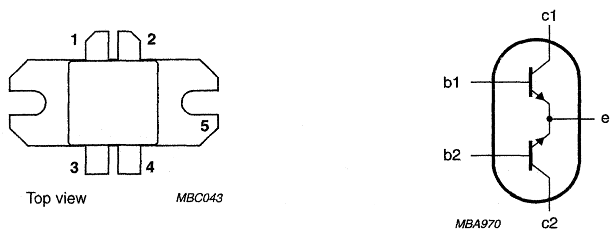


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

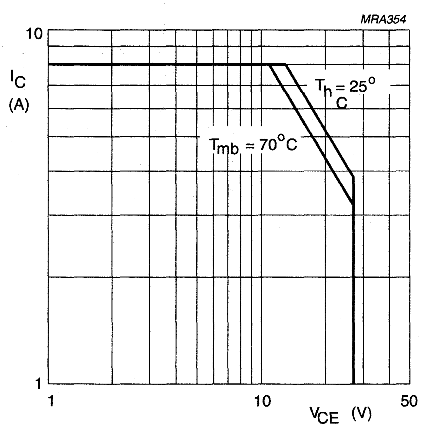
LIMITING VALUES (per transistor section unless otherwise specified)

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3.5	V
I_C, $I_{C(AV)}$	collector current	DC or average value	–	4	A
I_{CM}	collector current	peak value; f > 1 MHz	–	8	A
P_{tot}	total power dissipation	DC operation; T_{mb} = 70 °C (note 1)	–	87	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction operating temperature		–	200	°C

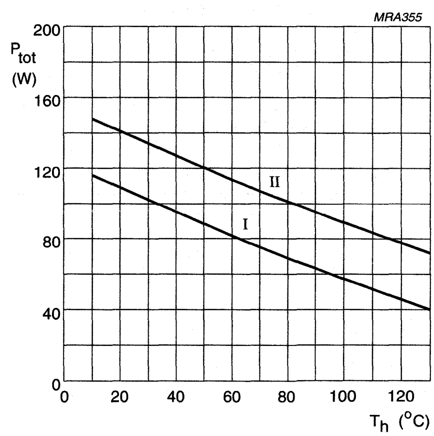
Note

1. Total device, both sections equally loaded.



Total device, both sections equally loaded.

Fig.2 DC SOAR.



(I) Continuous DC operation.
(II) Short time operation during mismatch.
Total device, both sections equally loaded.

Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb(DC)}$	from junction to mounting base	P_{dis} = 87 W; T_{mb} = 70 °C (note 1)	1.5	K/W
$R_{th\ mb\text{-}h}$	from mounting base to heatsink	note 1	0.2	K/W

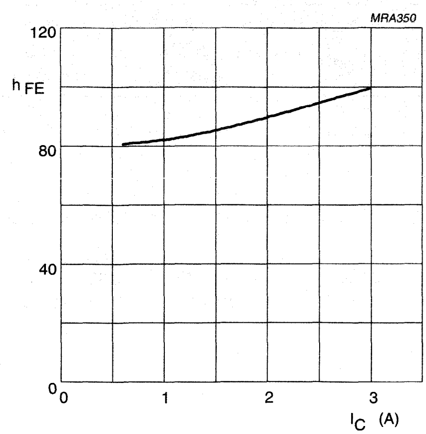
Note

1. Total device, both sections equally loaded.

CHARACTERISTICS

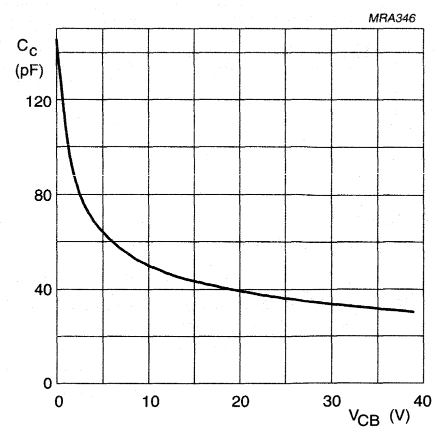
Values apply to either transistor section; T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 20 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 50 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	3.5	–	–	V
I_{CES}	collector-emitter leakage current	V_{BE} = 0; V_{CE} = 27 V	–	–	10	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 1.6 A	30	–	–	
C_c	collector capacitance	V_{CB} = 25 V; $I_E = I_e$ = 0; f = 1 MHz	–	36	45	pF



V_{CE} = 25 V.

Fig.4 DC current gain as a function of collector current, typical values.



$I_E = i_e = 0$; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage, typical values.

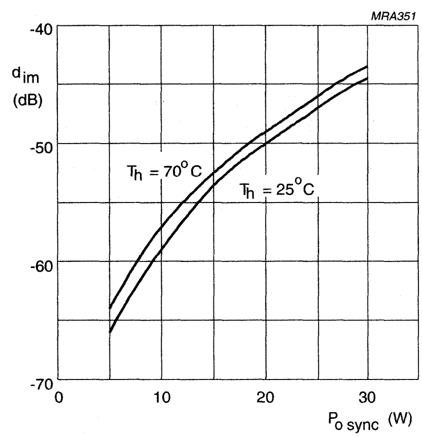
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull test circuit; $R_{th\ mb-h}$ = 0.2 K/W.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_P (dB)	d_{im} (dB) (note 1)	d_{cm} (%) (note 2)
c.w. class-A	860	25	2 × 1.6	25	> 10 typ. 11.5	< −45 typ. −47	< 20

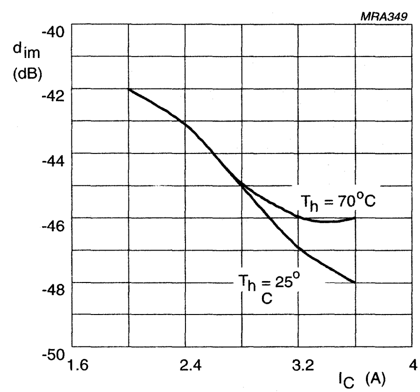
Notes

1. Three-tone test method: vision carrier −8 dB (860 MHz), sound carrier −7 dB (865.5 MHz), sideband signal −16 dB (861 MHz); zero dB corresponds to peak sync level.
2. Two-tone test method: vision carrier 0 dB (860 MHz), sound carrier −7 dB (865.5 MHz); zero dB corresponds to peak sync level. Cross-modulation distortion (d_{cm}) is the voltage variation (%) of the sound carrier when the vision carrier is switched from 0 dB to −20 dB.



Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (−8 dB, −16 dB, −7 dB); I_{CQ} = 2 × 1.6 A.

Fig.6 Intermodulation distortion as a function of output power.



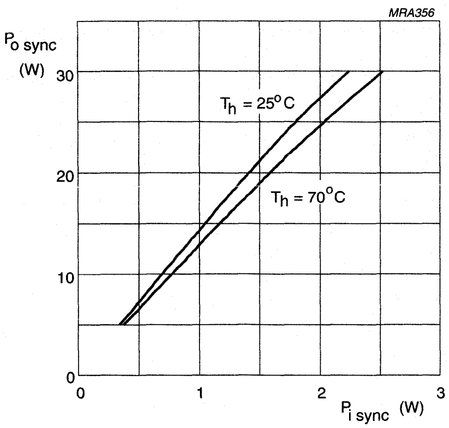
Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (−8 dB, −16 dB, −7 dB); $P_{o\ sync}$ = 25 W.

Fig.7 Intermodulation distortion as a function of collector current.

Ruggedness in Class-A operation

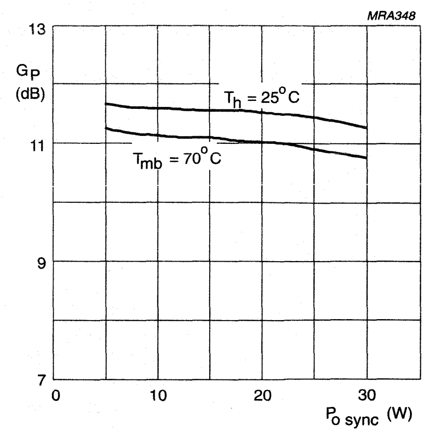
The BLV58 is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{CE} = 25 V, f = 860 MHz, T_h = 25 °C, $R_{th\ mb-h}$ = 0.2 K/W, I_{CQ} = 2 × 1.6 A, and rated output power.



Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (−8 dB, −16 dB, −7 dB); I_{CQ} = 2 × 1.6 A.

Fig.8 Output power as a function of input power.



Class-A operation; V_{CE} = 25 V; f = 860 MHz; 3-tone test (−8 dB, −16 dB, −7 dB); I_{CQ} = 2 × 1.6 A.

Fig.9 Gain as a function of output power, typical values.

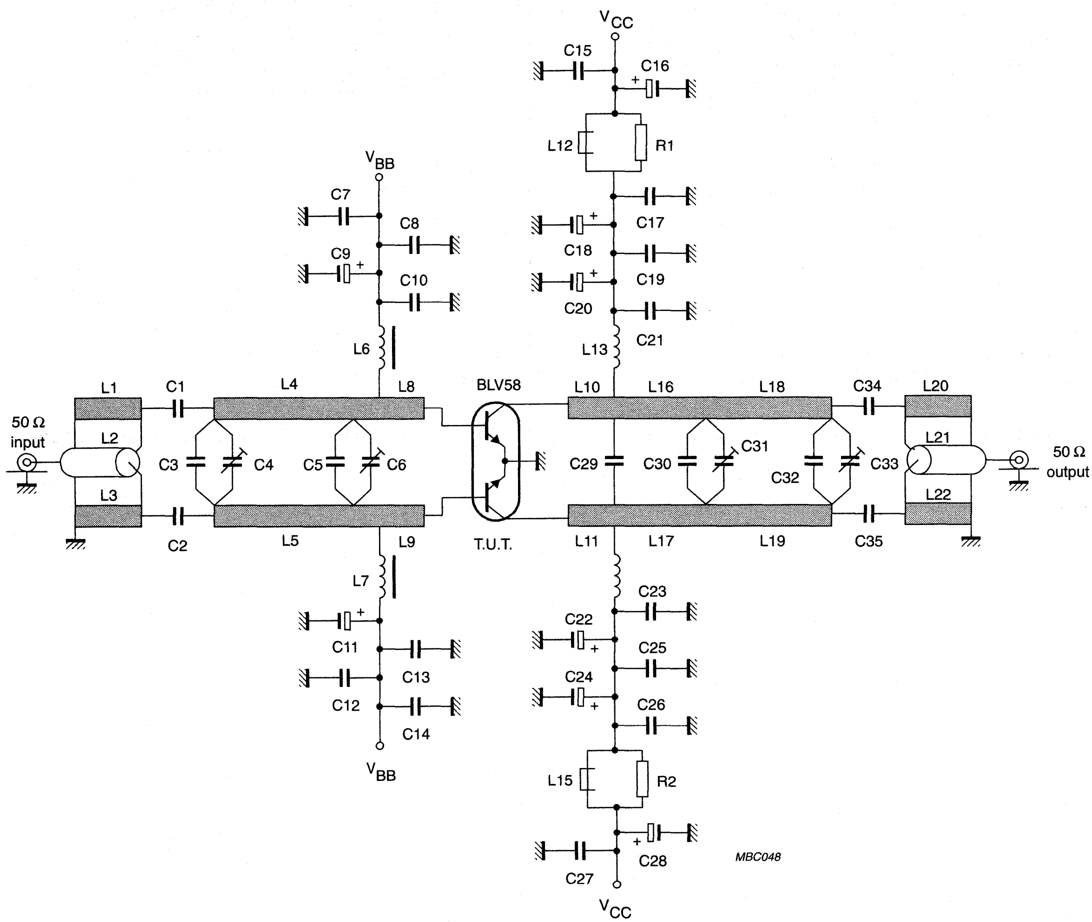


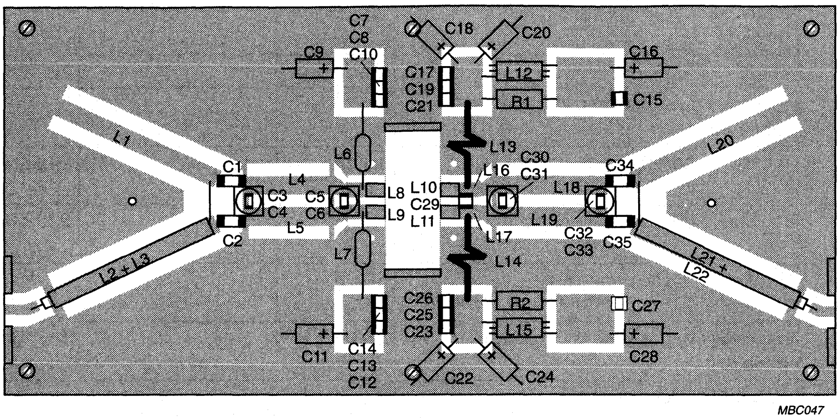
Fig.10 Class-A test circuit at f = 860 MHz.

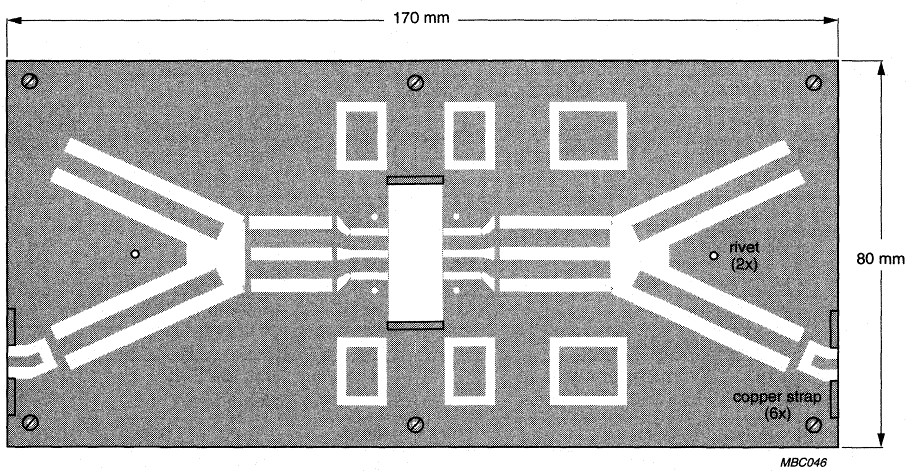
List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C34, C35	multilayer ceramic chip capacitor (note 1)	15 pF		
C3	multilayer ceramic chip capacitor (note 1)	3.9 pF		
C4, C6	film dielectric trimmer	5.5 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 1)	7.5 pF		
C7, C12, C17, C26	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C8, C14, C19, C25	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9, C11, C16, C20, C22, C28	63 V electrolytic capacitor	10 μF		
C10, C13, C15, C21, C23, C27	multilayer ceramic chip capacitor (note 1)	330 pF		
C18, C24	63 V electrolytic capacitor	1 μF		
C29	multilayer ceramic chip capacitor (note 1)	12 pF		
C30	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C31, C33	film dielectric trimmer	3.5 pF		2222 809 05001
C32	multilayer ceramic chip capacitor (note 1)	2.7 pF		
L1, L3, L20, L22	stripline (note 2)	35 Ω	39 mm × 4 mm	
L2, L21	semi-rigid cable (note 3)	50 Ω	ext. dia. 3.6 mm; length 39 mm	
L4, L5	stripline (note 2)	38 Ω	19 mm × 3.5 mm	
L6, L7	RF choke	470 nH		
L8, L9	stripline (note 2)	38 Ω	7.5 mm × 3.5 mm	
L10, L11	stripline (note 2)	38 Ω	4.5 mm × 3.5 mm	
L12, L15	grade 3B RF choke			4312 020 36642
L13, L14	1 turn 1.5 mm copper wire	14 nH	int. dia 7 mm; leads 2 × 6 mm	
L16, L17	stripline (note 2)	38 Ω	7 mm × 3.5 mm	
L18, L19	stripline (note 2)	38 Ω	18 mm × 3.5 mm	
R1, R2	1 W metal film resistor	10 Ω		

Notes

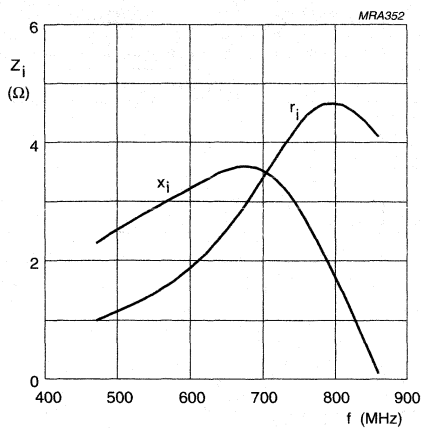
1. American Technical Ceramics type 100B or capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE microfibre-glass dielectric ($\varepsilon_r = 2.2$), thickness $1/32$ inch, thickness of copper sheet 2 × 35 μm.
3. Cables L2 and L21 are soldered to striplines L1 and L20, respectively.





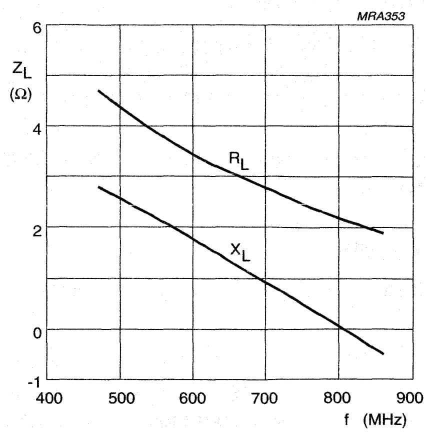
The components are mounted on one side of a copper clad PTFE microfibre-glass board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by hollow rivets and copper straps.

Fig.11 Component layout for 860 MHz class-A test circuit.



Class-A operation; V_{CE} = 25 V;
I_{CQ} = 1.6 A (per section); P_L = 25 W (total device);
T_h = 25 °C.

Fig.12 Input impedance per section (series components) as a function of frequency, typical values.



Class-A operation; V_{CE} = 25 V;
I_{CQ} = 1.6 A (per section); P_L = 25 W (total device);
T_h = 25 °C.

Fig.13 Load impedance per section (series components) as a function of frequency, typical values.

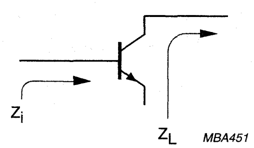
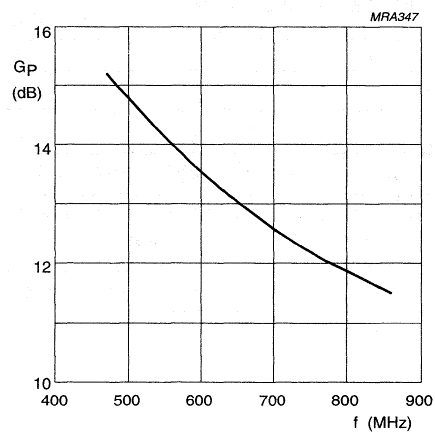


Fig.14 Definition of transistor impedance.



Class-A operation; V_{CE} = 25 V;
I_{CQ} = 1.6 A (per section); P_L = 25 W (total device);
T_h = 25 °C.

Fig.15 Power gain as a function of frequency, typical values.

UHF linear power transistor | BLV59

FEATURES

- Internal input matching to achieve an optimum wideband capability and high power gain
- Emitter-ballasting resistors for lower junction temperatures
- Titanium-platinum-gold metallization ensures long life and excellent reliability.

APPLICATIONS

- UHF linear amplifiers in television transmitters.

DESCRIPTION

NPN silicon planar epitaxial power transistor encapsulated in a 6-lead SOT171A flange package with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT171A

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	b	base
4	c	collector
5	e	emitter
6	e	emitter

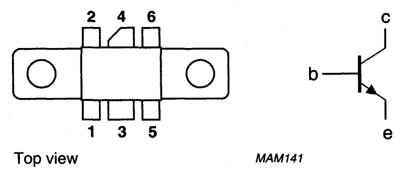


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter class-AB circuit.

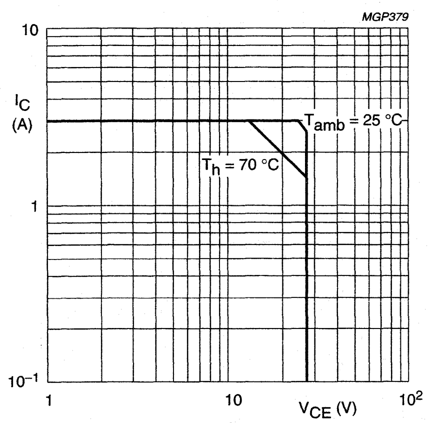
MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	860	25	30	>7	>50

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

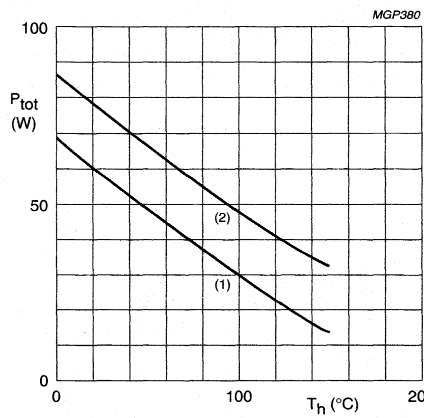
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3.5	V
I_C	collector current (DC)		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
I_{CM}	peak collector current	f > 1 MHz	–	9	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; f > 1 MHz	–	70	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C



$R_{th\ mb\text{-}h}$ = 0.4 K/W.

Fig.2 DC SOAR.



(1) Continuous operation (f > 1 MHz).
(2) Short-time operation during mismatch (f > 1 MHz).

Fig.3 Power/temperature derating curves.

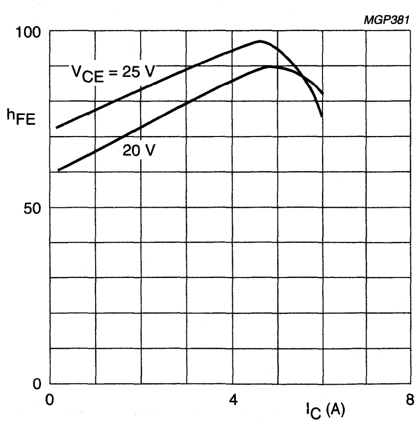
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C, P_{tot} = 50 W	2.3	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

CHARACTERISTICS

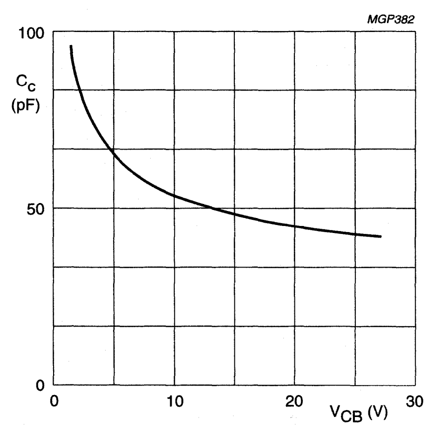
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 50 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 100 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	3.5	–	–	V
I_{CES}	collector leakage current	V_{CE} = 27 V; V_{BE} = 0	–	–	10	mA
$E_{(SBR)}$	second breakdown energy	L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	4	–	–	mJ
h_{FE}	DC current gain	V_{CE} = 24 V; I_C = 2 A	15	–	–	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	44	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_C = 0; f = 1 MHz	–	30	–	pF
C_{cf}	collector-flange capacitance		–	2	–	pF



T_j = 25 °C.

Fig.4 DC current gain as a function of collector current; typical values.



I_E = i_e = 0; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage; typical values

APPLICATION INFORMATION

RF performance up to T_h = 25 °C in a common emitter class-AB circuit; $R_{th\ mb-h}$ = 0.4 K/W.

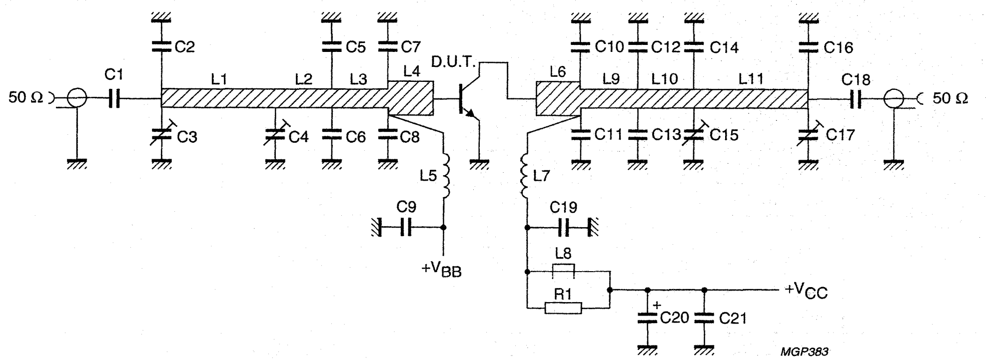
MODE OF OPERATION	f (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (mA)	G_p (dB)	P_L (W)	η_C (%)	ΔG_p (dB)(1)
CW, class-AB	860	25	60	>7 typ. 8.5	30	>50 typ. 55	<1 typ. 0.2

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

Ruggedness in class-AB operation

The BLV59 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases at rated load power under the following conditions: V_{CE} = 25 V; f = 860 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA.



Temperature compensated bias (R_i < 0.1 Ω).

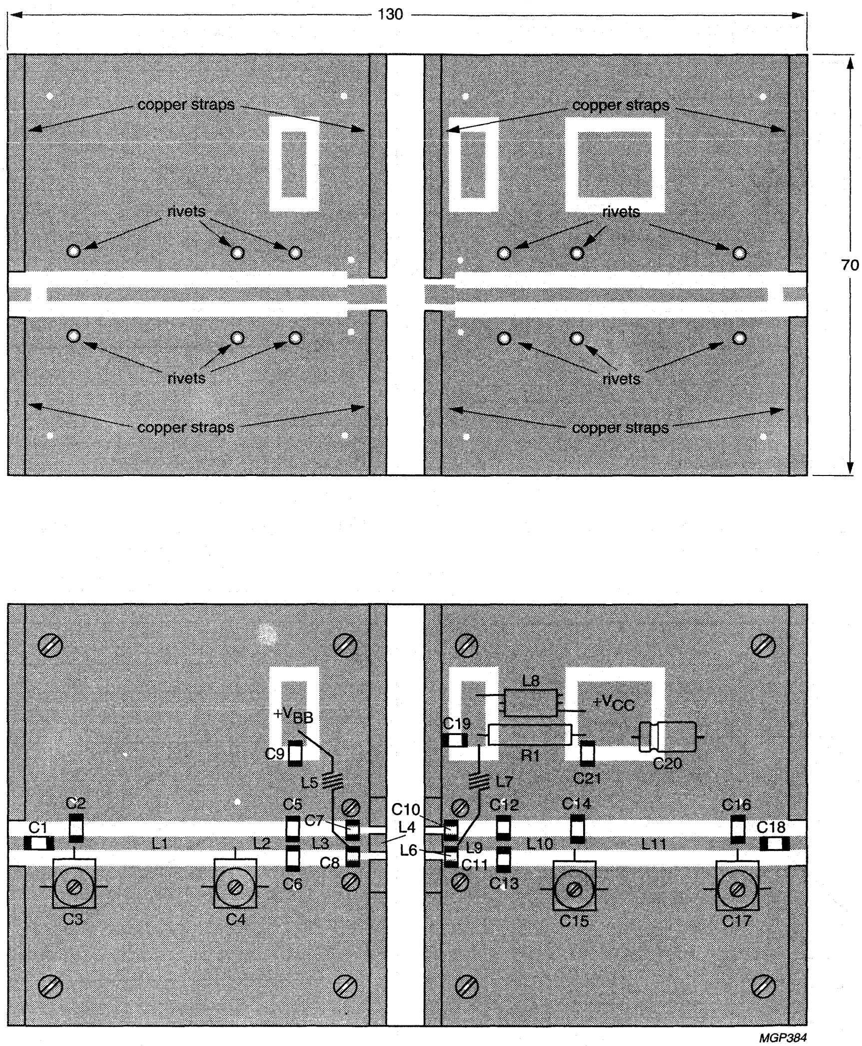
Fig.6 Class-AB test circuit at 860 MHz.

List of components (see Figs 6 and 7).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C18	multilayer ceramic chip capacitor; note 1	33 pF		
C2, C14, C16	multilayer ceramic chip capacitor; note 1	3.6 pF		
C3, C4, C15, C17	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C5, C6	multilayer ceramic chip capacitor; note 1	1.8 pF		
C7, C8	multilayer ceramic chip capacitor	6.2 pF		
C9, C21	multilayer ceramic chip capacitor; note 1	330 pF		
C10, C11	multilayer ceramic chip capacitor; note 2	5.6 pF		
C12	multilayer ceramic chip capacitor; note 1	5.6 pF		
C13	multilayer ceramic chip capacitor; note 1	6.2 pF		
C19	multilayer ceramic chip capacitor; note 1	10 pF		
C20	electrolytic capacitor	6.8 μF; 63 V		
L1, L11	stripline; note 3	50 Ω	26 mm × 2.4 mm	
L2, L3	stripline; note 3	50 Ω	9.5 mm × 2.4 mm	
L4	stripline; note 3	42.6 Ω	6 mm × 3 mm	
L5	4 turns of closely wound 0.4 mm enamelled copper wire	60 nH	int. diameter 3 mm leads 2 × 5 mm	
L6	stripline; note 3	42.6 Ω	4 mm × 3 mm	
L7	4 turns of closely wound 1 mm enamelled Cu wire	45 nH	int. diameter 4 mm leads 2 × 5 mm	
L8	Ferroxcube HF choke	grade 3B		4312 020 36642
L9	stripline; note 3	50 Ω	9 mm × 2.4 mm	
L10	stripline; note 3	50 Ω	13.5 mm × 2.4 mm	
R1	metal film resistor	10 Ω ±5%; 1 W		

Notes

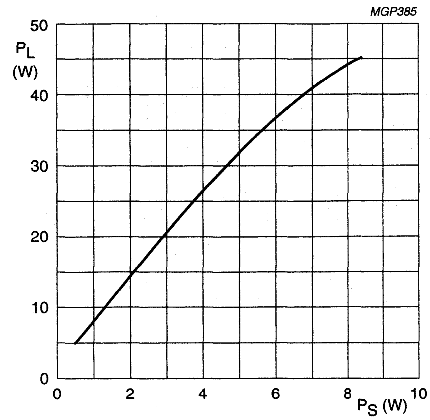
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed-circuit board with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$); thickness $1/32$".



Dimensions in mm.

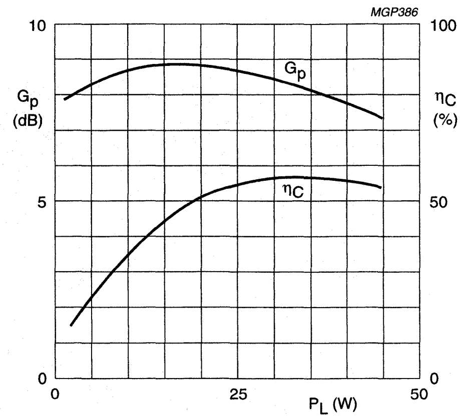
The components are situated on one side of the copper-clad PTFE-glass board, the other side is unetched and serves as a ground plane. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper on the component side and the ground plane.

Fig.7 Printed-circuit board and component layout for 860 MHz class-AB test circuit.



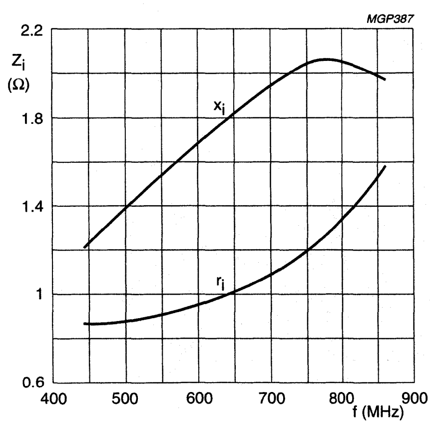
V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.4 K/W; class-AB operation.

Fig.8 Load power as a function of source power; typical values.



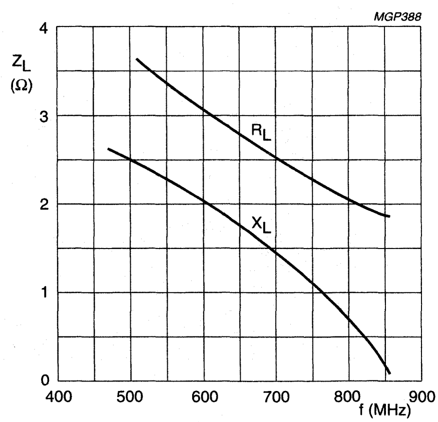
V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.4 K/W; class-AB operation.

Fig.9 Power gain and efficiency as a function of load power; typical values.



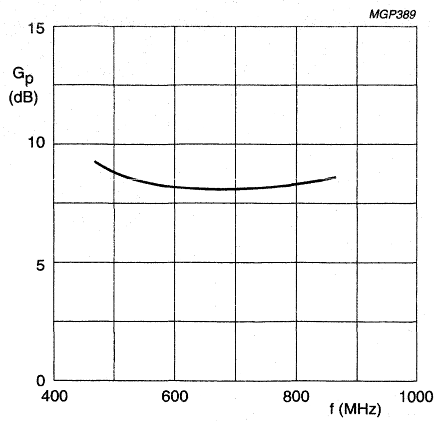
V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.10 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.11 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.12 Power gain as a function of load power; typical values.

UHF power transistor — BLV99/SL

FEATURES

- Emitter-ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

NPN silicon planar epitaxial transistor encapsulated in a 4-lead SOT172D envelope with a ceramic cap. It is designed primarily for use as a driver stage in base stations in the 900 MHz communications band. All leads are isolated from the mounting base.

PINNING - SOT172D

PIN	DESCRIPTION
1	emitter
2	base
3	collector
4	emitter

PIN CONFIGURATION

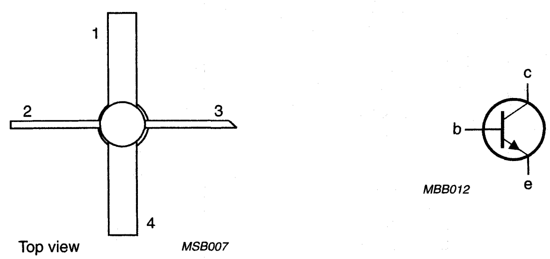


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

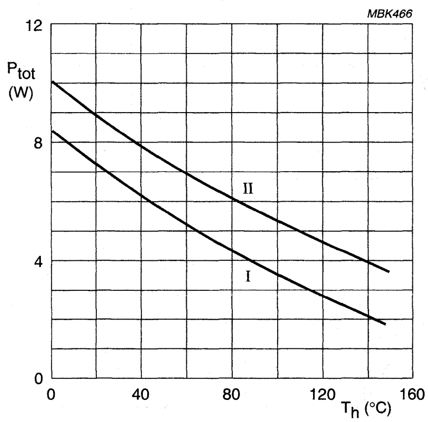
RF performance at T_{mb} = 25 °C in a common emitter class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
c.w. narrow band	900	24	2	> 8	> 55

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3.5	V
I_C	collector current	DC value	–	200	mA
I_{CM}	collector current	peak value f > 1 MHz	–	600	mA
P_{tot}	total power dissipation	f > 1 MHz; T_{mb} = 50 °C	–	6	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction operating temperature		–	200	°C



(I) Continuous RF operation.
(II) Short time operation during mismatch.

Fig.2 Power/temperature derating curves.

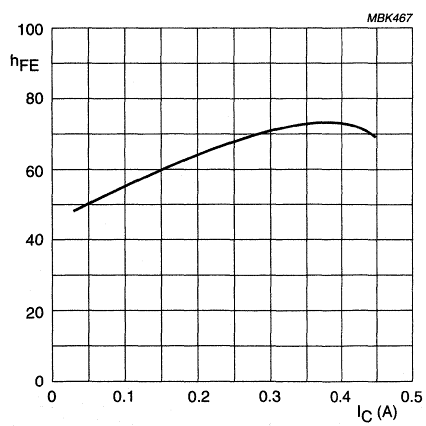
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb(RF)}$	from junction to mounting base	P_L = 4.5 W; T_{mb} = 25 °C	20	K/W

CHARACTERISTICS

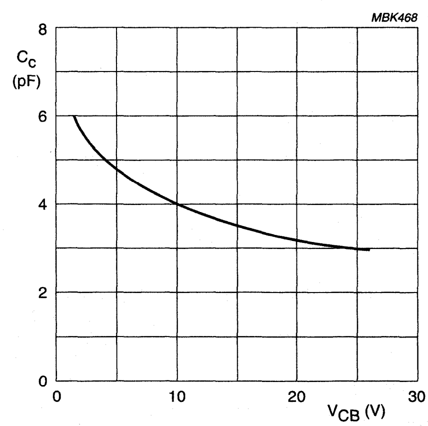
$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; $I_C = 5$ mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$V_{BE} = 0$; $I_C = 10$ mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 0.5$ mA	3.5	–	–	V
I_{CES}	collector-emitter leakage current	$V_{BE} = 0$; $V_{CE} = 27$ V	–	–	2	mA
h_{FE}	DC current gain	$V_{CE} = 20$ V; $I_C = 150$ mA	25	–	–	
E_{SBR}	second breakdown energy	L = 25 mH; $R_{BE} = 10\ \Omega$; f = 50 Hz	0.5	–	–	mJ
C_c	collector capacitance	$V_{CB} = 24$ V; $I_E = I_e = 0$; f = 1 MHz	–	3	–	pF
C_{re}	feedback capacitance	$V_{CE} = 24$ V; $I_C = 0$; f = 1 MHz	–	1.3	–	pF



$V_{CE} = 20$ V; $T_j = 25$ °C.

Fig.3 DC current gain as a function of collector current, typical values.



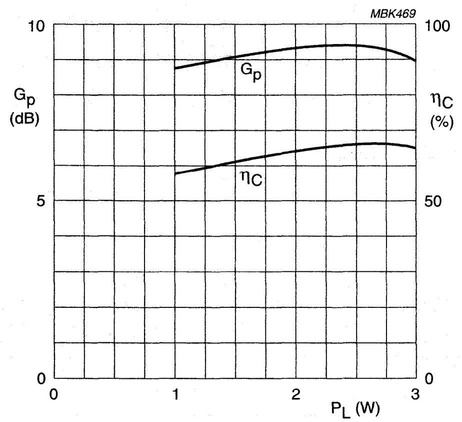
$I_E = i_e = 0$; f = 1 MHz.

Fig.4 Collector capacitance as a function of collector-base voltage, typical values.

APPLICATION INFORMATION

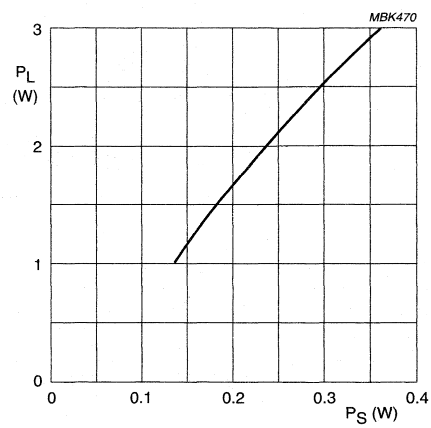
RF performance T_{mb} = 25 °C in a common emitter class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_c (%)
c.w. narrow band	900	24	2	> 8 typ. 9.3	> 55 typ. 63



Class-B operation; V_{CE} = 24 V; f = 900 MHz;
T_{mb} = 25 °C.

Fig.5 Gain and efficiency as functions of load power, typical values.



Class-B operation; V_{CE} = 24 V; f = 900 MHz;
T_{mb} = 25 °C.

Fig.6 Load power as a function of drive power, typical values.

Ruggedness in class-B operation

The BLV99/SL is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{CE} = 24 V, f = 900 MHz,
T_{mb} = 25 °C, and rated output power.

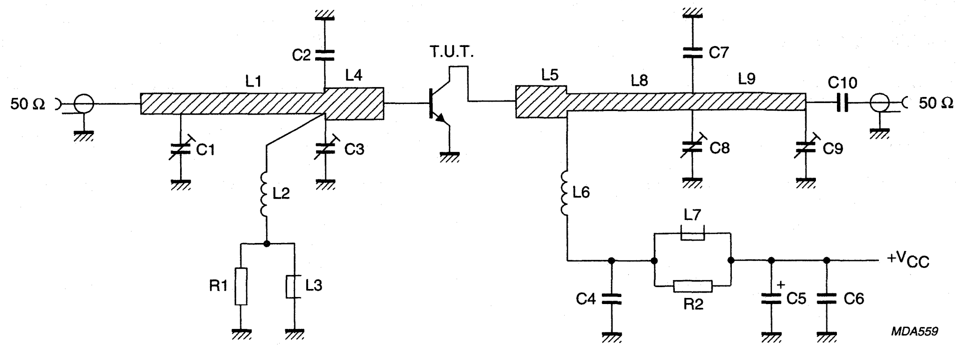


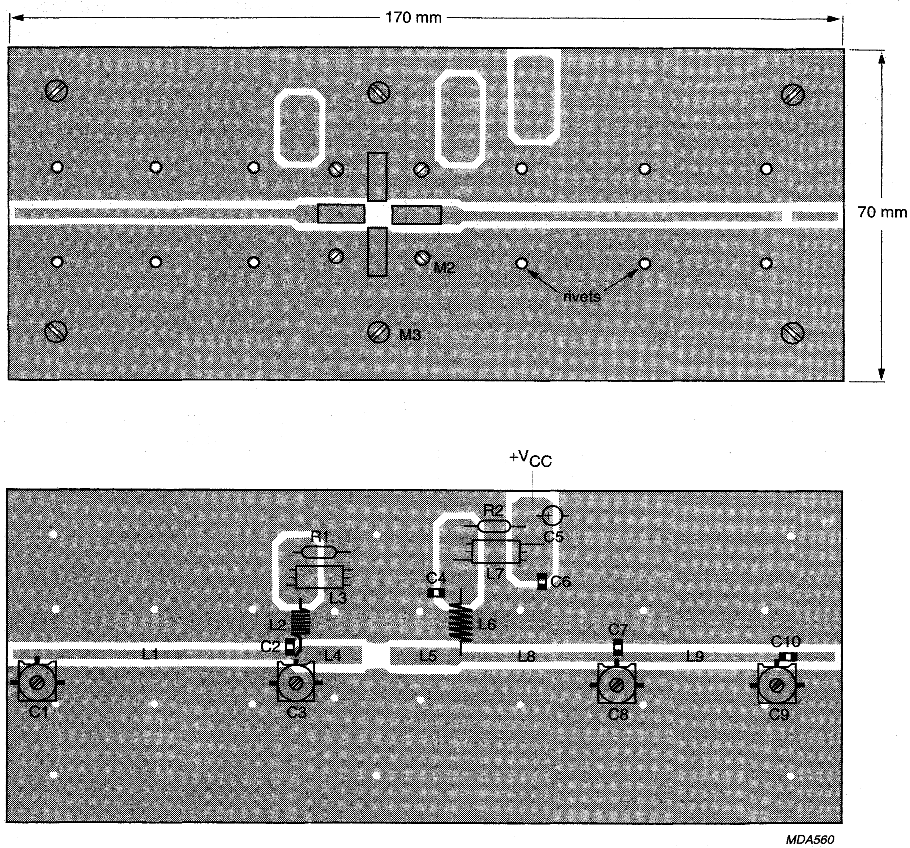
Fig.7 Class-B test circuit at f = 900 MHz.

List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C8, C9	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C2	multilayer ceramic chip capacitor (note 1)	4.7 pF		
C4, C6, C10	multilayer ceramic chip capacitor	220 pF		
C5	63 V electrolytic capacitor	1 μF		
C7	multilayer ceramic chip capacitor (note 1)	2.2 pF		
L1	stripline (note 2)	50 Ω	48 mm × 2.4 mm	
L2	7 turns enamelled 0.4 mm copper wire	50 nH	int. dia. 2 mm; leads 2 × 5 mm	
L3, L7	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L4, L5	stripline (note 2)	35 Ω	14 mm × 4 mm;	
L6	6 turns enamelled 1 mm copper wire	120 nH	int. dia. 6 mm; length 10 mm; leads 2 × 5 mm	
L8	stripline (note 2)	50 Ω	31 mm × 2.4 mm	
L9	stripline (note 2)	50 Ω	29 mm × 2.4 mm	
R1, R2	0.4 W metal film resistor	10 Ω, 5%		

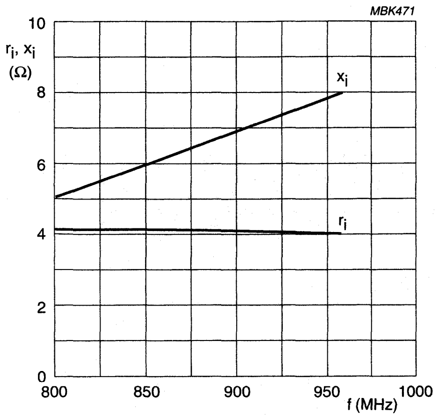
Notes

1. American Technical Ceramics type 100A or capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness $\frac{1}{32}$ inch.



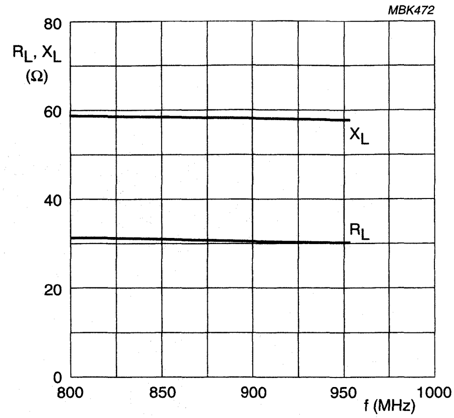
The components are mounted on one side of a copper clad PTFE fibre-glass board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by fixing screws, hollow rivets and copper straps under the emitters.

Fig.8 Component layout for 900 MHz class-B test circuit.



Class-B operation; V_{CE} = 24 V; P_L = 2 W;
T_{mb} = 25 °C.

Fig.9 Input impedance (series components) as a function of frequency, typical values.



Class-B operation; V_{CE} = 24 V; P_L = 2 W;
T_{mb} = 25 °C.

Fig.10 Load impedance (series components) as a function of frequency , typical values.

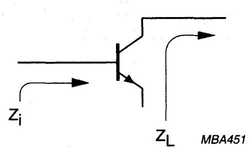
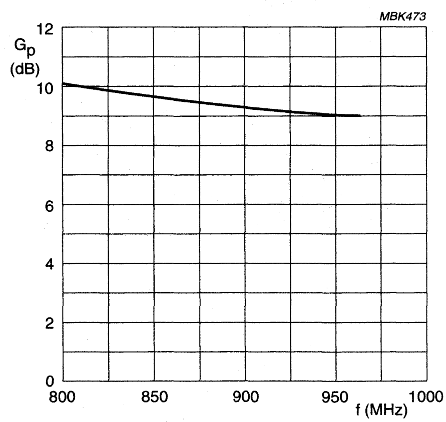


Fig.11 Definition of transistor impedance.



Class-B operation; V_{CE} = 24 V; P_L = 2 W;
T_{mb} = 25 °C.

Fig.12 Power gain as a function of frequency, typical values.

UHF power transistor BLV103

FEATURES

- Internal matching for an optimum wideband capability and high gain
- Emitter-ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

NPN silicon planar epitaxial transistor encapsulated in a 6-lead SOT171 flange envelope with a ceramic cap. It is intended for common emitter, class-AB operation in cellular radio base stations in the 960 MHz frequency band. All leads are isolated from the mounting base.

PINNING - SOT171

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

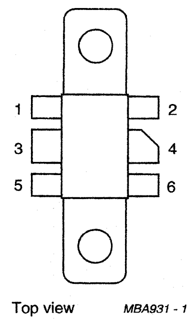
MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
c.w. class-AB	960	24	4	> 11.5	> 45

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

PIN CONFIGURATION



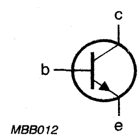
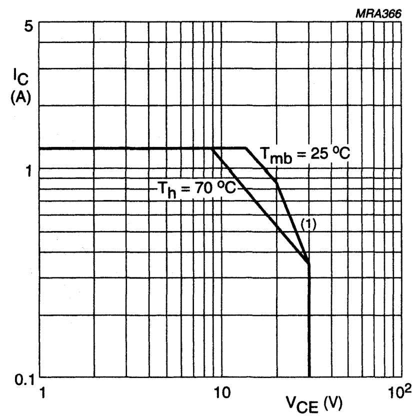


Fig.1 Simplified outline and symbol.

LIMITING VALUES

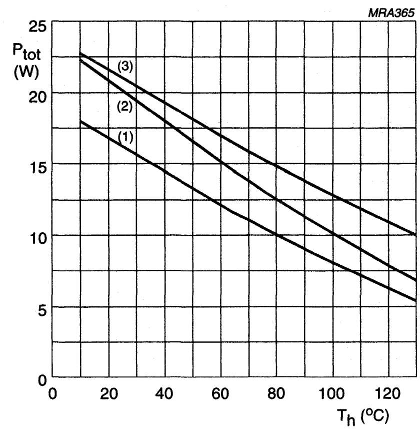
In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current	DC or average value	–	1.25	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	17	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction operating temperature		–	200	°C



(1) Second breakdown limit (independent of temperature).

Fig.2 DC SOAR.



(1) Continuous DC operation.
(2) Continuous RF operation.
(3) Short time operation during mismatch.

Fig.3 Power/temperature derating.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	from junction to mounting base	T_{mb} = 25 °C; P_{dis} = 17 W	10.3	K/W
$R_{th\ mb\text{-}h}$	from mounting base to heatsink		0.4	K/W

CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; $I_C = 4$ mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; $I_C = 30$ mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 2$ mA	4	–	–	V
I_{CES}	collector-emitter leakage current	$V_{BE} = 0$; $V_{CE} = 30$ V	–	–	1	mA
h_{FE}	DC current gain	$V_{CE} = 25$ V; $I_C = 300$ mA	20	40	–	
C_c	collector capacitance	$V_{CB} = 25$ V; $I_E = I_e = 0$; f = 1 MHz	–	6.6	8	pF
C_{re}	feedback capacitance	$V_{CE} = 25$ V; $I_C = 20$ mA; f = 1 MHz	–	3.5	4.5	pF

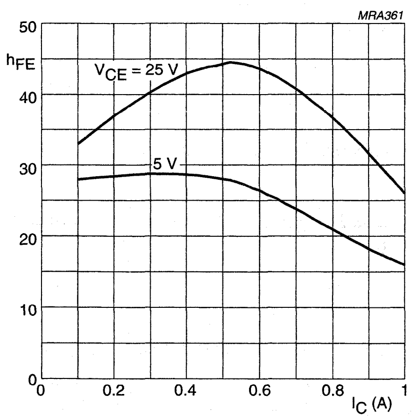
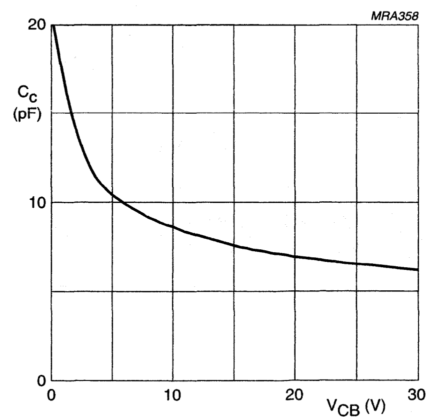


Fig.4 DC current gain as a function of collector current, typical values.



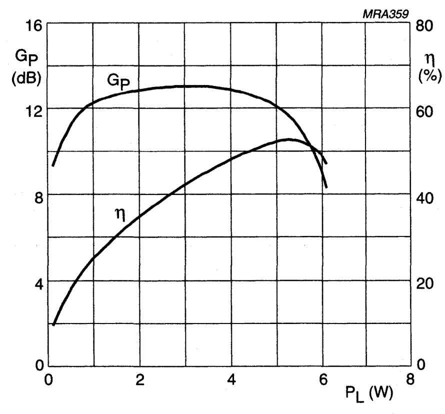
$I_E = i_e = 0$; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage, typical values.

APPLICATION INFORMATION

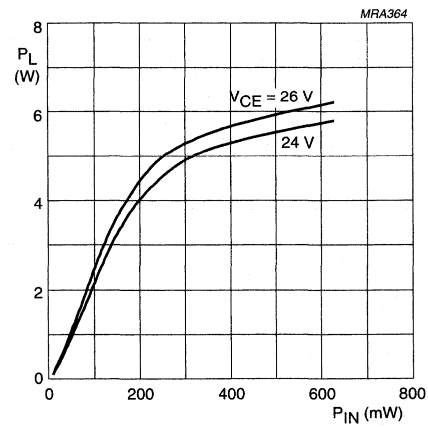
RF performance at T_h = 25 °C in a common emitter test circuit, $R_{th\ mb-h}$ = 0.4 K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_P (dB)	η_c (%)
c.w. class-AB	960	24	5	4	> 11.5 typ. 13	> 45 typ. 48
	960	26	5	4	typ. 14	typ. 50



Class-AB operation; I_{CQ} = 5 mA; f = 960 MHz;
V_{CE} = 24 V.

Fig.6 Gain and efficiency as functions of load power, typical values.



Class-AB operation; I_{CQ} = 5 mA; f = 960 MHz.

Fig.7 Load power as a function of drive power, typical values.

Ruggedness in class-AB operation

The BLV103 is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases at rated output power under the following conditions:

V_{CE} = 24 V; f = 960 MHz; T_h = 25 °C;
$R_{th\ mb-h}$ = 0.4 K/W.

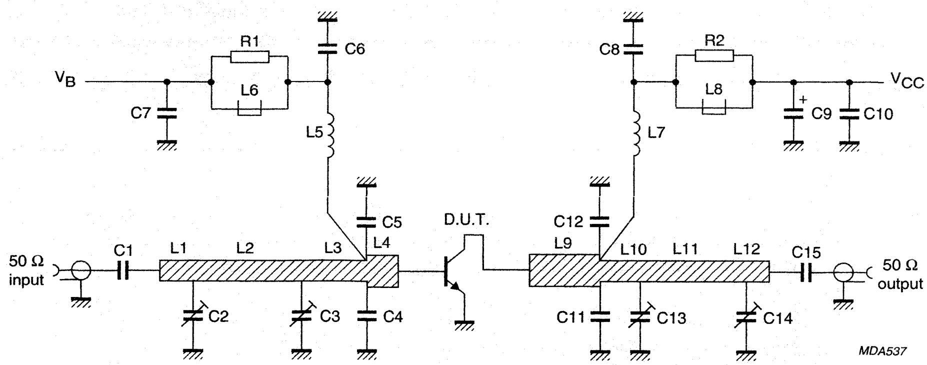


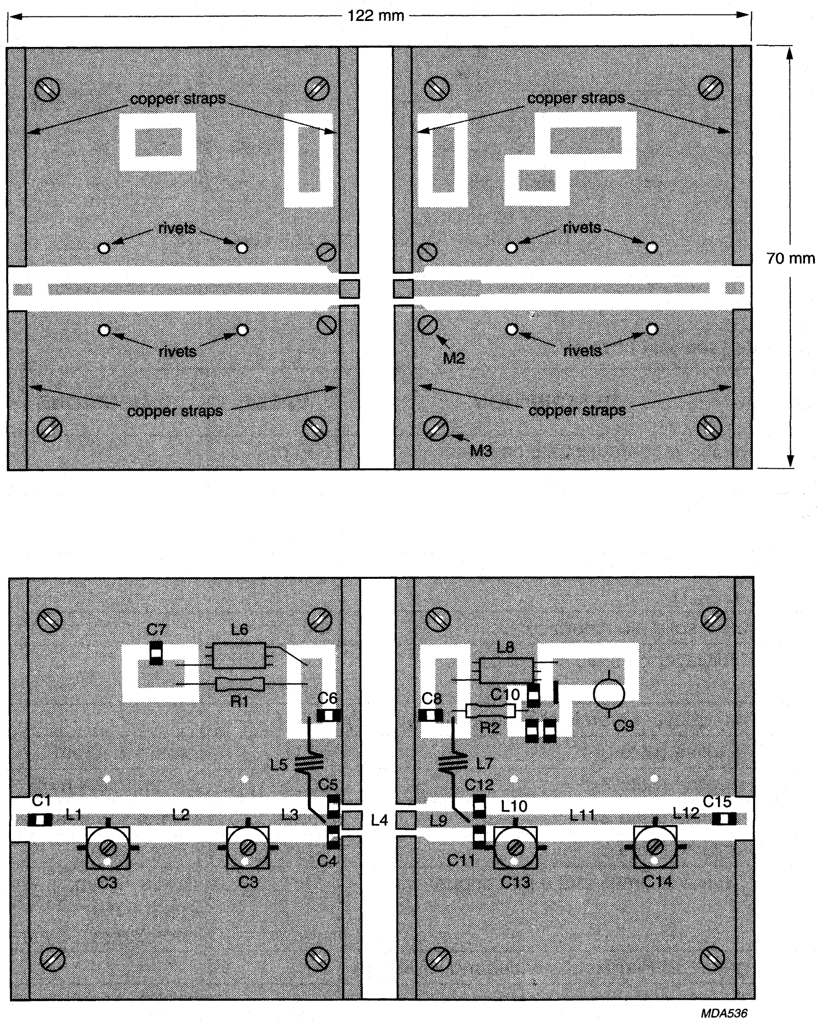
Fig.8 Class-AB test circuit at f = 960 MHz.

List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C7, C8, C15	multilayer ceramic chip capacitor	330 pF		
C2, C3, C13, C14	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C4, C5	multilayer ceramic chip capacitor (note 1)	5.1 pF		
C9	35 V solid aluminum capacitor	2.2 µF		2222 128 50228
C10	multilayer ceramic chip capacitor	3 × 100 nF in parallel		
C11, C12	multiplayer ceramic chip capacitor (note 2)	6.2 pF		
L1, L12	stripline (note 3)	50 Ω	9 mm × 2.4 mm	
L2, L11	stripline (note 3)	50 Ω	23 mm × 2.4 mm	
L3	stripline (note 3)	50 Ω	16 mm × 2.4 mm	
L4	stripline (note 3)	43 Ω	3 mm × 3 mm	
L5	3 turns enamelled 0.8 mm copper wire		int. dia. 3 mm; length 5 mm; leads 2 mm × 5 mm	
L6, L8	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	4 turns enamelled 0.8 mm copper wire		int. dia. 4 mm; length 5 mm; leads 2 mm × 5 mm	
L9	stripline (note 3)	43 Ω	14.5 mm × 3 mm	
L10	stripline (note 3)	50 Ω	4.5 mm × 2.4 mm	
R1, R2	0.4 W metal film resistor	10 Ω		2322 151 71009

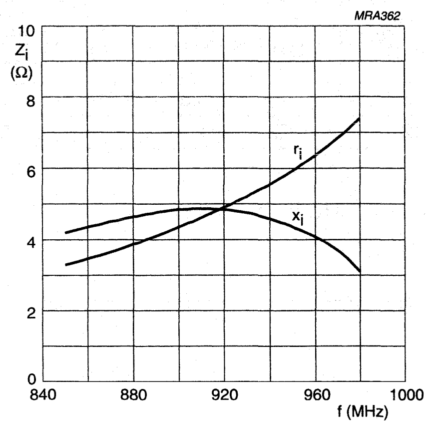
Notes

1. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2); thickness $^1/_{32}$ inch.



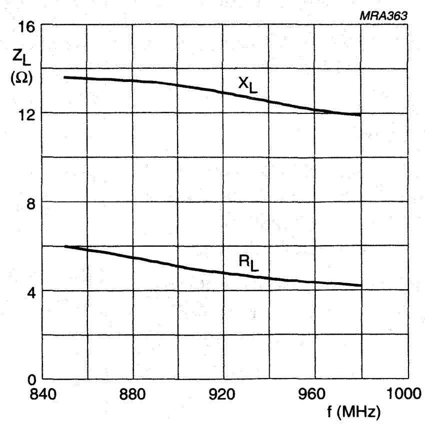
The circuit and components are situated on one side of a copper-clad PTFE fibre-glass board; the other side is fully metallized and serves as a ground plane. Connections are made by means of fixing screws, hollow rivets and copper straps around the board and under the emitters, to provide a direct contact between the components side and the ground plane.

Fig.9 Component layout for 960 MHz class-AB test circuit.



Class-AB operation; V_{CE} = 24 V; I_{CQ} = 5 mA;
P_L = 4 W; T_h = 25 °C.

Fig.10 Input impedance (series components) as a function of frequency, typical values.



Class-AB operation; V_{CE} = 24 V; I_{CQ} = 5 mA;
P_L = 4 W; T_h = 25 °C.

Fig.11 Load impedance (series components) as a function of frequency, typical values.

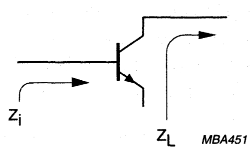
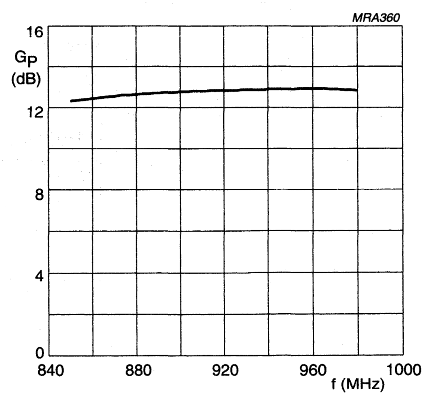


Fig.12 Definition of transistor impedance.



Class-AB operation; V_{CE} = 24 V; I_{CQ} = 5 mA;
P_L = 4 W; T_h = 25 °C.

Fig.13 Power gain as a function of frequency, typical values.

UHF power transistor — BLV193

FEATURES

- Emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

NPN silicon planar epitaxial transistor intended for common emitter class-A and class-AB operation in the 900 MHz communications band.

The transistor has a SOT171 flange envelope with a ceramic cap. All leads are isolated from the mounting base.

PINNING - SOT171

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dB) (note 1)
c.w. class-AB	900	12.5	12	≥ 6.5	≥ 50	–
c.w. class-A	900	12	6 (PEP)	typ. 11	–	typ. –30

Note

1. 2-tone measurement, f_p = 900 MHz, f_q = 901 MHz.

PIN CONFIGURATION

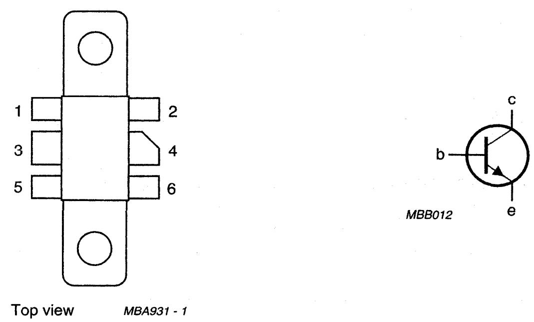


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	36	V
V_{CEO}	collector-emitter voltage	open base	–	16	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current	DC or average value	–	3.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	44	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	200	°C

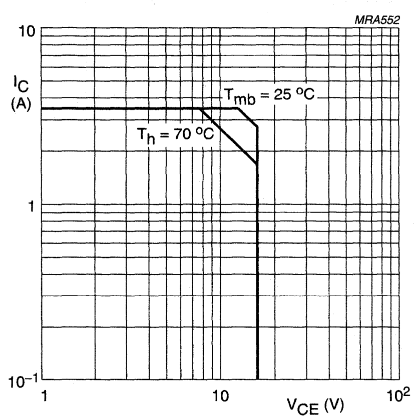
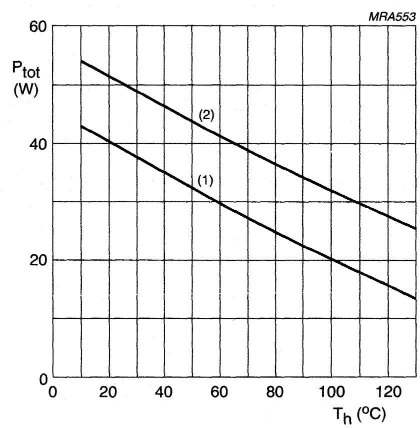


Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short time operation during mismatch.

Fig.3 Power derating curves.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	from junction to mounting base	P_{dis} = 44 W; T_{mb} = 25 °C	4.0 K/W
$R_{th\ mb\text{-}h}$	from mounting base to heatsink		0.4 K/W

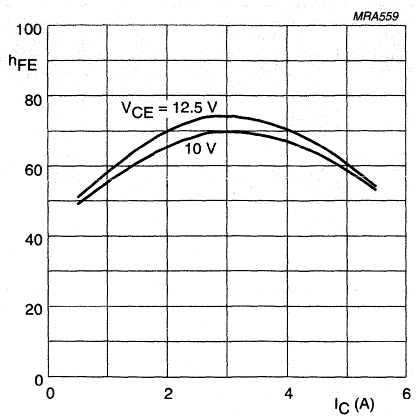
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_c = 20 mA	36	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_c = 40 mA	16	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.5 mA	3	–	–	V
I_{CES}	collector-emitter leakage current	V_{CE} = 16 V; V_{BE} = 0	–	–	1	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_c = 1.2 A; note 1	25	60	–	
C_c	collector capacitance	V_{CB} = 12.5 V; $I_E = I_e$ = 0; f = 1 MHz	–	24.5	–	pF
C_{re}	feedback capacitance	V_{CE} = 12.5 V; I_c = 0; f = 1 MHz	–	13	–	pF
$C_{c\text{-}mb}$	collector-mounting base capacitance		–	2	–	pF

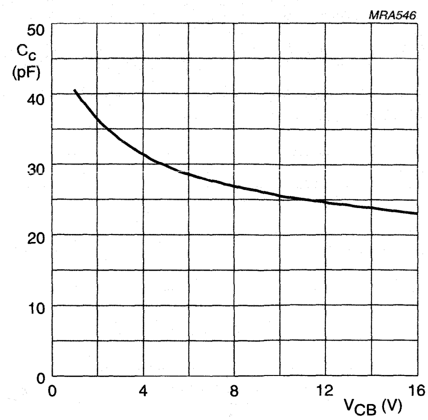
Note

1. Measured under pulse conditions: $t_p \leq 200$ µs; $\delta \leq 0.02$.



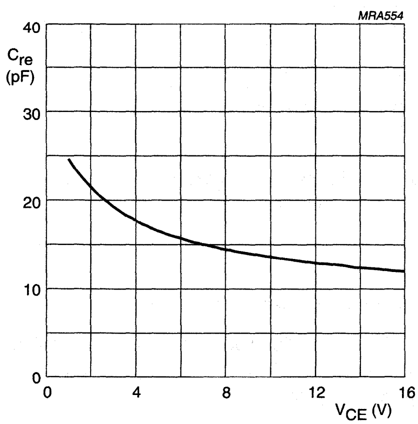
Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0.02$.

Fig.4 DC current gain as a function of collector current, typical values.



$I_E = i_e = 0$; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage, typical values.



f = 1 MHz.

Fig.6 Feedback capacitance as a function of collector-emitter voltage, typical values.

UHF power transistor BLV193

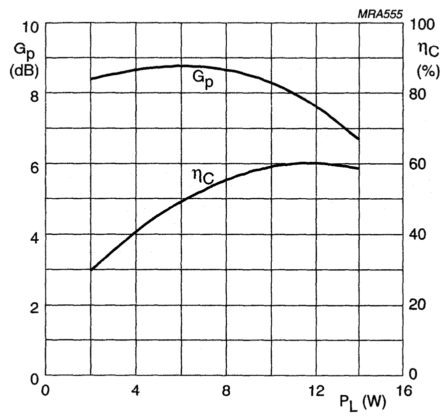
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter test circuit; $R_{th\ j\text{-}mb}$ = 0.4 K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	P_L (W)	G_P (dB)	η_c (%)	d_{im} (dB) (note 1)
c.w. class-AB	900	12.5	0.01	12	≥ 6.5 typ. 7.5	> 50 typ. 60	–
c.w. class-A	900	12	1.3	6 (PEP)	typ. 11	–	typ. –30

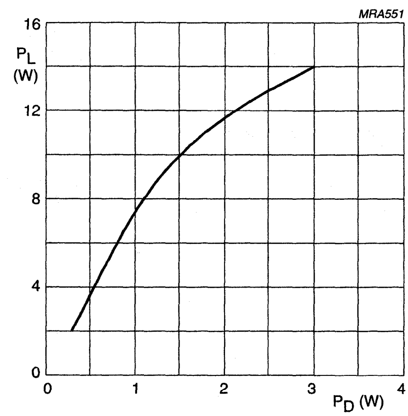
Note

1. 2-tone measurement, f_p = 900 MHz, f_q = 901 MHz.



Class-AB operation; V_{CE} = 12.5 V; f = 900 MHz; I_{CQ} = 10 mA.

Fig.7 Gain and efficiency as functions of load power, typical values.



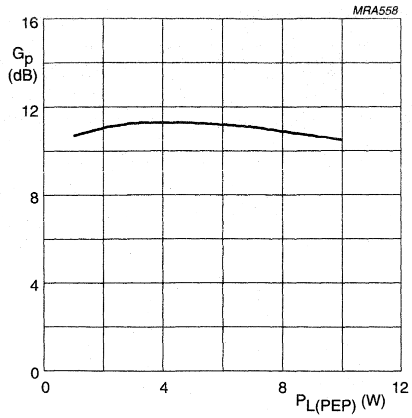
Class-AB operation; V_{CE} = 12.5 V; f = 900 MHz; I_{CQ} = 10 mA.

Fig.8 Load power as a function of drive power, typical values.

Ruggedness in class-AB operation

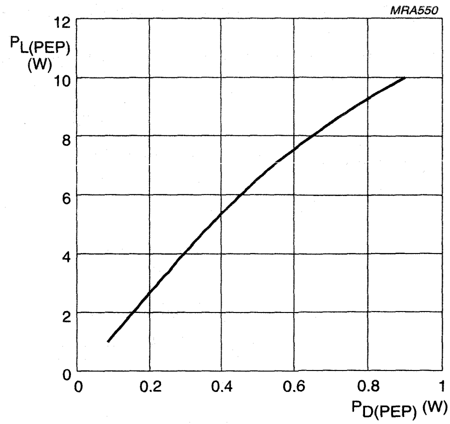
The BLV193 is capable of withstanding a load mismatch corresponding to VSWR = 10:1 through all phases under the following conditions:

V_{CE} = 15.5 V, f = 900 MHz,
T_h = 25 °C, $R_{th\ j\text{-}mb}$ = 0.4 K/W, and rated output power.



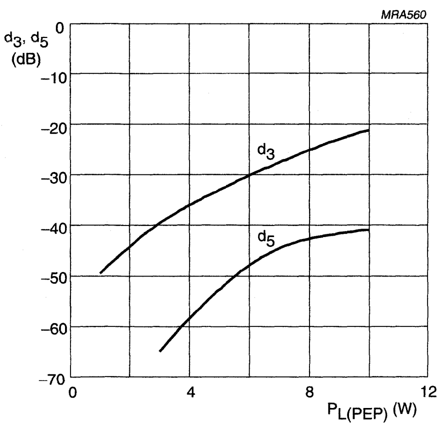
Class-A operation; V_{CE} = 12 V; I_C = 1.3 A;
f_p = 900 MHz; f_q = 901 MHz.

Fig.9 Gain as a function of load power (PEP), typical values.



Class-A operation; V_{CE} = 12 V; I_C = 1.3 A;
f_p = 900 MHz; f_q = 901 MHz.

Fig.10 Load power (PEP) as a function of drive power (PEP), typical values.



Class-A operation; V_{CE} = 12 V; I_C = 1.3 A;
f_p = 900 MHz; f_q = 901 MHz.

Fig.11 Intermodulation products as a function of load power (PEP), typical values.

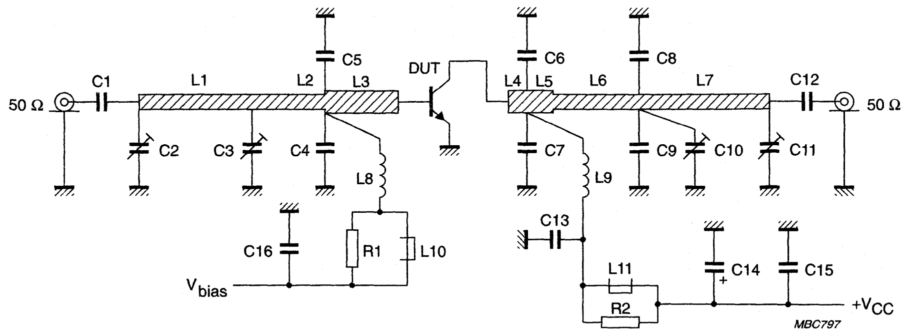


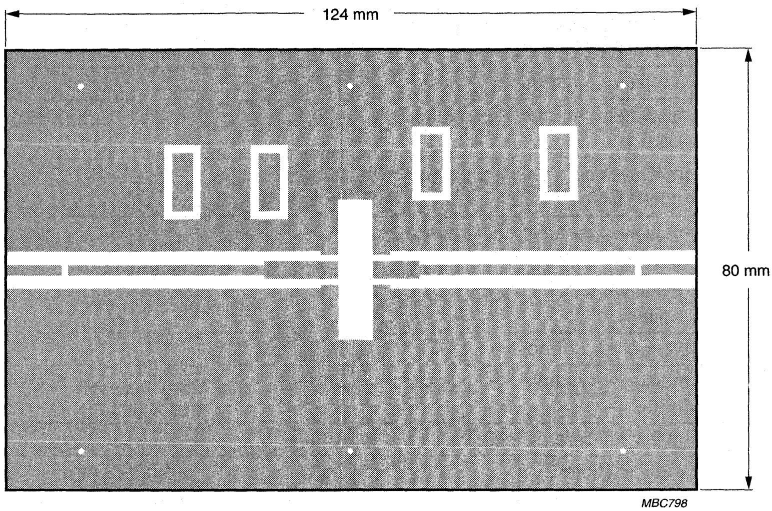
Fig.12 Class-A and class-AB test circuit at f = 900 MHz.

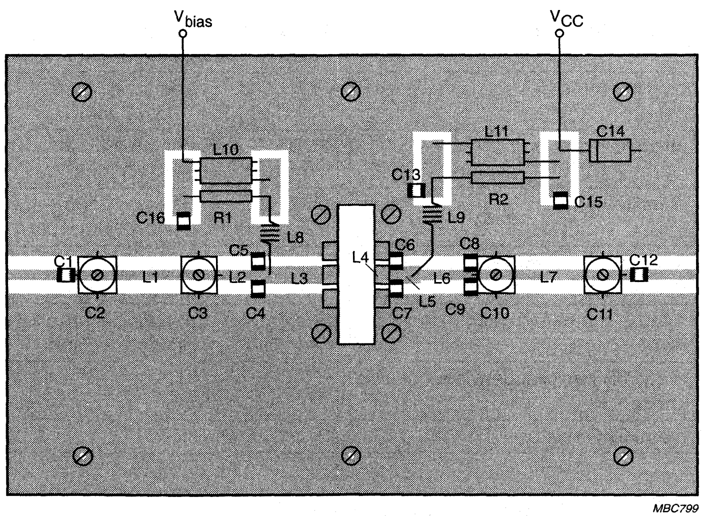
List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C12	multilayer ceramic chip capacitor (note 1)	33 pF		
C2, C3, C10, C11	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C4, C5	multilayer ceramic chip capacitor (note 1)	4.7 pF		
C6, C7	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C8, C9	multilayer ceramic chip capacitor (note 1)	3.3 pF		
C13	multilayer ceramic chip capacitor (note 1)	10 pF		
C14	electrolytic capacitor	6.8 μF, 63 V		
C15	multilayer ceramic chip capacitor (note 1)	330 pF		
C16	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1, L7	stripline (note 2)	50 Ω	length 29 mm; width 2.4 mm	
L2	stripline (note 2)	50 Ω	length 6 mm; width 2.4 mm	
L3	stripline (note 2)	42.7 Ω	length 13.1 mm; width 3 mm	
L4	stripline (note 2)	42.7 Ω	length 4.4 mm; width 3 mm	
L5	stripline (note 2)	42.7 Ω	length 4.6 mm; width 3 mm	
L6	stripline (note 2)	50 Ω	length 7 mm; width 2.4 mm	
L8	4 turns closely wound enamelled 0.4 mm copper wire	60 nH	int. dia 3 mm; leads 2 × 5 mm	
L9	4 turns enamelled 1 mm copper wire	45 nH	int. dia. 4 mm; leads 2 × 5 mm	
L10, L11	grade 3B Ferroxcube wideband HF choke			4312 020 36642
R1, R2	metal film resistor	10 Ω, 0.25 W		

Notes

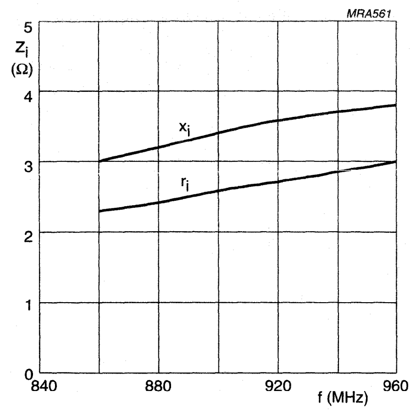
1. American Technical Ceramics type 100A or capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness $^1/_{32}$ inch.





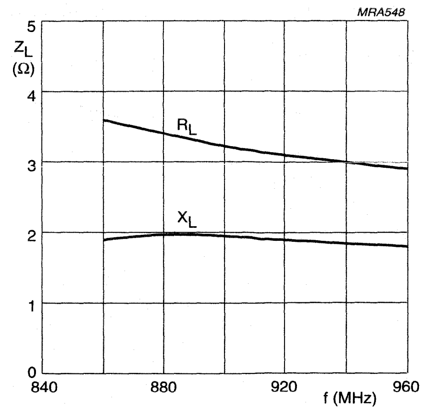
The components are mounted on one side of a copper clad PTFE fibre-glass board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by fixing screws and copper straps under the emitter leads.

Fig.13 Printed circuit board and component layout for 900 MHz test circuit.



Class-AB operation; V_{CE} = 12.5 V; I_{CQ} = 10 mA;
P_L = 12 W; T_h = 25 °C.

Fig.14 Input impedance (series components) as a function of frequency, typical values.



Class-AB operation; V_{CE} = 12.5 V; I_{CQ} = 10 mA;
P_L = 12 W; T_h = 25 °C.

Fig.15 Load impedance (series components) as a function of frequency, typical values.

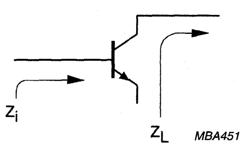
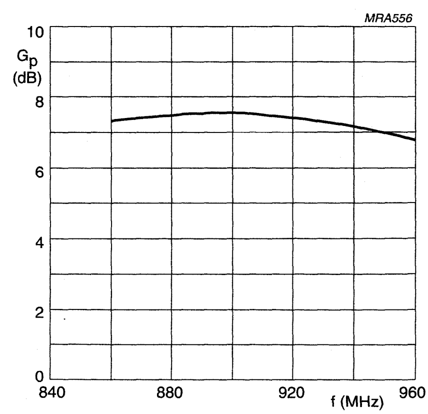
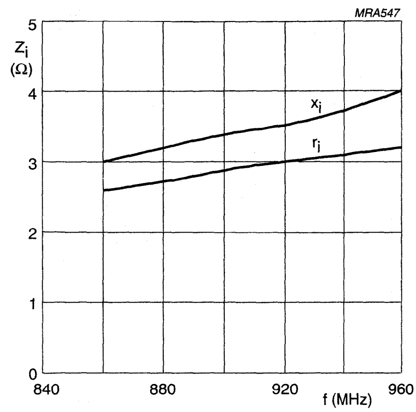


Fig.16 Definition of transistor impedance.



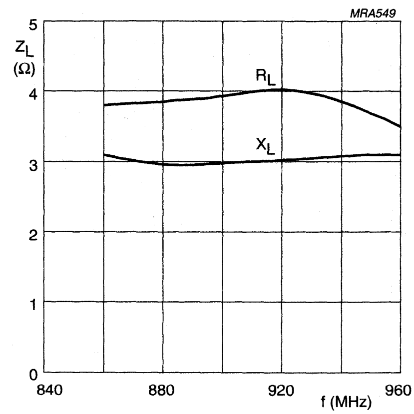
Class-AB operation; V_{CE} = 12.5 V; I_{CQ} = 10 mA;
P_L = 12 W; T_h = 25 °C.

Fig.17 Power gain as a function of frequency, typical values.



Class-A operation; V_{CE} = 12 V; I_C = 1.3 A; T_h = 25 °C.

Fig.18 Input impedance (series components) as a function of frequency, typical values.



Class-A operation; V_{CE} = 12 V; I_C = 1.3 A; T_h = 25 °C.

Fig.19 Load impedance (series components) as a function of frequency, typical values.

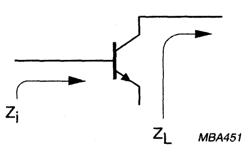
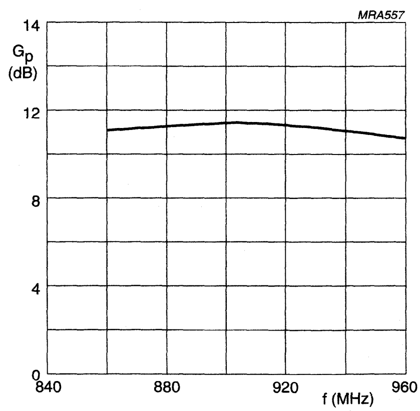


Fig.20 Definition of transistor impedance.



Class-A operation; V_{CE} = 12 V; I_C = 1.3 A; T_h = 25 °C.

Fig.21 Power gain as a function of frequency, typical values.

UHF power transistor BLV194

FEATURES

- Emitter-ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

NPN silicon planar epitaxial transistor intended for common emitter class-AB operation in the 900 MHz communications band.

The transistor has a SOT171 flange envelope with a ceramic cap.

All leads are isolated from the mounting base.

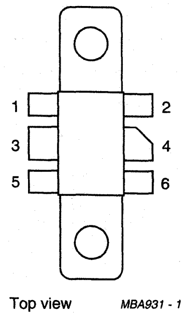
PINNING - SOT171

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	900	12.5	16	≥ 7	≥ 50



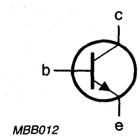


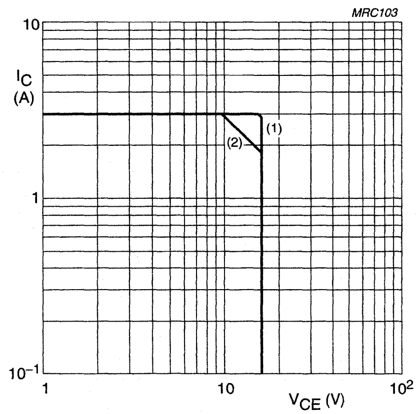
Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

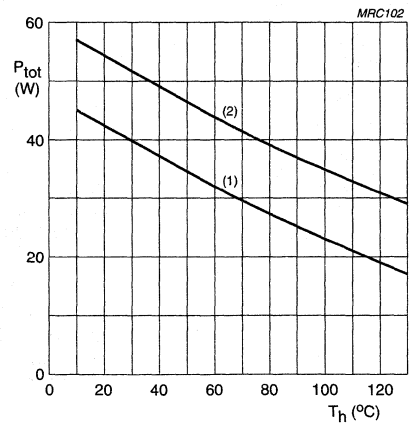
In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	open base	–	16	V
V_{CES}	collector-emitter voltage	base short-circuited	–	32	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	DC collector current		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	46	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C



(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{dis} = 46 W; T_{mb} = 25 °C	3.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4 K/W

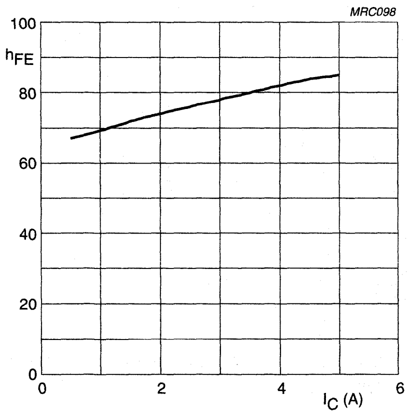
CHARACTERISTICS

T_j = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_B = 0; I_C = 40 mA	16	–	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 20 mA; V_{BE} = 0	32	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 0; I_E = 5 mA	3	–	–	V
I_{CER}	collector leakage current	R_{BE} = 700 Ω; V_{CE} = 16 V	–	–	1	mA
h_{FE}	DC current gain	I_C = 1.2 A; V_{CE} = 10 V (note 1)	25	70	–	
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = 12.5 V; f = 1 MHz	–	26	–	pF
C_{re}	feedback capacitance	I_C = 0; V_{CB} = 12.5 V; f = 1 MHz	–	19	–	pF
$C_{c\text{-}mb}$	collector-mounting base capacitance		–	2	–	pF

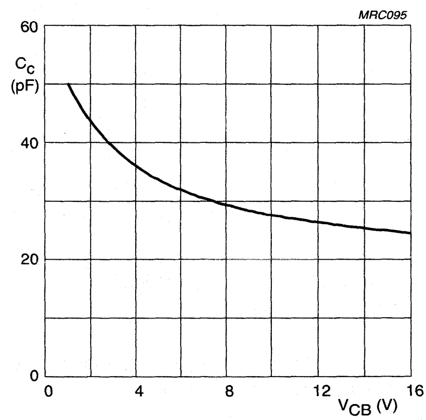
Note

1. Measured under pulse conditions: $t_p \leq 200$ µs; $\delta \leq 0.02$.



V_{CE} = 10 V.
Measured under pulse conditions: $t_p \leq 200$ µs;
$\delta \leq 0.02$.

Fig.4 DC current gain as a function of collector current, typical values.



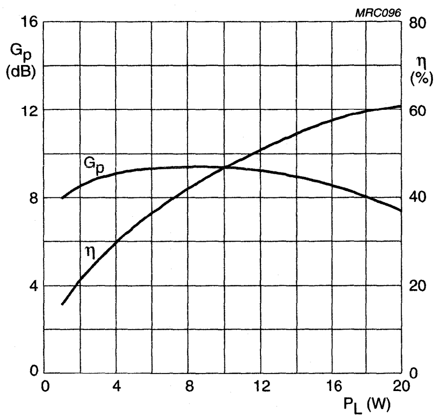
$I_E = i_e$ = 0; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage, typical values.

APPLICATION INFORMATION

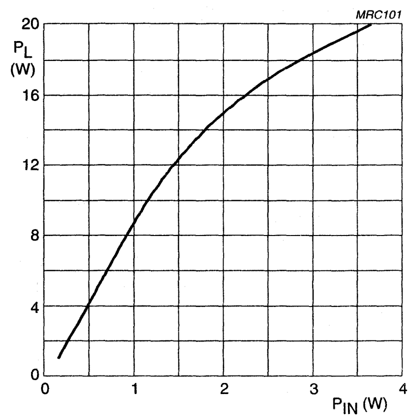
RF performance at $T_h = 25$ °C in a common emitter test circuit.
$R_{th\ j\text{-}mb} = 0.4$ K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_P (dB)	η_C (%)
CW, class-AB	900	12.5	10	16	≥ 7 typ. 8.5	≥ 50 typ. 57



Class-AB operation: $I_{CQ} = 10$ mA; $V_{CE} = 12.5$ V; f = 900 MHz.

Fig.6 Power gain and efficiency as functions of load power, typical values.



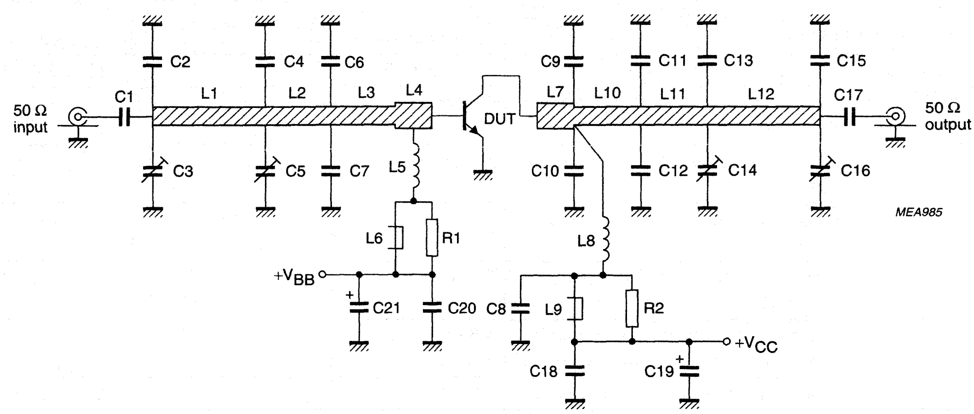
Class-AB operation: $I_{CQ} = 10$ mA; $V_{CE} = 12.5$ V; f = 900 MHz.

Fig.7 Load power as a function of input power, typical values.

Ruggedness in class-AB operation

The BLV194 is capable of withstanding a load mismatch corresponding to VSWR = 20:1 through all phases at rated output power under the following conditions:

$V_{CE} = 15.5$ V; $T_h = 25$ °C; $R_{th\ j\text{-}mb} = 0.4$ K/W; f = 900 MHz.



f = 900 MHz.

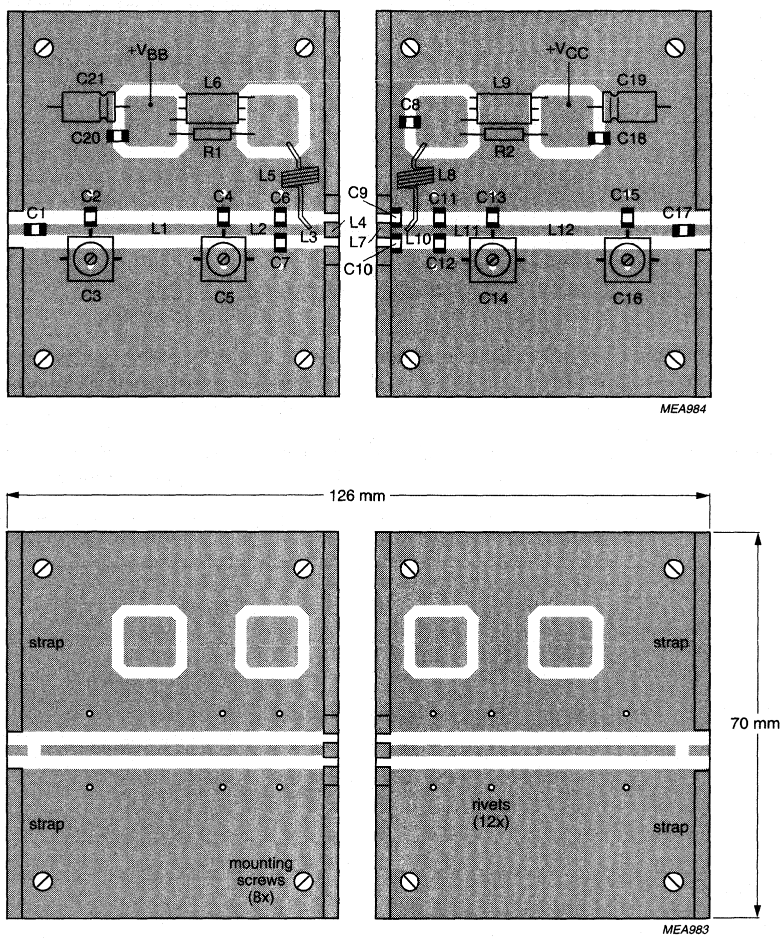
Fig.8 Class-AB test circuit.

List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C17	multilayer ceramic chip capacitor (note 1)	330 pF		
C3, C5, C14, C16	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C2, C6, C7	multilayer ceramic chip capacitor (note 1)	4.3 pF		
C4	multilayer ceramic chip capacitor (note 1)	3.9 pF		
C13, C15	multilayer ceramic chip capacitor (note 1)	4.7 pF		
C9, C10	multilayer ceramic chip capacitor (note 3)	5.6 pF		
C11, C12	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C18	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C19, C21	electrolytic capacitor	10 μF, 63 V		2222 030 37688
L1, L12	stripline (note 3)	50 Ω	length 24 mm width 2.4 mm	
L2, L11	stripline (note 3)	50 Ω	length 10 mm width 2.4 mm	
L3	stripline (note 3)	50 Ω	length 8 mm width 2.4 mm	
L4, L7	stripline (note 3)	41 Ω	length 3 mm width 3.2 mm	
L5, L8	4 turns enamelled 1 mm copper wire	45 nH	int. dia. 4 mm leads 2 × 5 mm	
L6, L9	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L10	stripline (note 3)	50 Ω	length 7 mm width 2.4 mm	
R1, R2	0.25 W metal film resistor	10 Ω		

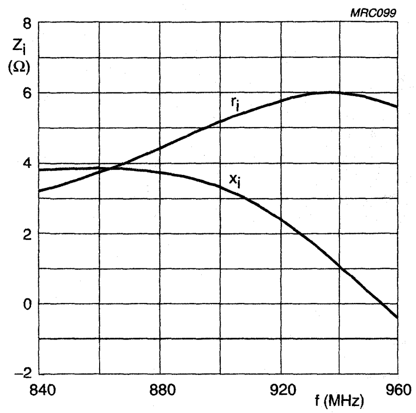
Notes

1. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed- circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness $^1/_{32}$ inch.



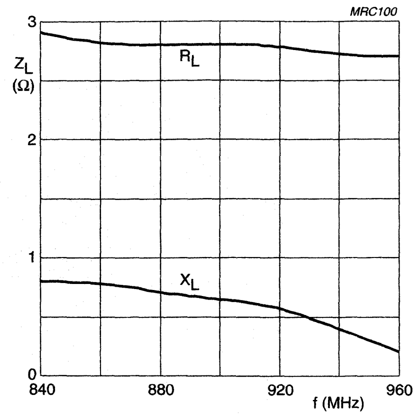
The components are mounted on one side of a copper-clad PTFE fibre-glass board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by fixing screws and copper straps under the emitter leads.

Fig.9 Component layout for 900 MHz class-AB test circuit.



Class-AB operation: I_{CQ} = 10 mA; V_{CE} = 12.5 V;
T_h = 25 °C; P_L = 16 W.

Fig.10 Input impedance as a function of frequency (series components), typical values.



Class-AB operation: I_{CQ} = 10 mA; V_{CE} = 12.5 V;
T_h = 25 °C; P_L = 16 W.

Fig.11 Load impedance as a function of frequency (series components), typical values.

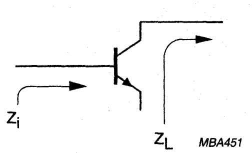
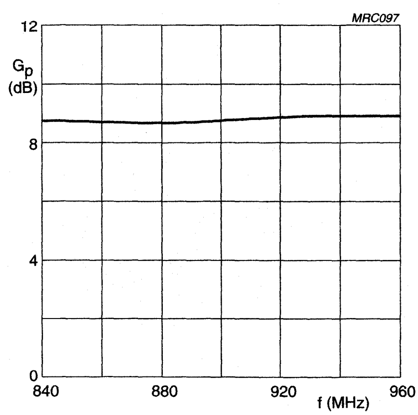


Fig.12 Definition of transistor impedance.



Class-AB operation: I_{CQ} = 10 mA; V_{CE} = 12.5 V;
T_h = 25 °C; P_L = 16 W.

Fig.13 Power gain as a function of frequency, typical values.

UHF linear push-pull power transistor BLV857

FEATURES

- Internal input matching for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATION

- Common emitter class-A operation in linear transposers/transmitters (television) in the 470 to 860 MHz frequency band.

DESCRIPTION

NPN silicon planar transistor with two sections in push-pull configuration. The device is encapsulated in a SOT324B 4-lead rectangular flange package with a ceramic cap. The common emitters are connected to the flange.

PINNING SOT324B

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1
2	c2	collector 2
3	b1	base 1
4	b2	base 2
5	e	common emitters

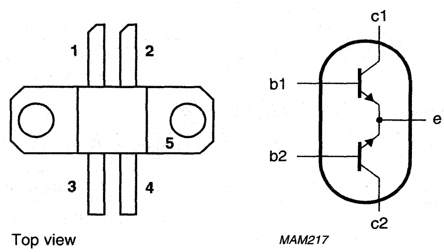


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)
CW class-A	860	25	2 × 1.1	≥10(1)	≥10(1)

Note

1. Three-tone test signal (−8, −16 and −10 dB); $d_{im} = -54$ dB.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

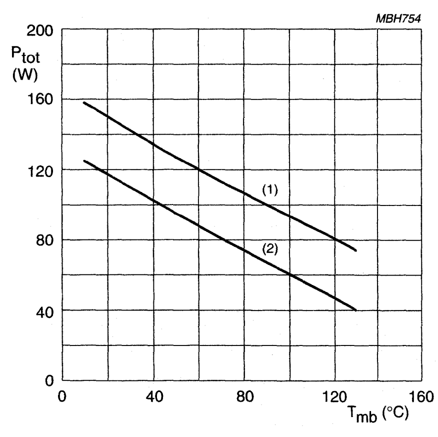
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	collector current (DC)		–	7.4	A
$I_{C(AV)}$	average collector current		–	7.4	A
P_{tot}	total power dissipation	T_{mb} = 70 °C; note 1; see Fig.2	–	80	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	P_{tot} = 80 W; T_{mb} = 70 °C note 1	1.6	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	note 1	0.4	K/W

Note to Limiting values and Thermal characteristics

1. Total device; both sections equally loaded.



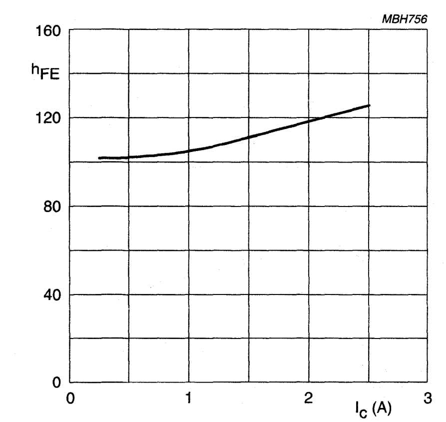
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.2 Power derating curve.

CHARACTERISTICS

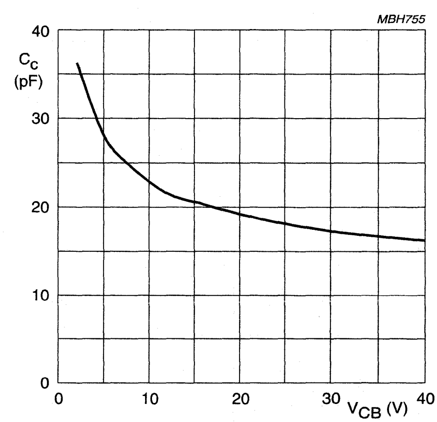
Values apply to either transistor section; T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 15 mA; I_E = 0	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 30 mA; I_B = 0	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 0.6 mA; I_C = 0	2.5	–	–	V
I_{CBO}	collector-base leakage current	V_{CB} = 27 V; V_{BE} = 0	–	–	1.5	mA
I_{CEO}	collector-emitter leakage current	V_{CE} = 20 V	–	–	3	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 1.1 A; see Fig.3	30	–	140	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz; see Fig.4	–	18	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_C = 0; f = 1 MHz	–	11	–	pF



V_{CE} = 25 V; t_p = 500 µs; δ = <1 %.

Fig.3 DC current gain as a function of collector current; typical values.



I_E = i_e = 0; f = 1 MHz.

Fig.4 Collector capacitance as a function of collector-base voltage; typical values.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull class-A test circuit.

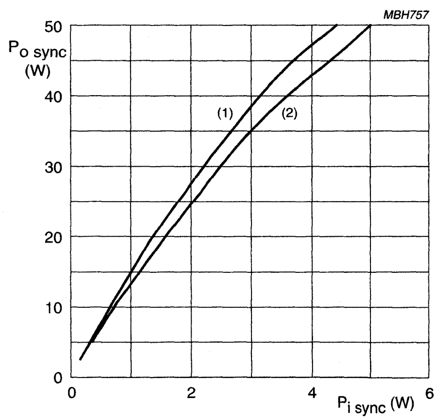
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB)
CW class-A	860	25	2 × 1.1	≥10(1)	≥10(1)	≤−54(1)
CW class-A	860	25	2 × 1.1	≥10(2)	≥10(2)	≤−51(2)

Notes

1. Three-tone test method: f_{vision} = 855.25 MHz (vision carrier −8 dB); f_{sound} = 860.75 MHz (sound carrier −10 dB); $f_{sideband}$ = 859.68 MHz (sideband signal −16 dB); 0 dB corresponds to peak sync level.
2. Three-tone test method: f_{vision} = 855.25 MHz (vision carrier −8 dB); f_{sound} = 860.75 MHz (sound carrier −7 dB); $f_{sideband}$ = 859.68 MHz (sideband signal −16 dB); 0 dB corresponds to peak sync level.

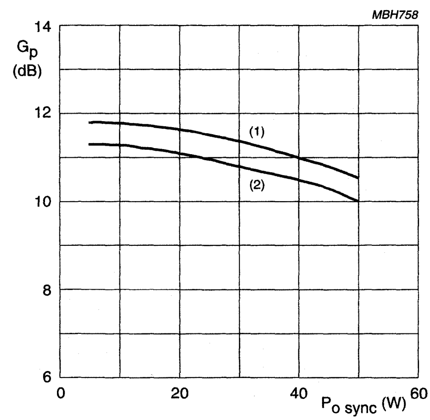
Ruggedness in class-A operation

The BLV857 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the conditions: V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; T_h = 25 °C; $P_{o\ sync}$ = 10 W.



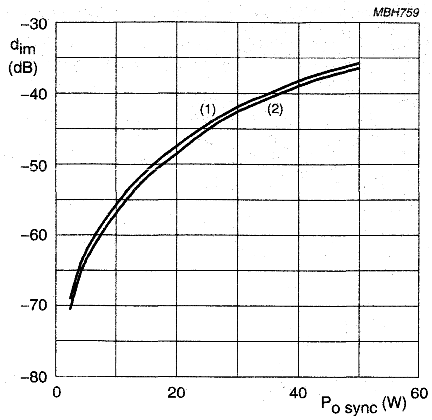
V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; (3-tone; −8/−16/−10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.5 Output power as a function of input power; typical values.



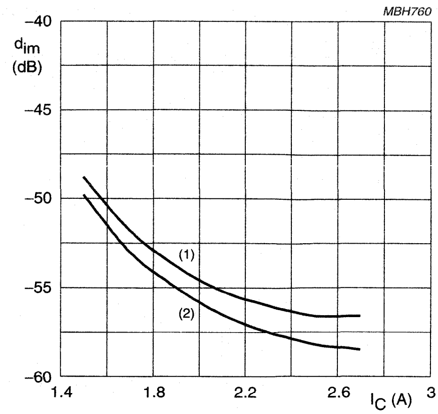
V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; (3-tone; −8/−16/−10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.6 Power gain as a function of output power; typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; (3-tone; −8/−16/−10 dB).
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.7 Intermodulation distortion as a function of output power; typical values.



V_{CE} = 25 V; f = 860 MHz; (3-tone; −8/−16/−10 dB).
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.8 Intermodulation distortion as a function of collector current; typical values.

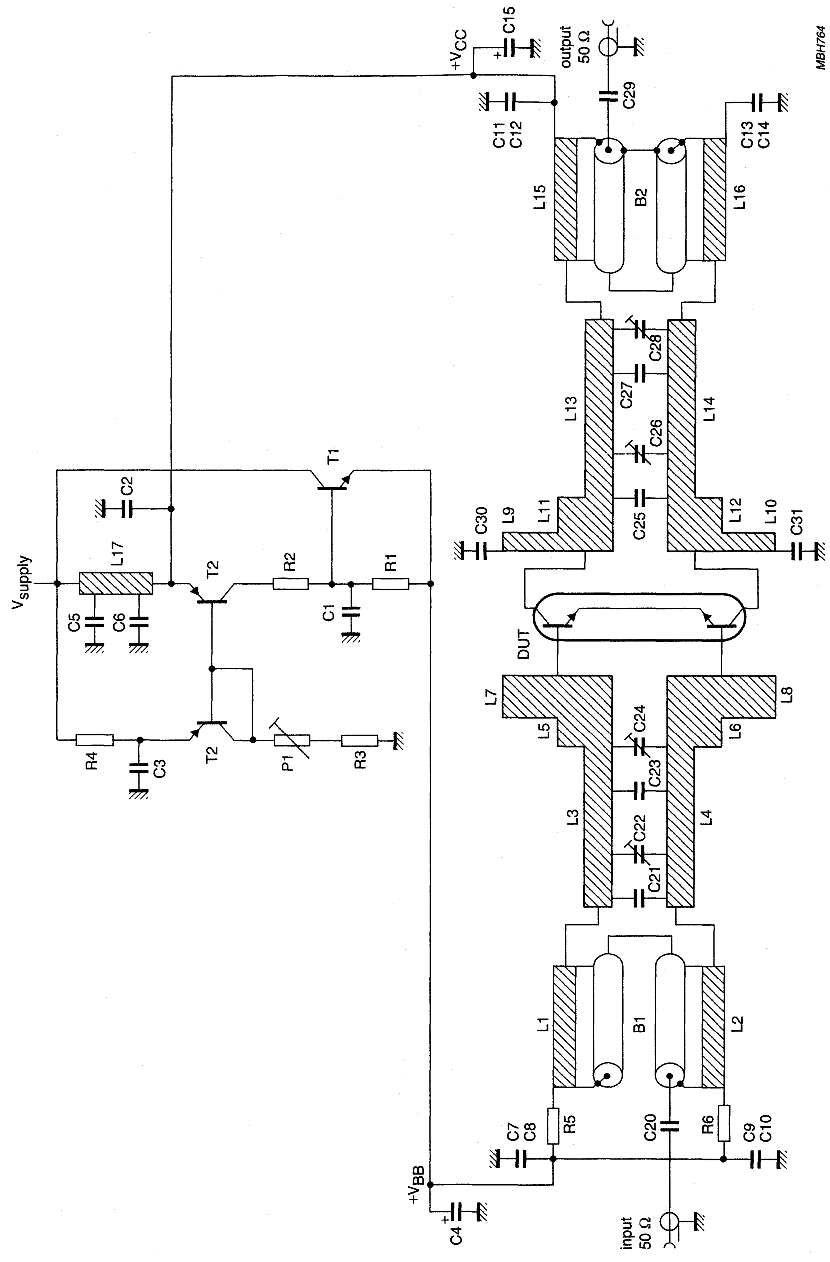
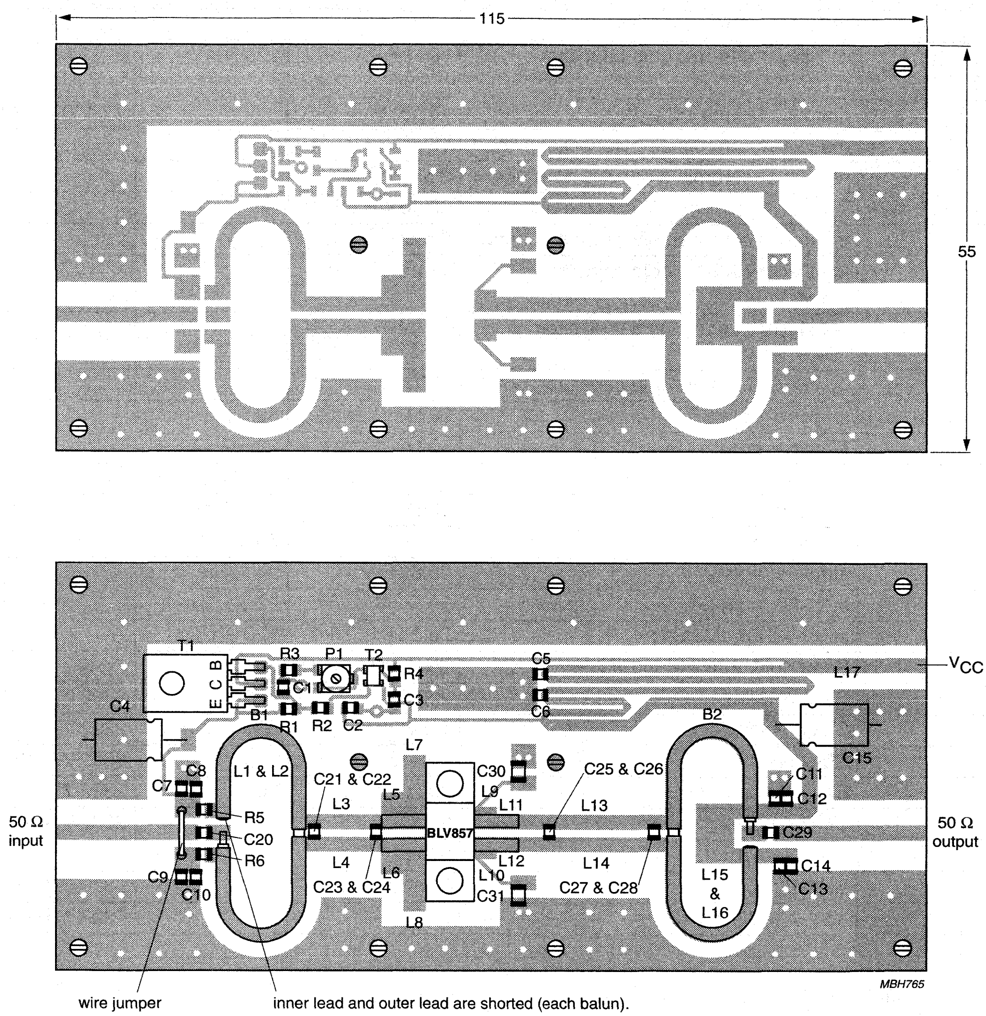


Fig.9 Class-A test circuit at f = 860 MHz.



Dimensions in mm.

The components are situated on one side of the copper-clad epoxy fibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

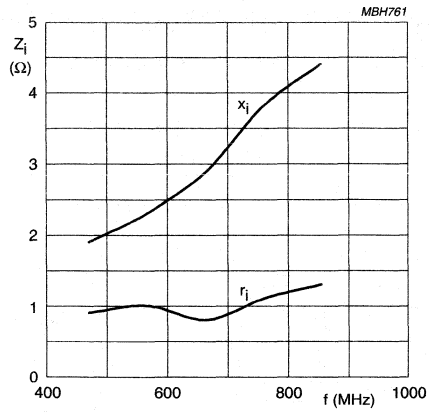
Fig.10 Printed-circuit board and component lay-out for 860 MHz class-A test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C3, C5, C6, C7, C8, C9, C10	multilayer ceramic chip capacitor	10 nF	805	2222 590 16627
C4	solid aluminium capacitor	47 μF; 25 V		2222 030 36479
C11, C12, C13, C14, C30, C31	multilayer ceramic chip capacitor	100 nF	1206	2222 591 16641
C15	solid aluminium capacitor	10 μF; 63 V		2222 030 38109
C20	multilayer ceramic chip capacitor; note 1	18 pF		
C21	multilayer ceramic chip capacitor; note 1	3 pF		
C22, C24, C26, C28	Tekelec Giga trim 37271; note 3	0.6 to 4.5 pF		
C23	multilayer ceramic chip capacitor; note 1	7.5 pF		
C25	multilayer ceramic chip capacitor; notes 1 and 3	11 pF		
C27	multilayer ceramic chip capacitor; notes 1 and 3	9.1 pF		
C29	multilayer ceramic chip capacitor; note 1	100 pF		
L1, L2, L15, L16	stripline; note 2	50 Ω	30.6 × 2 mm	
L3, L4	stripline; note 2	50 Ω	10 × 2 mm	
L5, L6	stripline; note 2	26.5 Ω	3 × 5 mm	
L7, L8	stripline; note 2	15 Ω	3 × 10 mm	
L9, L10	stripline; note 2	104 Ω	6 × 0.5 mm	
L11, L12	stripline; note 2	38.8 Ω	3 × 3 mm	
L13, L14	stripline; note 2	50 Ω	22.5 × 2 mm	
L17	stripline; notes 2 and 4	76.2 Ω	120 × 1 mm	
B1, B2	Semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	70 mm	
R1	SMD resistor	220 Ω	805	2322 734 22201
R2	SMD resistor	1.8 Ω	805	2322 734 21808
R3	SMD resistor	4.3 kΩ	805	2322 734 24302
R4	SMD resistor	33 Ω	805	2322 734 23309
R5, R6	SMD resistor	3.3 Ω	805	2322 734 23308
P1	potentiometer	2 kΩ		
T1	NPN transistor	BD139		9330 912 20112
T2	double PNP transistor	BCV62		5322 130 60505

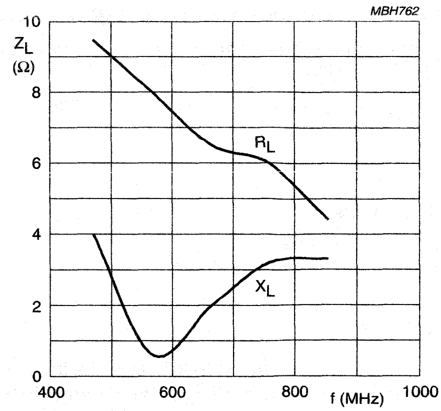
Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board: Rogers ULTRALAM 2000 (B0300M1046QB) (ε_r = 2.55); thickness 0.76 mm.
3. Position of C25 and C26: distance of centre capacitor to transistor BLV857 = 7.5 mm. Position of C27 and C28: distance of centre capacitor to balun B2 = 1.5 mm.
4. The sense resistor on the bias unit is implemented as a stripline L17, in this way we obtain a small sense resistor (approximately 80 mΩ) which can handle the dissipated power.



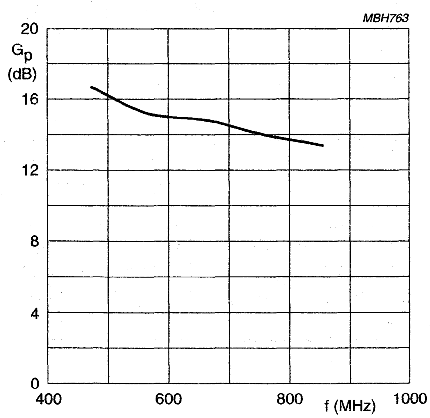
V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; $P_{o\ sync}$ = 10 W (total device); T_h = 25 °C.

Fig.11 Input impedance (per section) as a function of frequency (series components); typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; $P_{o\ sync}$ = 10 W (total device); T_h = 25 °C.

Fig.12 Load impedance (per section) as a function of frequency (series components); typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; $P_{o\ sync}$ = 10 W (total device); T_h = 25 °C.

Fig.13 Gain as a function of frequency; typical values.

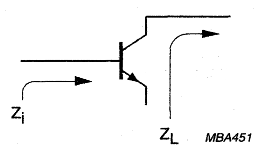


Fig.14 Definition of transistor impedance.

UHF linear push-pull power transistor BLV859

FEATURES

- Double internal input and output matching for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATION

- Common emitter class-A operation in linear transposers/transmitters (television) in the 470 to 860 MHz frequency band.

DESCRIPTION

NPN silicon planar transistor with two sections in push-pull configuration. The device is encapsulated in a SOT262B 4-lead rectangular flange package, with two ceramic caps. It delivers a $P_{o\ sync}$ = 20 W in class-A operation at 860 MHz and a supply voltage of 25 V.

PINNING SOT262B

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1
2	c2	collector 2
3	b1	base 1
4	b2	base 2
5	e	emitter

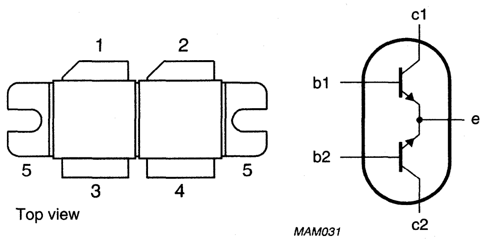


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)
CW class-A	860	25	2 × 2.25	≥20(1)	≥10(1)

Note

1. Three-tone test signal (−8, −16 and −10 dB); d_{im} = −54 dB.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

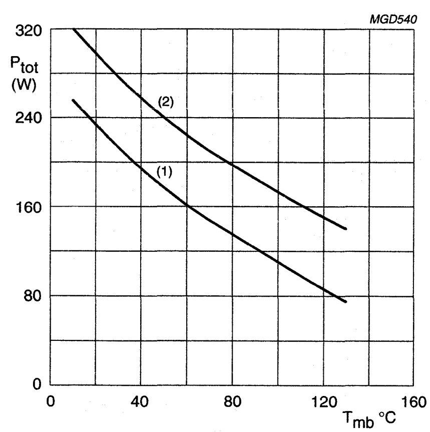
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	collector current (DC)		–	15	A
$I_{C(AV)}$	average collector current		–	15	A
P_{tot}	total power dissipation	T_{mb} = 70 °C; note 1	–	145	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	P_{tot} = 145 W; T_{mb} = 70 °C note 1	0.9	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	note 1	0.15	K/W

Note to Limiting values and Thermal characteristics

1. Total device; both sections equally loaded.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.2 Power derating curve.

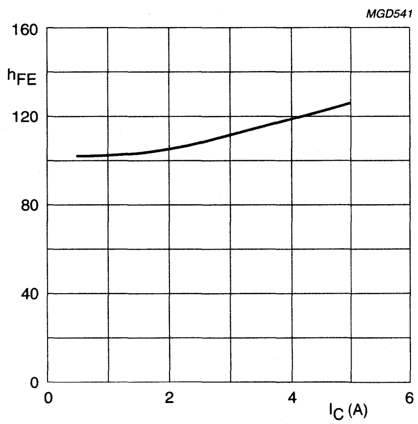
CHARACTERISTICS

Values apply to either transistor section; T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 30 mA; I_E = 0	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 60 mA; I_B = 0	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 1.2 mA; I_C = 0	2.5	–	–	V
I_{CBO}	collector-base leakage current	V_{CB} = 27 V; V_{BE} = 0	–	–	3	mA
I_{CEO}	collector-emitter leakage current	V_{CE} = 20 V	–	–	6	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 2.25 A	30	–	140	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	36(1)	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_B = 0; f = 1 MHz	–	22	–	pF

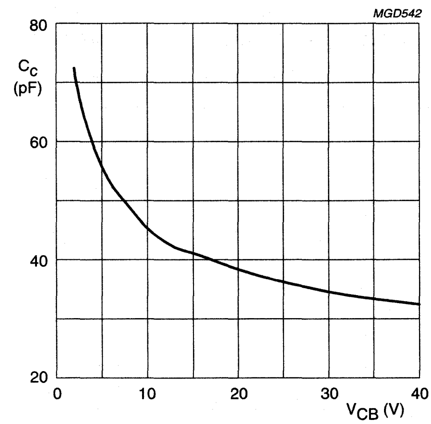
Note

1. The value of C_c is that of the die only; it is not measurable, because of the internal matching network.



V_{CE} = 25 V; t_p = 500 μs; δ = <1 %.

Fig.3 DC current gain as a function of collector current; typical values.



I_E = i_e = 0; f = 1 MHz.

Fig.4 Collector capacitance as a function of collector-base voltage; typical values.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull class-A test circuit.

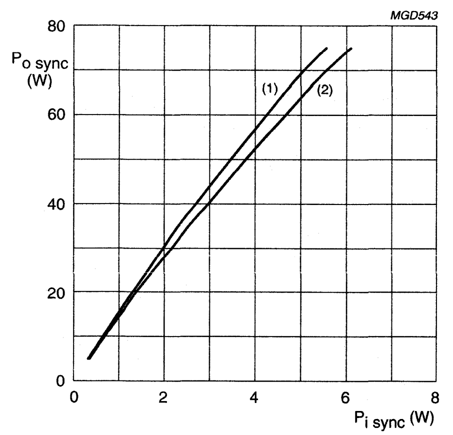
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB)
CW class-A	860	25	2 × 2.25	≥20 (1)	≥10 (1)	≤−54 (1)
CW class-A	860	25	2 × 2.25	≥20 (2)	≥10 (2)	≤−51 (2)

Notes

1. Three-tone test method (vision carrier −8 dB, sound carrier −10 dB, sideband signal −16 dB), 0 dB corresponds to peak sync level.
2. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), 0 dB corresponds to peak sync level.

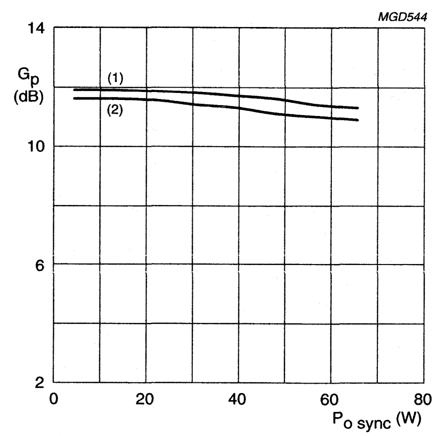
Ruggedness in class-A operation

The BLV859 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the conditions: V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; f = 860 MHz; T_h = 25 °C; $P_{o\ sync}$ = 20 W.



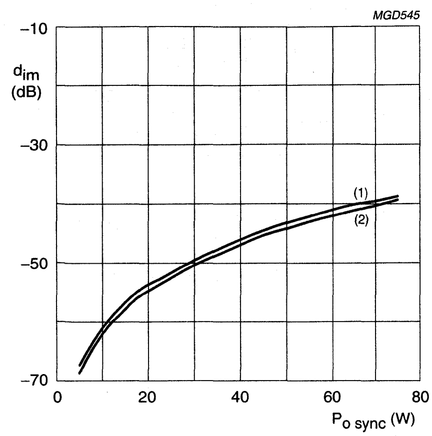
V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; f = 860 MHz; (3-tone; −8/−16/−10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.5 Output power as a function of input power; typical values.



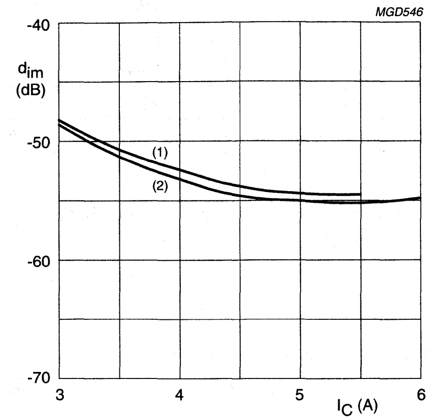
V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; f = 860 MHz; (3-tone; −8/−16/−10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.6 Power gain as a function of output power; typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.7 Intermodulation distortion as a function of output power; typical values.



V_{CE} = 25 V; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.8 Intermodulation distortion as a function of collector current; typical values.

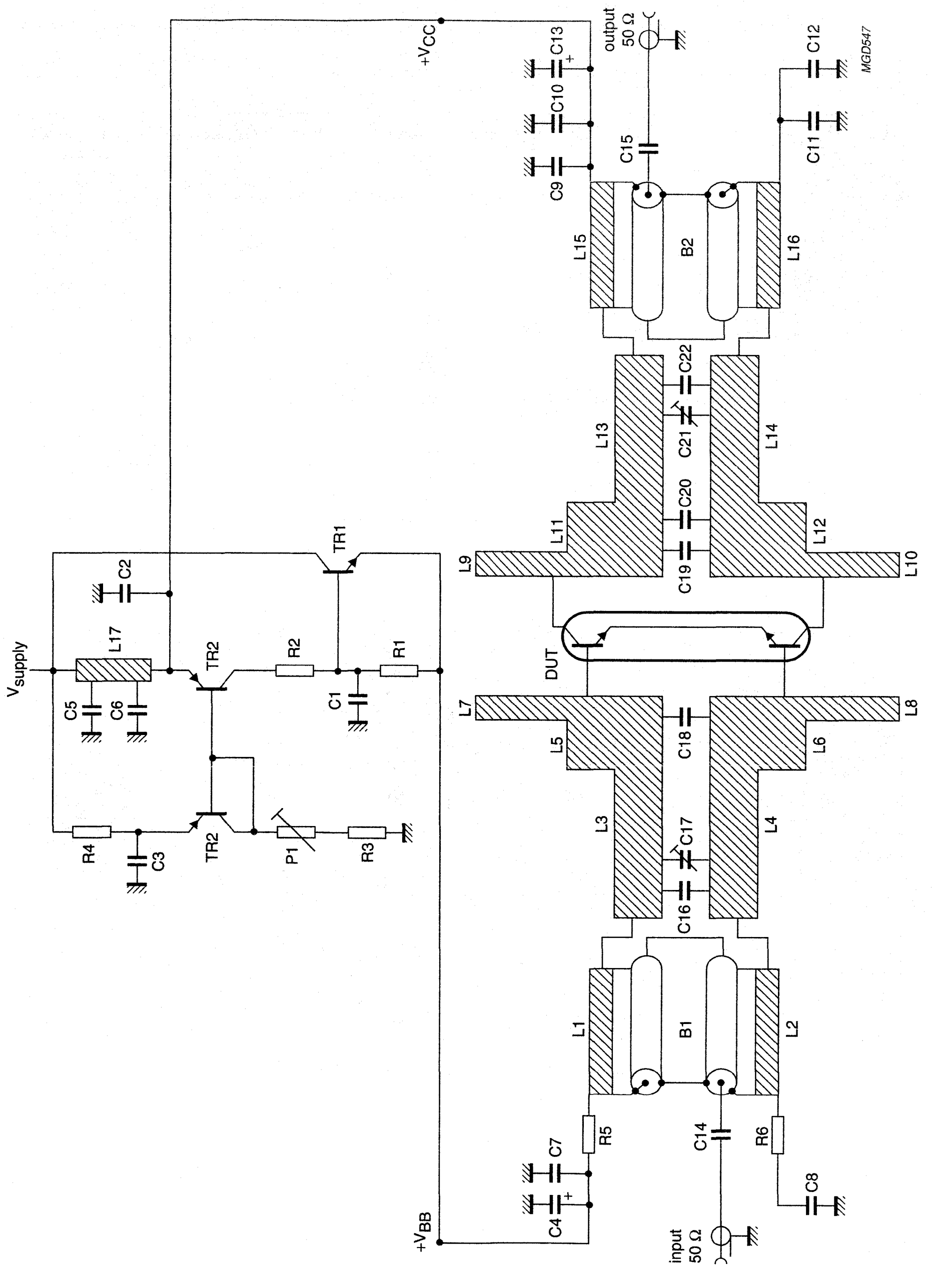
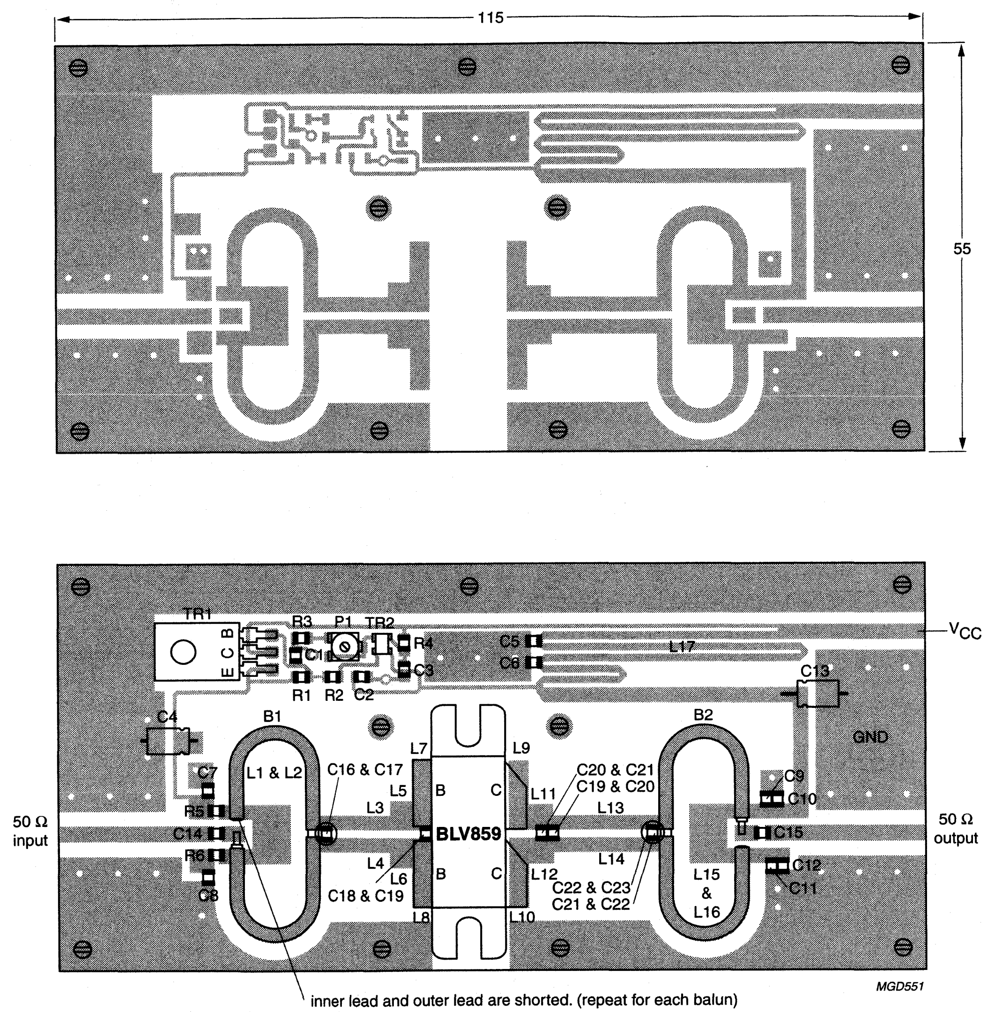


Fig.9 Class-A test circuit at f = 860 MHz.



Dimensions in mm.

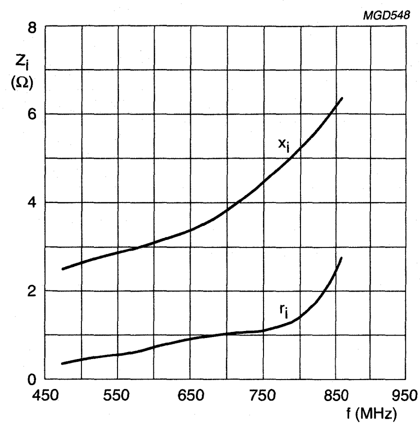
Fig.10 Printed-circuit board and component lay-out for 860 MHz class-A test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C3, C5, C6	multilayer ceramic chip capacitor;	15 nF	805	2222 590 16629
C4	solid aluminium capacitor	47 μF; 25 V		2222 030 36479
C7, C8	multilayer ceramic chip capacitor	10 nF	805	2222 590 16627
C9, C10, C11, C12	multilayer ceramic chip capacitor	100 nF	1206	2222 591 16641
C13	solid aluminium capacitor	10 μF; 63 V		2222 030 381109
C14, C15	multilayer ceramic chip capacitor; note 1	47 pF		
C16	multilayer ceramic chip capacitor; note 1	8.2 pF		
C17, C21	Tekelec Giga trim 37271	0.6 to 4.5 pF		
C18	multilayer ceramic chip capacitor; note 1	13 pF		
C19	multilayer ceramic chip capacitor; note 1	3.9 pF		
C20	multilayer ceramic chip capacitor; note 1	12 pF		
C22	multilayer ceramic chip capacitor; note 1	9.1 pF		
L1, L2, L15, L16	stripline; note 2	50 Ω	2 × 30.6 mm	
L3, L4	stripline; note 2	50 Ω	2 × 9.5 mm	
L5, L6	stripline; note 2	32.4 Ω	4 × 3 mm	
L7, L8, L9, L10	stripline; note 2	16.2 Ω	9.5 × 2.6 mm	
L11, L12	stripline; note 2	37.5 Ω	3.5 × 3.4 mm	
L13, L14	stripline; note 2	50 Ω	2 × 13.9 mm	
L17	stripline; note 2	77.7 Ω	1 × 120 mm	
B1, B2	Semi rigid coax balun UT70-25	Z = 25 Ω, ±1.5 Ω	70 mm	
R1	SMD resistor	220 Ω	805	2322 734 22201
R2	SMD resistor	1.8 Ω	805	2322 734 21808
R3	SMD resistor	2.7 kΩ	805	2322 734 22702
R4	SMD resistor	33 Ω	805	2322 734 23309
R7, R8	SMD resistor	3.3 Ω	805	2322 734 23308
P1	Murata potentiometer RG4M08-102VM-TG	1 kΩ		
TR1	NPN transistor	BD139		9330 912 20112
TR2	double PNP transistor	BVC62		5332 130 60505

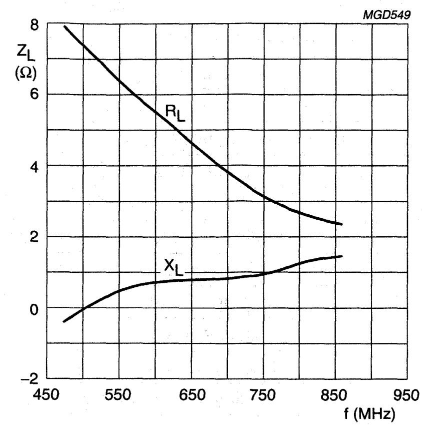
Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad PCB: Rogers ULTRALAM 200 (B0300M1046QB) (ε_r = 2.55); thickness 0.76 mm.



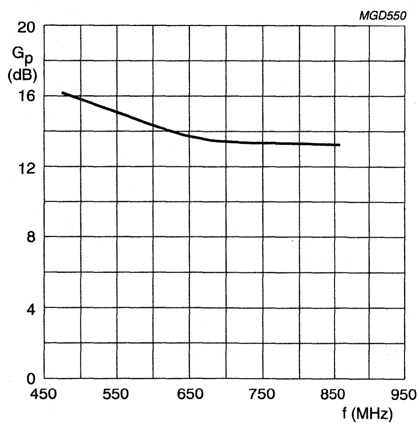
V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; $P_{o\ sync}$ = 20 W (total device); T_h = 25 °C.

Fig.11 Input impedance (per section) as a function of frequency (series components); typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; $P_{o\ sync}$ = 20 W (total device); T_h = 25 °C.

Fig.12 Load impedance (per section) as a function of frequency (series components); typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; $P_{o\ sync}$ = 20 W (total device); T_h = 25 °C.

Fig.13 Gain as a function of frequency; typical values.

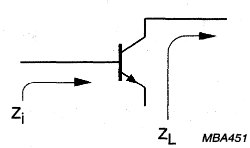


Fig.14 Definition of transistor impedance.

UHF linear push-pull power transistor BLV861

FEATURES

- Double stage internal input and output matching networks for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Common emitter class-AB output stages of television transmitter amplifiers (sound and vision) operating in bands 4 and 5 (470 to 860 MHz).

DESCRIPTION

NPN silicon planar epitaxial transistor with two sections in push-pull configuration. The device is encapsulated in a SOT289A 4-lead rectangular flange package, with a ceramic cap.

PINNING

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1; note 1
2	c2	collector 2; note 1
3	b1	base 1
4	b2	base 2
5	e	common emitters; note 2

Notes

1. Collectors c1 and c2 are internally connected.
2. Common emitters are connected to the flange.

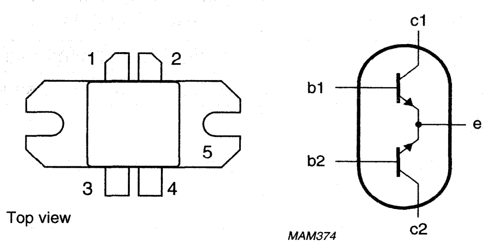


Fig.1 Simplified outline (SOT289A) and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	ΔG_p (dB)
CW class-AB	860	28	100	≥8.5	≥55	≤1

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

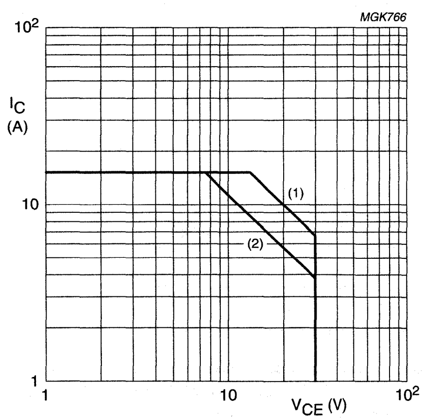
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	15	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 220 W; note 1	0.8	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.2	K/W

Note

1. Thermal resistance is determined under specified RF operating conditions.



Total device; both sections equally loaded.
(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.

CHARACTERISTICS

Values apply to either transistor section; T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_E = 0; I_C = 35 mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_B = 0; I_C = 90 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 2 mA; I_C = 0	3	–	–	V
I_{CBO}	collector-base leakage current	V_{CB} = 28 V	–	–	3	mA
h_{FE}	DC current gain	I_C = 2.8 A; V_{CE} = 10 V	30	–	120	–
Δh_{FE}	DC current gain ratio of both sections	I_C = 4.5 A; V_{CE} = 10 V	0.67	–	1.5	–
C_c	collector capacitance	I_E = i_e= 0; V_{CE} = 28 V; f = 1 MHz; note 1	–	47	–	pF

Note

1. The value of C_c is that of the die only; it is not measurable because of the internal matching network.

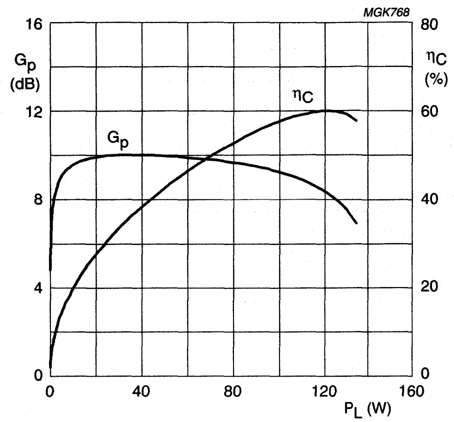
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull class-AB test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	P_L (W)	G_p (dB)	η_C (%)	ΔG_p (dB)
CW class-AB	860	28	0.1	100	≥8.5	≥55	≤1

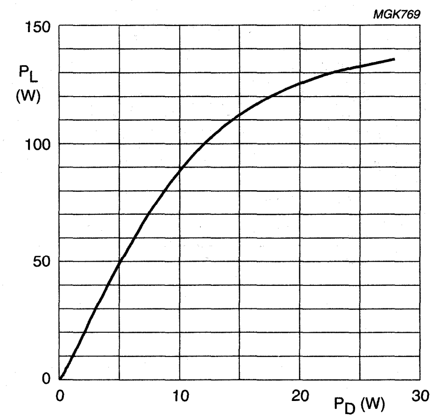
Ruggedness in class-AB operation

The BLV861 is capable of withstanding a load mismatch corresponding to VSWR = 3 : 1 through all phases under the conditions: T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.1 A; P_L = 100 W; $R_{th\ mb\text{-}h}$ = 0.2 K/W.



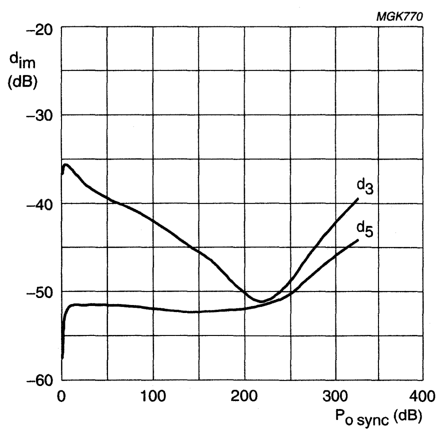
T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.1 A.

Fig.3 Power gain and collector efficiency as functions of load power; typical values.



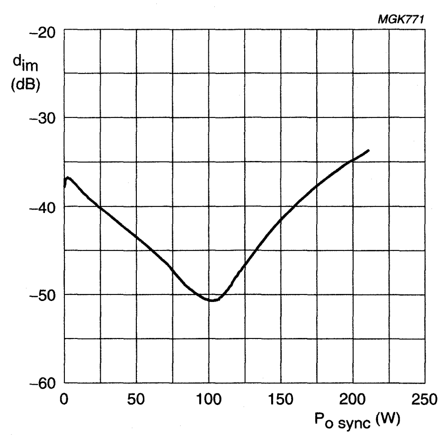
T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.1 A.

Fig.4 Load power as a function of drive power; typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.1 A;
2-tone:
f_{vision} = 855.25 MHz (−8 dB);
$f_{sideband}$ = 859.68 MHz (−16 dB).

Fig.5 Intermodulation distortion as a function of output power; typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.1 A;
3-tone:
f_{vision} = 855.25 MHz (−8 dB);
$f_{sideband}$ = 859.68 MHz (−16 dB);
f_{sound} = 860.75 MHz (−10 dB).

Fig.6 Intermodulation distortion as a function of output power; typical values.

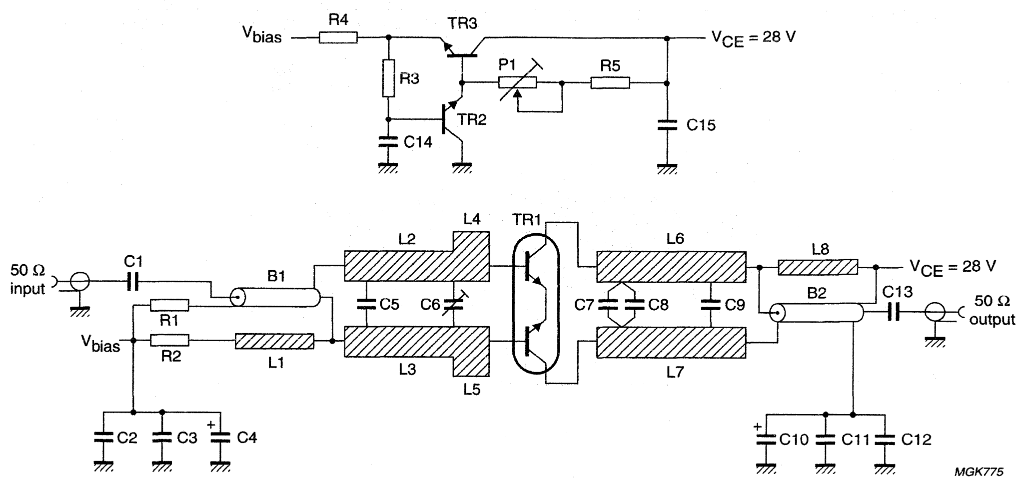
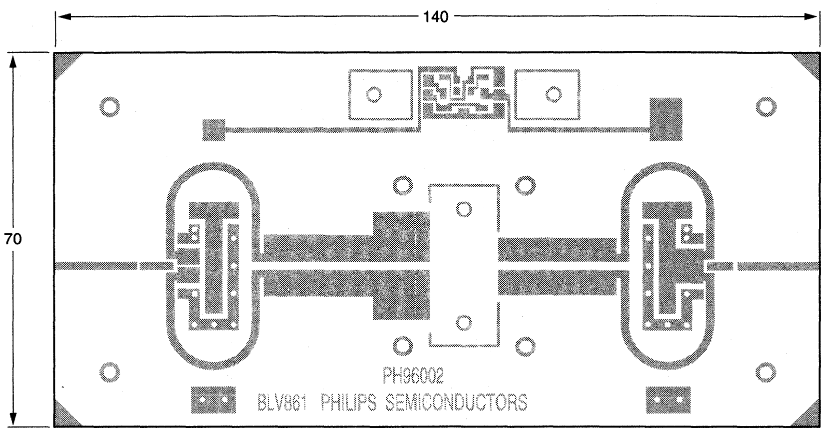
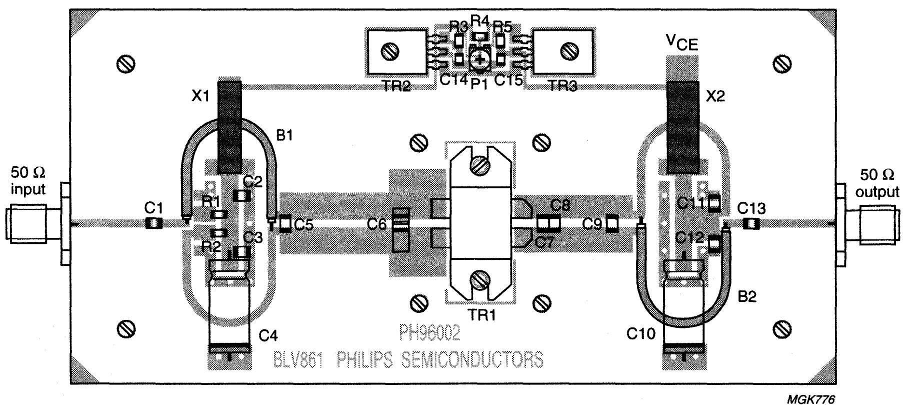


Fig.7 Class-AB test circuit at 860 MHz.





Dimensions in mm.

The components are situated on one side of the copper-clad PTFE-glass board (TLX8) from Taconic, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

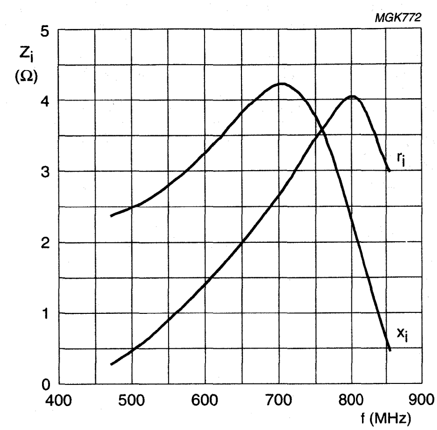
Fig.8 Printed-circuit board and component layout for the 860 MHz class-AB test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C13	multilayer ceramic chip capacitor; note 1	15 pF		
C2, C11, C15	multilayer ceramic chip capacitor	15 nF	0805	2222 590 16629
C3, C12	multilayer ceramic chip capacitor	100 nF	1206	2222 581 16641
C4, C10	solid aluminium capacitor	100 μF; 40 V		2222 031 37101
C5	multilayer ceramic chip capacitor; note 2	8.2 pF		
C6	multilayer ceramic chip capacitor + Tekelek trimmer; note 2	10 pF; 0.6 to 4.5 pF		
C7	multilayer ceramic chip capacitor; note 3	10 pF		
C8	multilayer ceramic chip capacitor; note 3	2.7 pF		
C9	multilayer ceramic chip capacitor; note 2	3 pF		
C14	multilayer ceramic chip capacitor; note 1	100 nF		
L1, L8	stripline; note 4		46 × 1.8 mm	
L2, L3	stripline; note 4		20 × 5 mm	
L4, L5	stripline; note 4		10 × 10 mm	
L6, L7	stripline; note 4		21 × 5 mm	
B1	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	46 mm	
B2	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	46 mm	
R1, R2, R4	SMD resistor	1 Ω	0805	2122 118 04562
R3	SMD resistor	47 Ω	0805	2122 118 04598
R5	SMD resistor	1.2 kΩ	0805	2122 118 04579
P1	potentiometer	4.7 kΩ		
X1, X2	copper ribbon hairpin			
TR1	NPN push-pull RF transistor BLV861			9340 542 40112
TR2, TR3	NPN transistor BD139			9330 912 20112

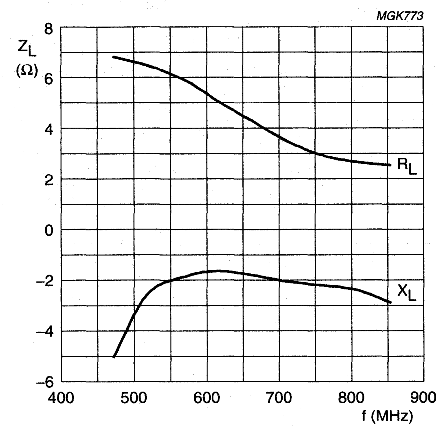
Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board: PTFE-glass material (TLX8) from Taconic (ε_r = 2.55); thickness 0.5 mm.



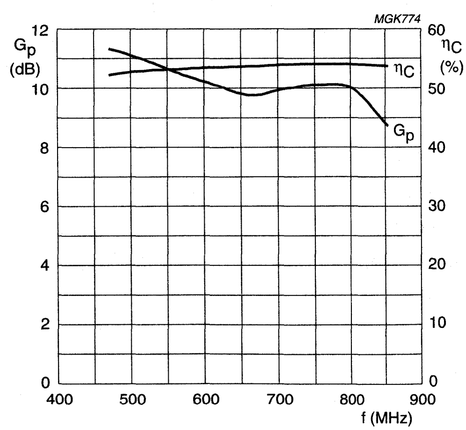
T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.1 A; P_L = 100 W (total device).

Fig.9 Input impedance (per section) as a function of frequency (series components); typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.1 A; P_L = 100 W (total device).

Fig.10 Load impedance (per section) as a function of frequency (series components); typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.1 A; P_L = 100 W (total device).

Fig.11 Power gain and collector efficiency as functions of frequency; typical values.

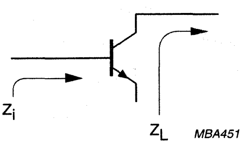


Fig.12 Definition of transistor impedance.

UHF linear push-pull power transistor BLV862

FEATURES

- Double stage internal input and output matching networks for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Common emitter class-AB operation in output stages in bands 4 and 5 (470 to 860 MHz) television transmitter amplifiers (vision or sound).

DESCRIPTION

NPN silicon planar epitaxial transistor with two sections in push-pull configuration. The device is encapsulated in a SOT262B 4-lead rectangular flange package, with two ceramic caps.

PINNING

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1; note 1
2	c2	collector 2; note 1
3	b1	base 1
4	b2	base 2
5	e	common emitter; note 2

Notes

1. Collectors 1 and 2 are connected together internally.
2. Common emitters are connected to the flange.

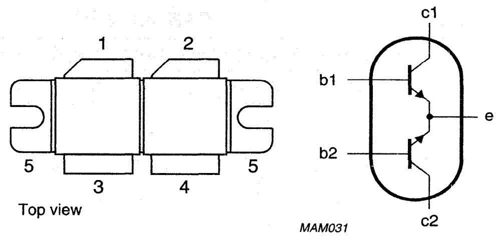


Fig.1 Simplified outline (SOT262B) and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	ΔG_p (dB)
CW class-AB	860	28	150	≥8 typ. 9	≥45 typ. 52	≤1

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

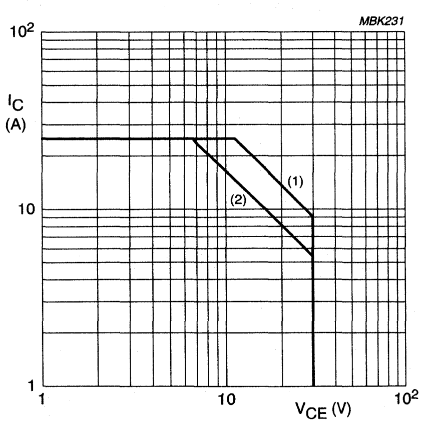
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	25	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	350	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 350 W; note 1	0.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.15	K/W

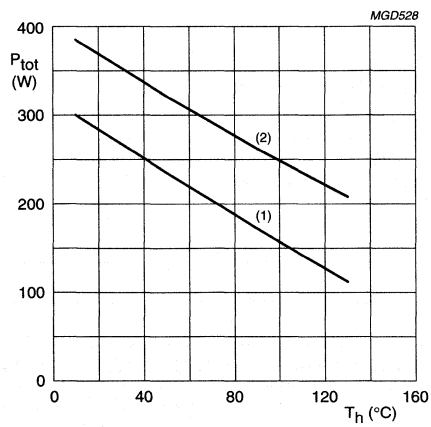
Note

1. Thermal resistance is determined under specified RF operating conditions.



Total device; both sections equally loaded.
(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.



Total device; both sections equally loaded.
(1) Continuous operation.
(2) Short time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

Values apply to either transistor section; T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_E = 0; I_C = 60 mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_B = 0; I_C = 150 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 3 mA; I_C = 0	3	–	–	V
I_{CBO}	collector-base leakage current	V_{CB} = 28 V	–	–	5	mA
h_{FE}	DC current gain	I_C = 4.5 A; V_{CE} = 10 V	30	–	140	–
Δh_{FE}	DC current gain ratio of both sections	I_C = 4.5 A; V_{CE} = 10 V	0.67	–	1.5	–
C_c	collector capacitance	$I_E = i_e$= 0; V_{CE} = 28 V; f = 1 MHz; note 1	–	75	–	pF

Note

1. The value of C_c is that of the die only, it is not measurable because of the internal matching network.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull class-AB test circuit; note 1.

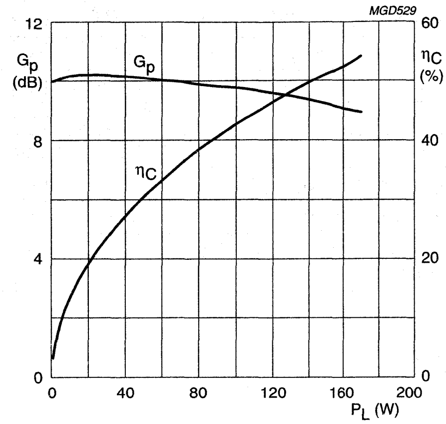
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	P_L (W)	G_p (dB)	η_C (%)	ΔG_p (dB)
CW class-AB	860	28	0.8	150	≥8 typ. 9	≥45 typ. 52	≤1

Note

1. See application note *"AN98014 in handbook SC19b."*

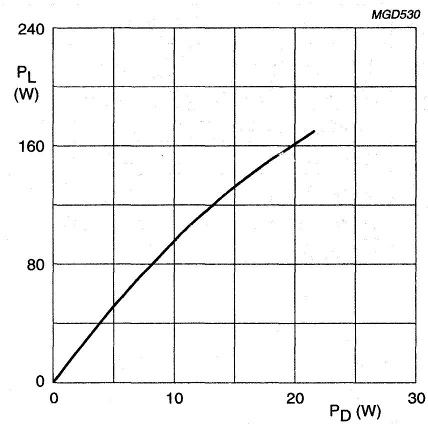
Ruggedness in class-AB operation

The BLV862 is capable of withstanding a load mismatch corresponding to VSWR = 2 : 1 through all phases under the conditions: T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W; $R_{th\ mb-h}$ = 0.15 K/W.



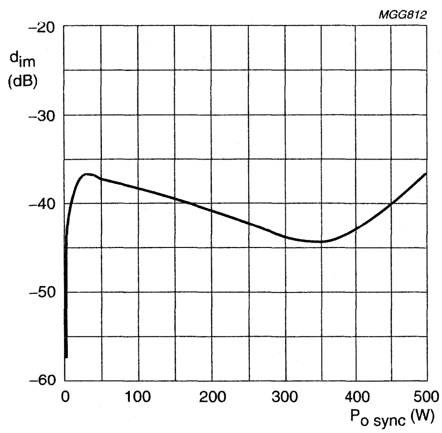
T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.8 A.

Fig.4 Power gain and collector efficiency as functions of load power; typical values.



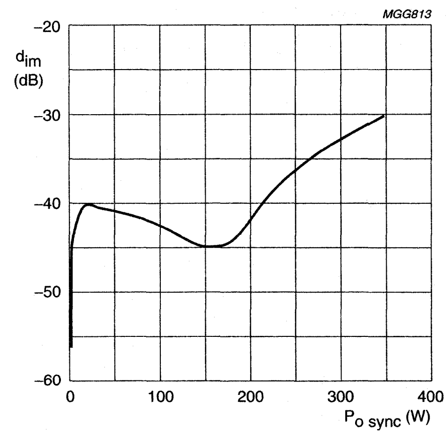
T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.8 A.

Fig.5 Load power as a function of drive power; typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A;
2-tone: f_{vision} = 855.25 MHz (-8 dB); $f_{sideband}$ = 859.68 MHz (-16 dB).

Fig.6 Intermodulation distortion as a function of output power; typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A;
3-tone: f_{vision} = 855.25 MHz (-8 dB); $f_{sideband}$ = 859.68 MHz (-16 dB);
f_{sound} = 860.75 MHz (-10 dB).

Fig.7 Intermodulation distortion as a function of output power; typical values.

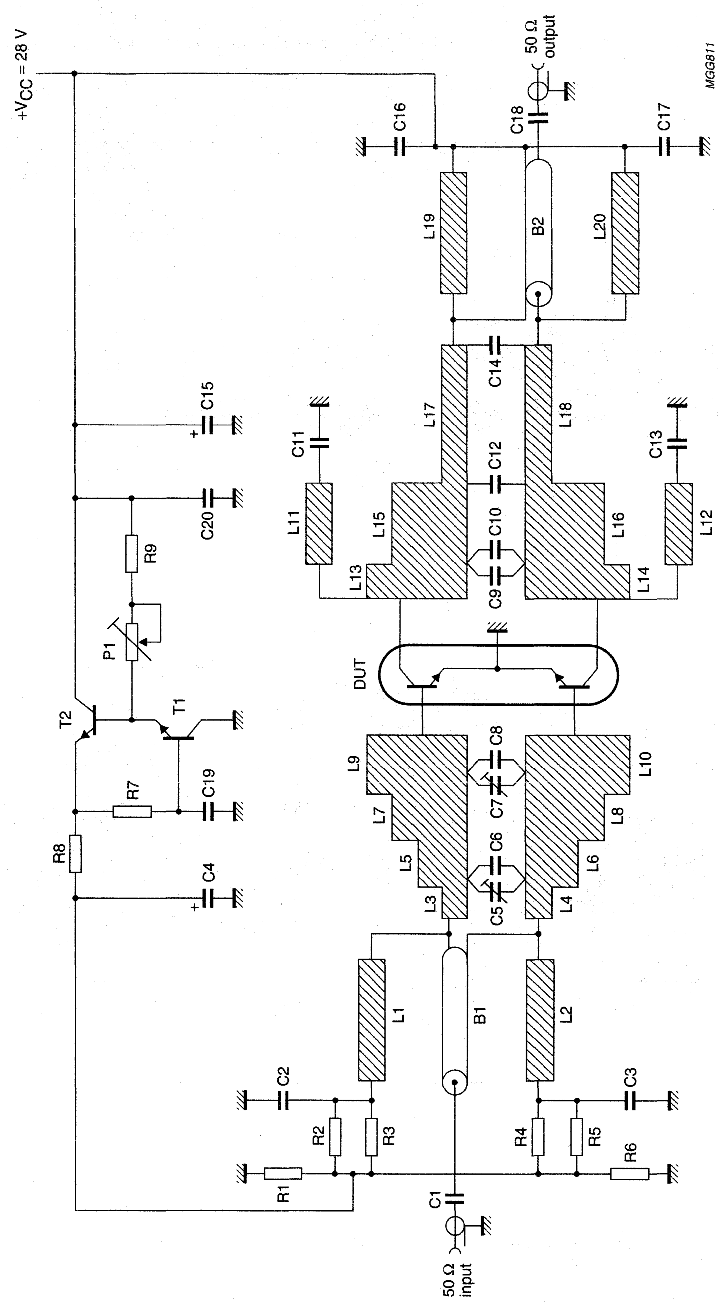
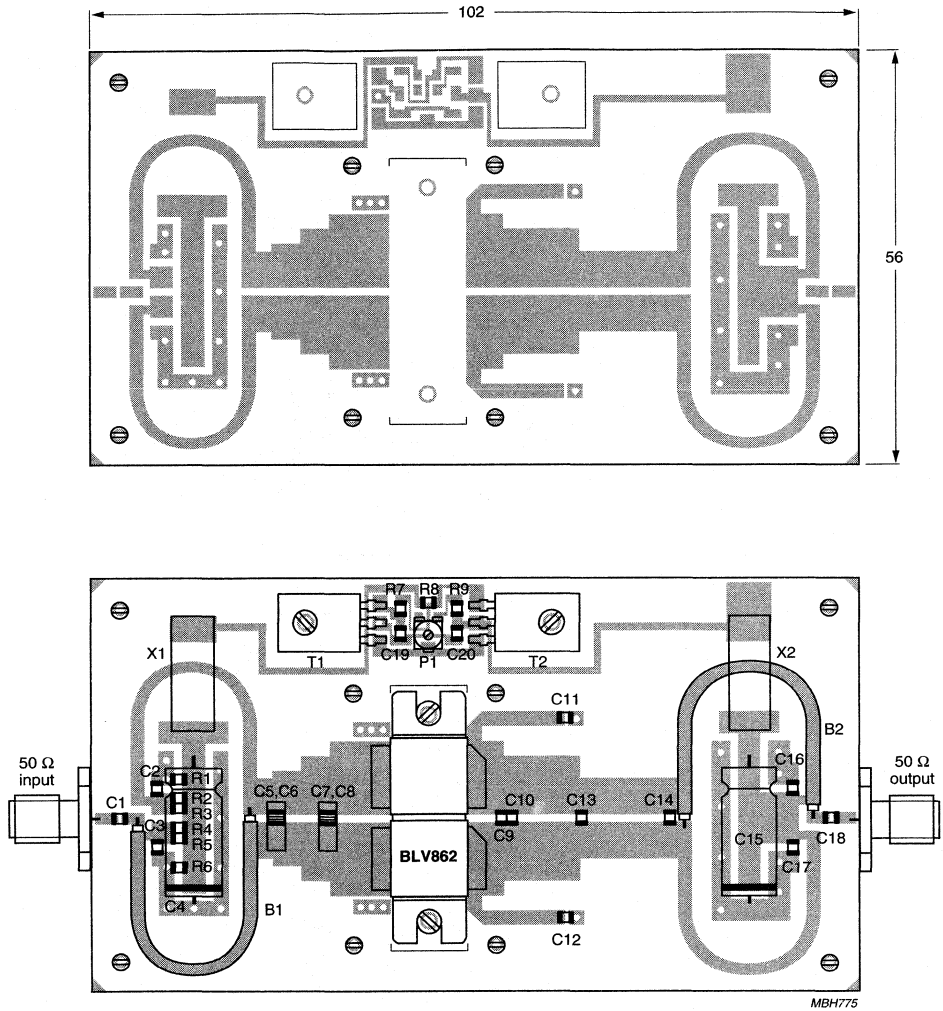


Fig.8 Class-AB test circuit at f = 860 MHz.



Dimensions in mm.

The components are situated on one side of the copper-clad PTFE-glass board (TLX8) from Taconic, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

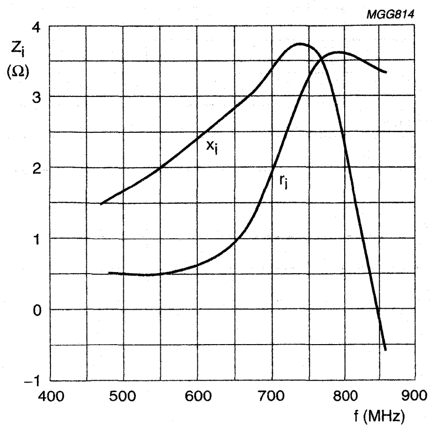
Fig.9 Printed-circuit board and component lay-out for the 860 MHz class-AB test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1	multilayer ceramic chip capacitor; note 1	10 pF		
C2. C3	multilayer ceramic chip capacitor	1 nF		2222 852 47102
C4	solid aluminium capacitor	220 µF; 16 V		2222 031 35221
C5, C7	Tekelec trimmer	1 to 5 pF		
C6, C8	multilayer ceramic chip capacitor; note 2	6.8 pF		
C9, C10	multilayer ceramic chip capacitor; note 3	10 pF		
C11, C13	multilayer ceramic chip capacitor; note 1	100 pF		
C12	multilayer ceramic chip capacitor; note 1	8.2 pF		
C14	multilayer ceramic chip capacitor; note 2	3.9 pF		
C15	solid aluminium capacitor	100 µF; 40 V		2222 031 37101
C16, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C18	multilayer ceramic chip capacitor; note 1	22 pF		
C19	multilayer ceramic chip capacitor; note 1	100 pF		
C20	multilayer ceramic chip capacitor	15 nF		2222 852 47153
L1, L2	stripline; note 4		47 × 1.8 mm	
L3, L4	stripline; note 4		2 × 5 mm	
L5, L6	stripline; note 4		4 × 6 mm	
L7, L8	stripline; note 4		4 × 8 mm	
L9, L10	stripline; note 4		8.1 × 10 mm	
L11, L12	stripline; note 4		15 × 2 mm	
L13, L14	stripline; note 4		5 × 10 mm	
L15, L16	stripline; note 4		10 × 8 mm	
L17, L18	stripline; note 4		12.9 × 5 mm	
L19, L20	stripline; note 4		48.7 × 1.8 mm	
B1	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	47 mm	
B2	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	48.7 mm	
R1, R6	SMD resistor	100 Ω	0805	2122 118 03881
R2, R3, R4, R5, R8	SMD resistor	1 Ω	0805	2122 118 04562
R7	SMD resistor	47 Ω	0805	2122 118 04598
R9	SMD resistor	1.2 kΩ	0805	2122 118 04579
P1	potentiometer	4.7 kΩ		
X1, X2	copper ribbon hairpin			
T1, T2	NPN transistor	BD139		9330 912 20112

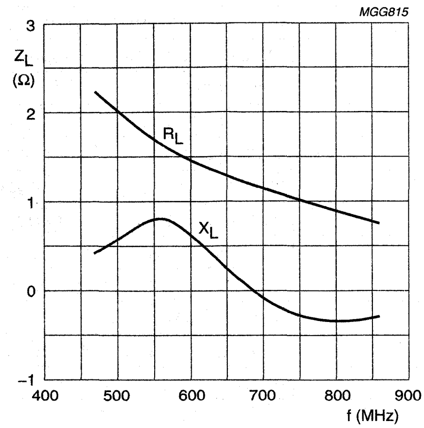
Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board: PTFE-glass material (TLX8) from Taconic (ε_r = 2.55); thickness 0.5 mm.



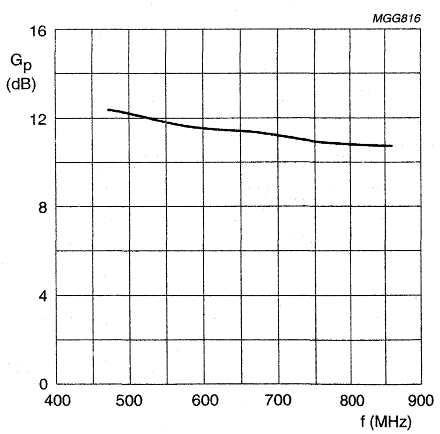
T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W (total device).

Fig.10 Input impedance (per section) as function of frequency (series components); typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W (total device).

Fig.11 Load impedance (per section) as function of frequency (series components); typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W (total device).

Fig.12 Power gain as a function of frequency; typical values.

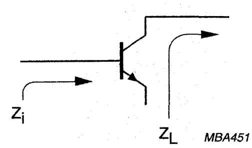


Fig.13 Definition of transistor impedance.

UHF power transistor BLV904

FEATURES

- Emitter ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability
- Internal input matching to achieve high power gain and easy design of wideband circuits.

APPLICATIONS

- Common emitter class-AB operation in base stations in the 820 to 960 MHz frequency range.

DESCRIPTION

NPN silicon planar epitaxial power transistor in an 8-lead SOT409B SMD package with ceramic cap.
All leads are isolated from the mounting base.

PINNING - SOT409B

PIN	DESCRIPTION
1, 4, 5, 8	emitter
2, 3	base
6, 7	collector

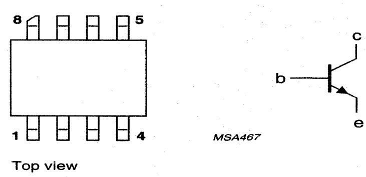


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	960	26	5	≥13	≥50	–
2-tone, class-AB	f_1 = 960; f_2 = 960.1	26	5 (PEP)	typ. 15.5	typ. 40	typ. –30

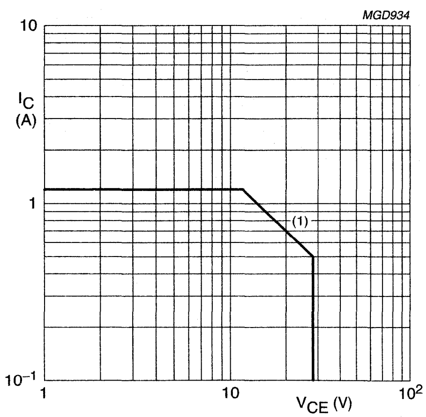
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current (DC)		–	1.2	A
$I_{C(AV)}$	collector current (average)		–	1.2	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; note 1	–	17	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

Note

1. Transistor with metallized ground plane mounted on a printed-circuit board, see *"Mounting and soldering recommendations in the General part of handbook SC19a"*.



(1) T_s = 60 °C.

Fig.2 DC SOAR.

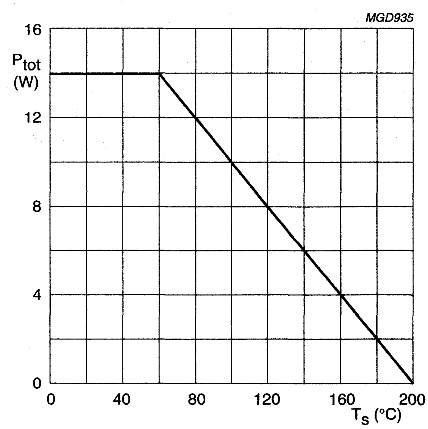


Fig.3 Total power dissipation as a function of the soldering point temperature.

UHF power transistor BLV904

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 17 W; T_{mb} = 25 °C; note 1	10	K/W

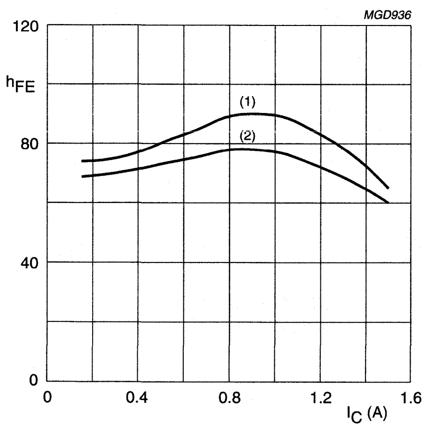
Note

1. Transistor with metallized ground plane mounted on a printed-circuit board, see *"Mounting and soldering recommendations in the General part of handbook SC19a"*.

CHARACTERISTICS

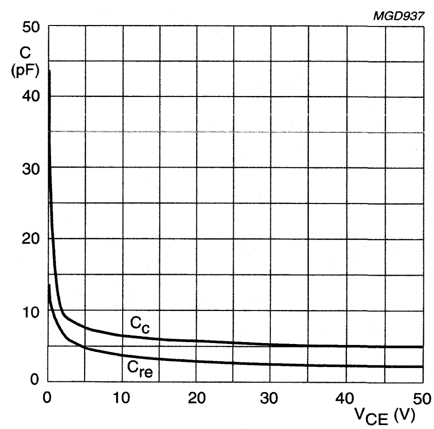
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 5 mA	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 10 mA	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.5 mA	4	–	–	V
I_{CES}	collector leakage current	V_{CE} = 26 V; V_{BE} = 0	–	–	1.3	mA
h_{FE}	DC current gain	V_{CE} = 26 V; I_C = 600 mA	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; I_E = i_e = 0; f = 1 MHz	–	6	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	2.5	–	pF



(1) V_{CE} = 26 V; t_p = 500 μs; δ = < 1 %.
(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.



f = 1 MHz.

Fig.5 Capacitance as a function of collector-emitter voltage; typical values.

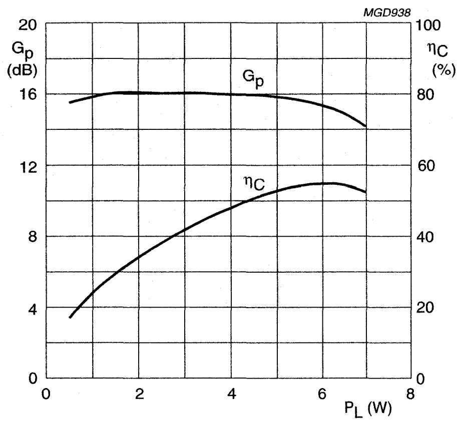
APPLICATION INFORMATION

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	960	26	15	5	≥13 typ. 15.5	≥50 typ. 55	–
2-tone, class-AB	f_1 = 960; f_2 = 960.1	26	15	5 (PEP)	typ. 15.5	typ. 40	typ. –30

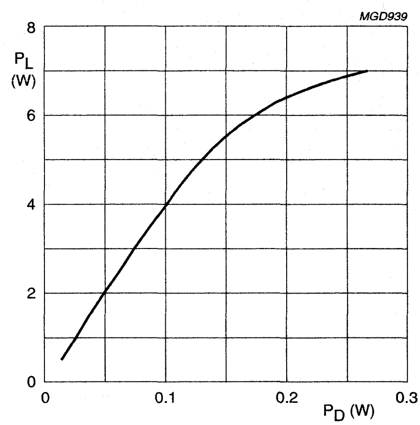
Ruggedness in class-AB operation

The BLV904 is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: f = 960 MHz; V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 5 W; T_{mb} = 25 °C.



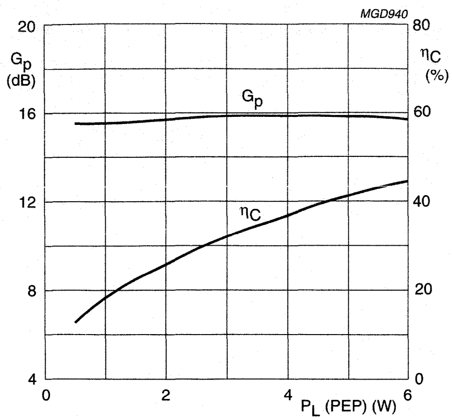
CW, class-AB; V_{CE} = 26 V; I_{CQ} = 15 mA; f = 960 MHz; T_{mb} = 25 °C.

Fig.6 Power gain and collector efficiency as functions of load power; typical values.



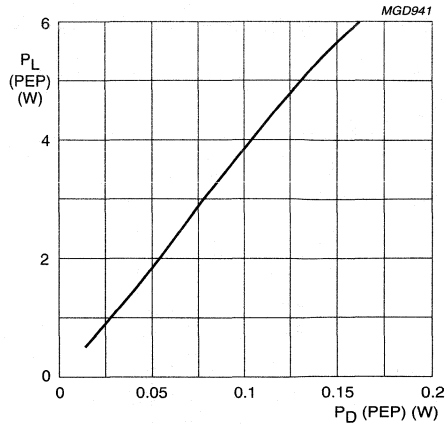
CW, class-AB; V_{CE} = 26 V; I_{CQ} = 15 mA; f = 960 MHz; T_{mb} = 25 °C.

Fig.7 Load power as a function of drive power; typical values.



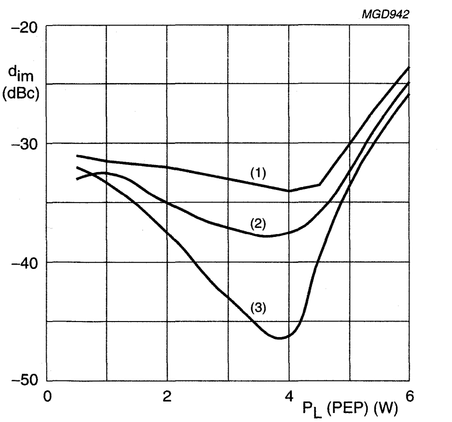
V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 960 MHz; f_2 = 960.1 MHz.

Fig.8 Power gain and collector efficiency as functions of peak envelope load power; typical values.



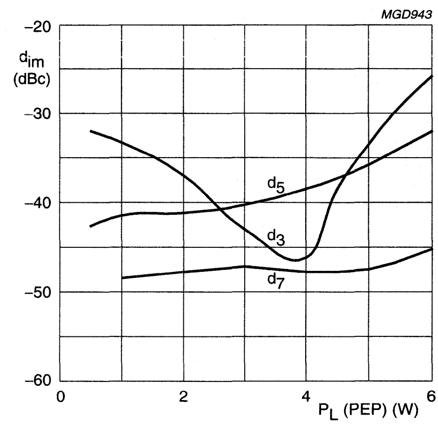
V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 960 MHz; f_2 = 960.1 MHz.

Fig.9 Peak envelope load power as a function of peak envelope drive power; typical values.



V_{CE} = 26 V; f_1 = 960 MHz; f_2 = 960.1 MHz.
(1) I_{CQ} = 15 mA. (2) I_{CQ} = 40 mA. (3) I_{CQ} = 60 mA.

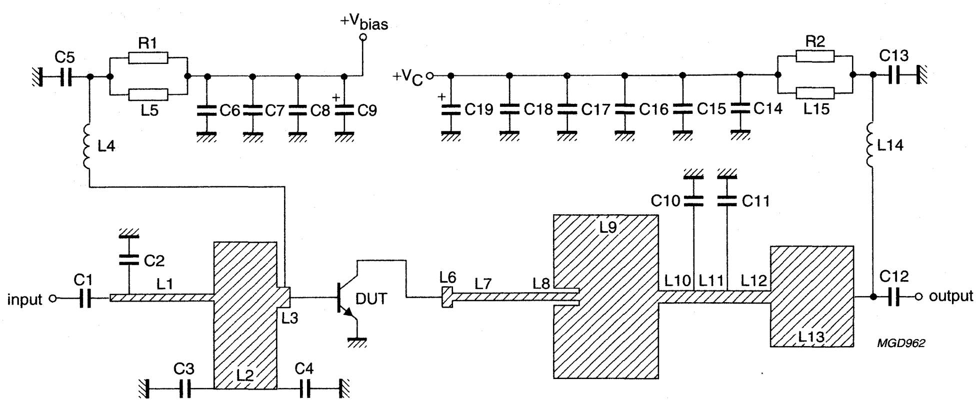
Fig.10 Third order intermodulation distortion as a function of peak envelope load power; typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 960 MHz; f_2 = 960.1 MHz.

Fig.11 Intermodulation distortion as a function of peak envelope load power; typical values.

Test circuit information



f = 960 MHz.

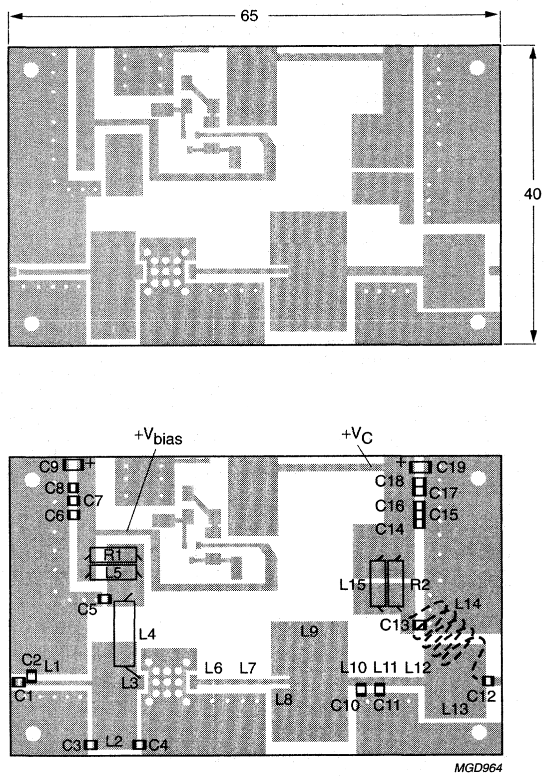
Fig.12 Class-AB test circuit.

List of components (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C12	multilayer ceramic chip capacitor; note 1	24 pF		
C2	multilayer ceramic chip capacitor; note 1	3.3 pF		
C3	multilayer ceramic chip capacitor, note 1	2.2 pF		
C4	multilayer ceramic chip capacitor; note 1	1.6 pF		
C5, C6, C13, C18	multilayer ceramic chip capacitor; note 2	200 pF		
C7, C17	multilayer ceramic chip capacitor; note 2	110 pF		
C8, C14, C15, C16	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C9, C19	tantalum SMD capacitor	10 μF; 35 V		
C10	multilayer ceramic chip capacitor; note 1	1.8 pF		
C11	multilayer ceramic chip capacitor; note 1	13 pF		
L1	stripline; note 3	50 Ω	8.2 × 0.65 mm	
L2	stripline; note 3	4.9 Ω	6 × 14 mm	
L3, L6	stripline; note 3	24.5 Ω	1.5 × 2 mm	
L4	RF-choke	0.22 μH		
L5, L15	grade 4S2 ferroxcube chip-bead			4330 030 36301
L7	stripline; note 3	46.3 Ω	12.22 × 0.7 mm	
L8	stripline; notes 3 and 4	4.3 Ω	7.58 × 16.1 mm	
L9	stripline; note 3	4.3 Ω	10 × 16.1 mm	
L10	stripline; note 3	34.3 Ω	1.9 × 1.2 mm	
L11	stripline; note 3	34.3 Ω	3.2 × 1.2 mm	
L12	stripline; note 3	34.3 Ω	4.8 × 1.2 mm	
L13	stripline; note 3	6.7 Ω	8 × 9.9 mm	
L14	5 turns enamelled 1 mm copper wire			
R1	metal film resistor	100 Ω; 0.4 W		
DUT	transistor	BLV904		

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with epoxy fibreglass dielectric ($\varepsilon_r = 10.2$); thickness 0.64 mm.
4. Not connected over total length; only 7.58 mm connected.

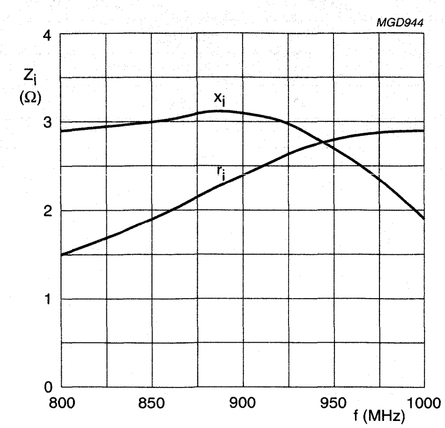


Dimensions in mm.

f = 960 MHz.

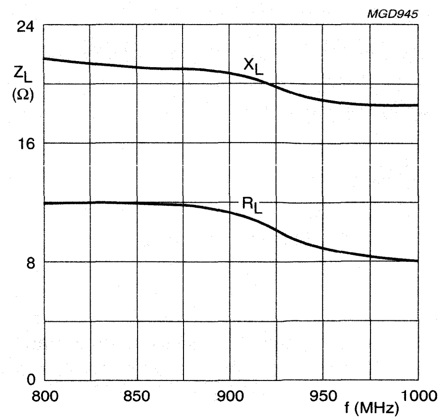
The components are situated on one side of the copper-clad epoxy fibreglass board, the other side is not etched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.13 Component layout for class-AB test circuit.



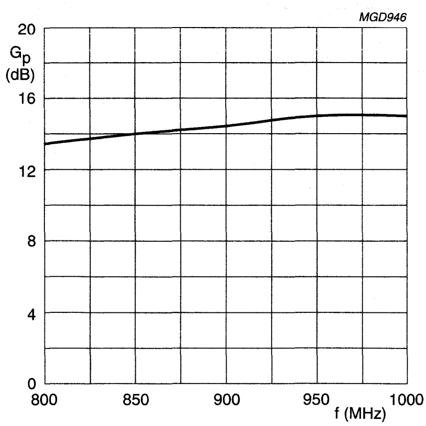
V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 5 W; T_{mb} = 25 °C.

Fig.14 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 5 W; T_{mb} = 25 °C.

Fig.15 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 5 W; T_{mb} = 25 °C.

Fig.16 Power gain as a function of frequency; typical values.

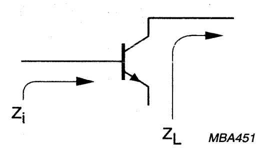


Fig.17 Definition of transistor impedance.

MOUNTING RECOMMENDATIONS

Heat from the device is transferred via the leads and the metallized underside. For optimum heat transfer it is recommended that the transistor be mounted on a grounded metallized area on the component side of the printed-circuit board. This metallized area should contain a large number of metallized, solder-filled through-holes. The non-component side of the printed-circuit board forms a ground plane. When the printed-circuit board is mounted on the heatsink using heatsink compound, a thermal resistance from mounting base to heatsink of 0.9 K/W can be attained.

UHF power transistor BLV909

FEATURES

- Emitter ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability
- Internal input matching to achieve high power gain and easy design of wideband circuits.

APPLICATIONS

- Common emitter class-AB operation in base stations in the 820 to 960 MHz frequency range.

DESCRIPTION

NPN silicon planar epitaxial transistor in an 8-lead SOT409B SMD package with a ceramic cap. All leads are isolated from the mounting base.

PINNING - SOT409B

PIN	SYMBOL	DESCRIPTION
1, 4, 5, 8	e	emitter
2, 3	b	base
6, 7	c	collector

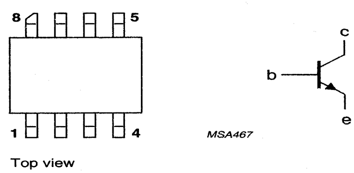


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	960	26	9	≥9.5	≥50	–
2-tone, class-AB	f_1 = 960; f_2 = 960.1	26	9 (PEP)	≥9.5	≥35	typ. –30

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

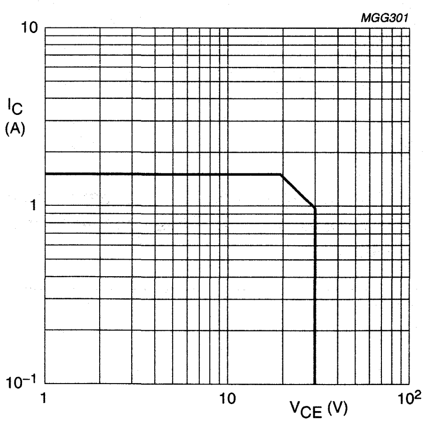
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	70	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	1.5	A
$I_{C(AV)}$	average collector current		–	1.5	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; note 1	–	29	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 29 W; T_{mb} = 25 °C; note 1	6	K/W

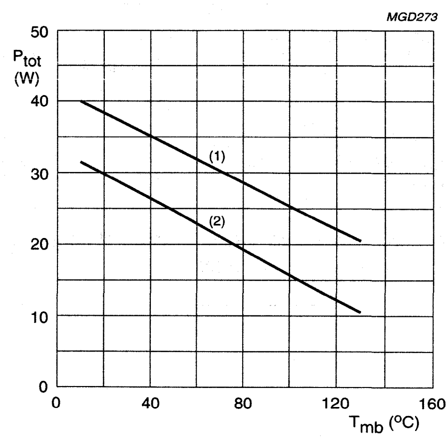
Note to the Limiting values and Thermal characteristics

1. Transistor with metallized ground plane mounted on a printed-circuit board, see *"Mounting and soldering section, Handbook SC19a."*



T_{mb} = 25 °C.

Fig.2 DC SOAR.



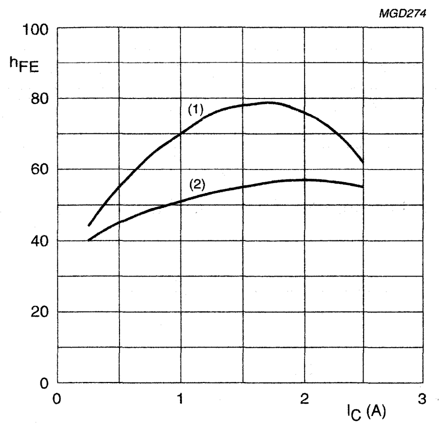
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power derating curves.

CHARACTERISTICS

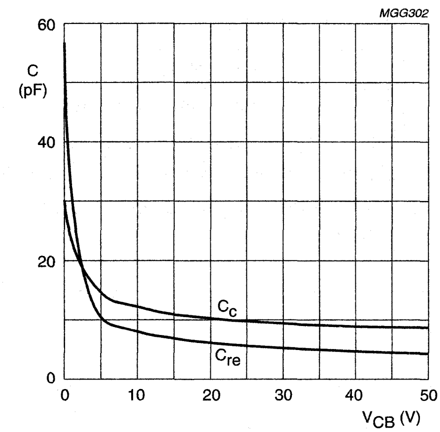
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 5 mA	70	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 15 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.3 mA	3	–	–	V
I_{CES}	collector leakage current	V_{CE} = 28 V; V_{BE} = 0	–	–	0.75	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 500 mA	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; $I_E = i_e$ = 0; f = 1 MHz	–	10	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	6	–	pF



(1) V_{CE} = 26 V; t_p = 500 µs; $\delta \leq 1$ %.
(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.



f = 1 MHz.

Fig.5 Collector and feedback capacitance as a function of collector-base voltage; typical values.

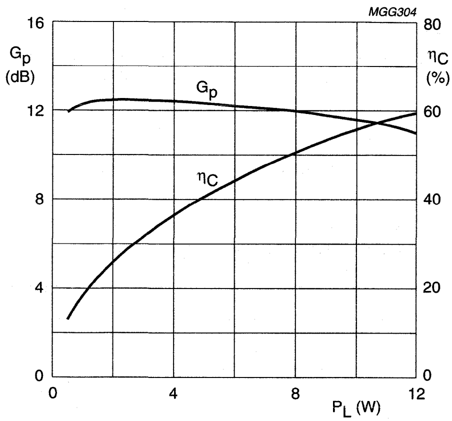
APPLICATION INFORMATION

RF performance at T_{mb} = 25 °C in a common emitter test circuit (see Figs 12 and 13).

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	960	26	25	9	≥9.5, typ. 11.5	≥50, typ. 55	–
2-tone, class-AB	f_1 = 960; f_2 = 960.1	26	25	9 (PEP)	≥9.5, typ. 11.5	≥35, typ. 40	typ. –30

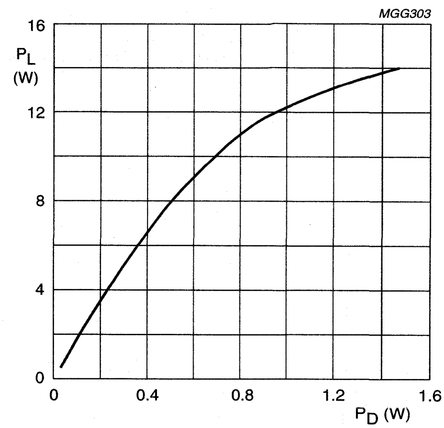
Ruggedness in class-AB operation

The BLV909 is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: f = 960 MHz; V_{CE} = 26 V; I_{CQ} = 25 mA; T_{mb} = 25 °C.



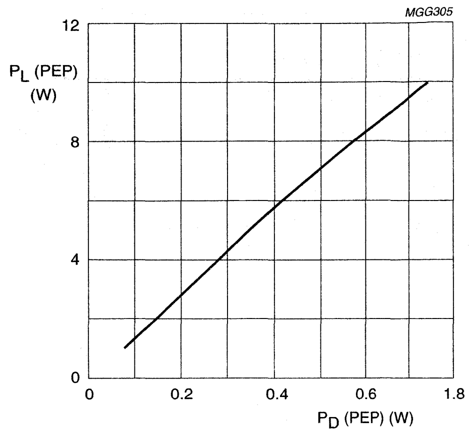
V_{CE} = 26 V; I_{CQ} = 25 mA; f = 960 MHz.

Fig.6 Power gain and collector efficiency as functions of load power; typical values.



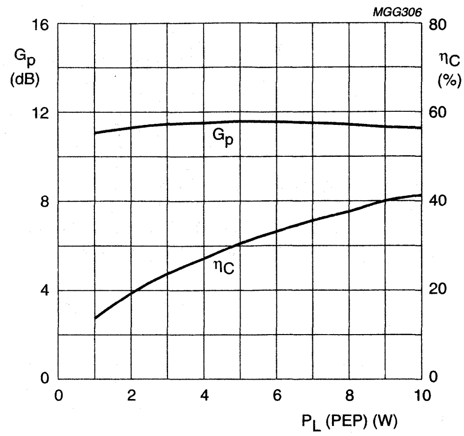
V_{CE} = 26 V; I_{CQ} = 25 mA; f = 960 MHz.

Fig.7 Load power as a function of drive power; typical values.



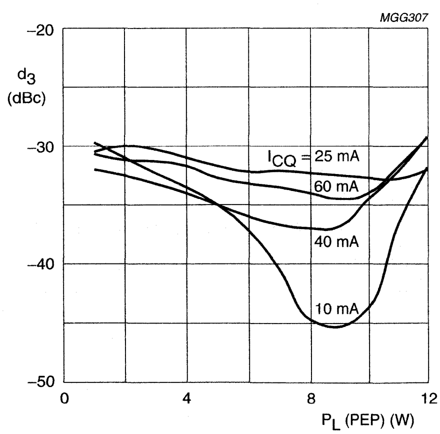
V_{CE} = 26 V; I_{CQ} = 25 mA; f_1 = 960 MHz; f_2 = 960.1 MHz.

Fig.8 Peak envelope load power as a function of drive power; typical values.



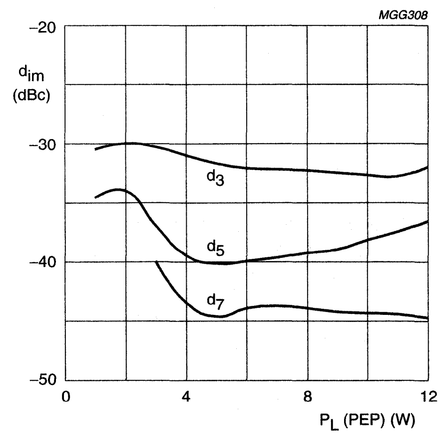
V_{CE} = 26 V; I_{CQ} = 25 mA; f_1 = 960 MHz; f_2 = 960.1 MHz.

Fig.9 Power gain and efficiency as functions of peak envelope load power; typical values.



V_{CE} = 26 V; f_1 = 960 MHz; f_2 = 960.1 MHz.

Fig.10 Third order intermodulation distortion as a function of peak envelope load power; typical values.



V_{CE} = 26 V; I_{CQ} = 25 mA; f_1 = 960 MHz; f_2 = 960.1 MHz.

Fig.11 Intermodulation distortion as a function of peak envelope load power; typical values.

Test circuit information

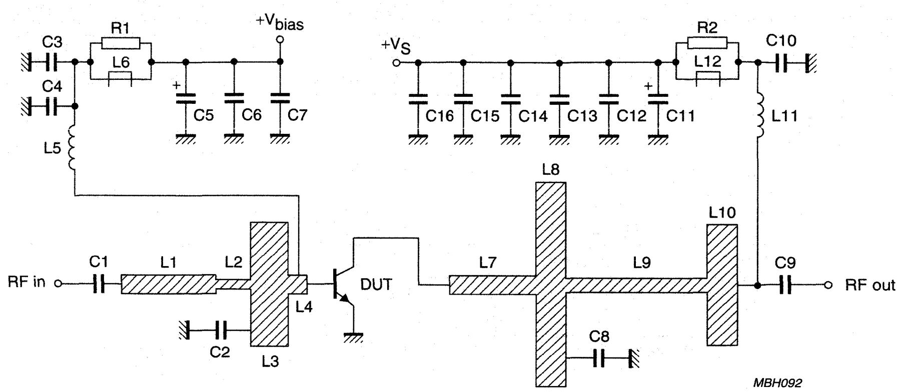


Fig.12 Common emitter test circuit for class-AB operation at 900-960 MHz.

Mounting recommendations

Both the metallized rear side and the leads of the device contribute to the heat flow. For the best results, it is recommended to mount the transistor on a grounded metallized area on the printed-circuit board, which is equipped with a large number of through metallized holes filled with solder.

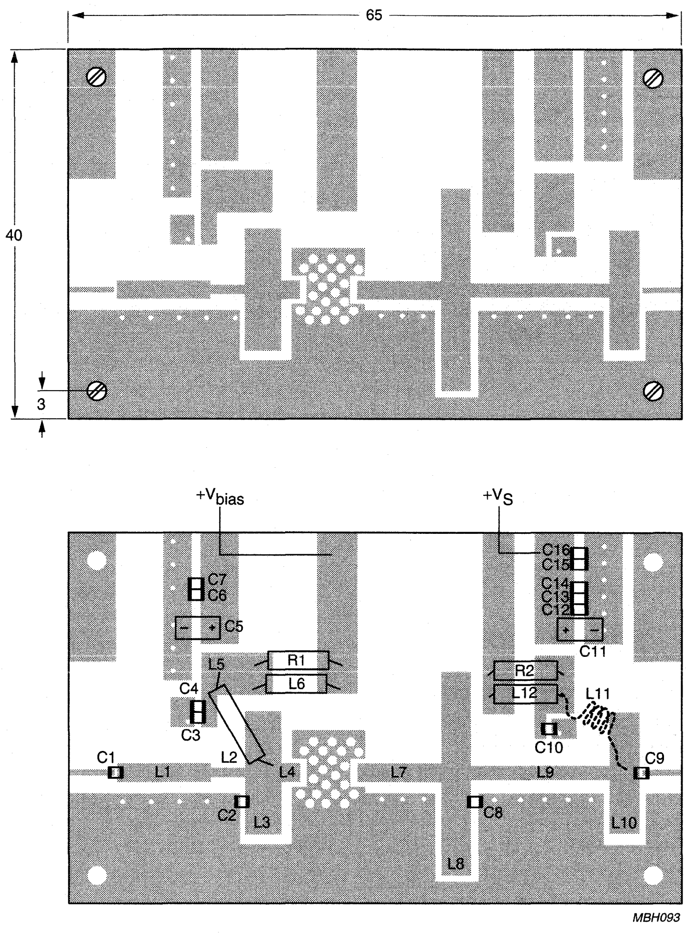
When the heatsink is mounted to the rear side of the printed-circuit board by means of heatsink compound, a thermal resistance between the mounting base and the heatsink of 0.9 K/W can be achieved.

List of components used in test circuit (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C9	multilayer ceramic chip capacitor; note 1	24 pF		
C2	multilayer ceramic chip capacitor; notes 1 and 2	5.6 pF		
C3, C7, C10, C16	multilayer ceramic chip capacitor; note 3	110 pF		
C4, C15	multilayer ceramic chip capacitor; note 3	200 pF		
C5, C11	tantalum SMD capacitor	10 μF, 35 V		
C6, C12, C13, C14	ceramic chip capacitor	100 nF		2222 852 47104
C8	multilayer ceramic chip capacitor; note 1	8.2 pF		
L1	stripline; note 4	24.3 Ω	length 9.85 mm width 2 mm	
L2	stripline; note 4	37.5 Ω	length 3.63 mm width 1 mm	
L3	stripline; note 4	5.11 Ω	length 4.1 mm width 13.3 mm	
L4	stripline; note 4	24.3 Ω	length 2 mm width 2 mm	
L5	RF choke	0.22 μH		
L6, L12	grade 4S2 ferroxcube chip-bead			
L7	stripline; note 4	24.3 Ω	length 9.2 mm width 2 mm	
L8	stripline; note 4	3.2 Ω	length 3.1 mm width 22 mm	
L9	stripline; note 4	29.4 Ω	length 14.4 mm width 1.5 mm	
L10	stripline; note 4	5.22 Ω	length 3.2 mm width 13 mm	
L11	5 turns enamelled 1 mm copper wire	35 nH	pitch 1.23 mm int. dia. 3.2 mm	
R1, R2	metal film resistor	100 Ω, 0.4 W		

Notes

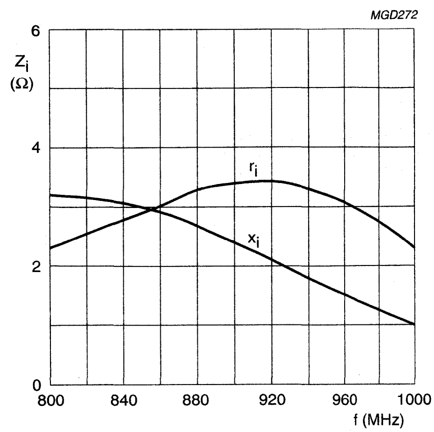
1. American Technical Ceramics type 100A or capacitor of same quality.
2. For operation at 820 to 900 MHz: C2 = 6.2 pF.
3. American Technical Ceramics type 100B or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board, with PTFE fibre-glass dielectric (ε_r = 10.2); thickness 0.64 mm.



Dimensions in mm.

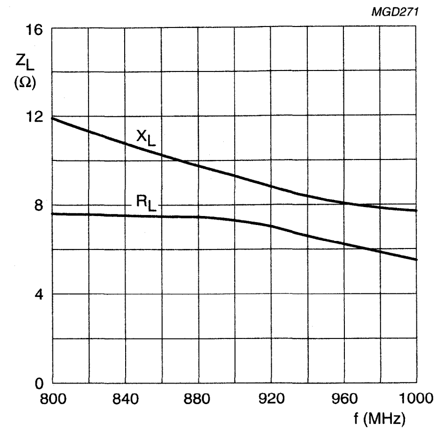
The components are situated on one side of the copper-clad PCB, the other side is unetched and serves as a ground plane.
Earth connections from the component side to the ground plane are made by through metallization.

Fig.13 Component layout and printed-circuit board and component lay-out for 900 to 960 MHz class-AB test circuit.



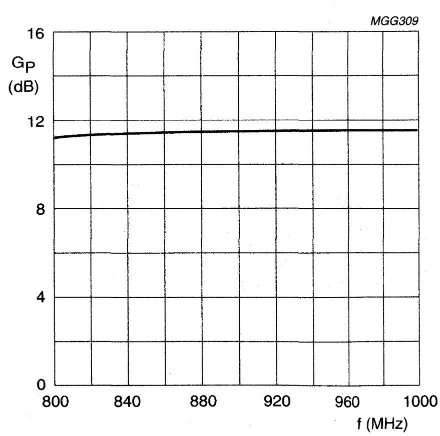
V_{CE} = 26 V; I_{CQ} = 25 mA; P_L = 9 W; T_{mb} = 25 °C.

Fig.14 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 25 mA; P_L = 9 W; T_{mb} = 25 °C.

Fig.15 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 25 mA; P_L = 9 W; T_{mb} = 25 °C.

Fig.16 Power gain as a function of frequency; typical values.

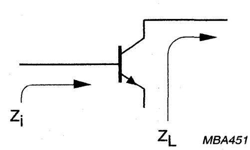


Fig.17 Definition of transistor impedance.

UHF power transistor BLV910

FEATURES

- Internal input matching to achieve high power gain and easy design of wideband circuits
- Emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Base station transmitters in the 820 to 960 MHz range.

PINNING - SOT171

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	b	base
4	c	collector
5	e	emitter
6	e	emitter

DESCRIPTION

NPN silicon planar epitaxial transistor intended for common emitter class-AB operation. The transistor is encapsulated in a 6-lead SOT171 flange envelope with a ceramic cap. All leads are isolated from the flange.

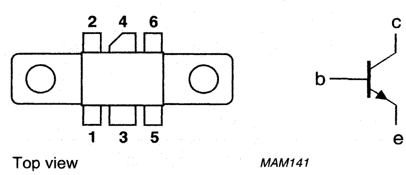


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	960	26	10	≥ 11	≥ 55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

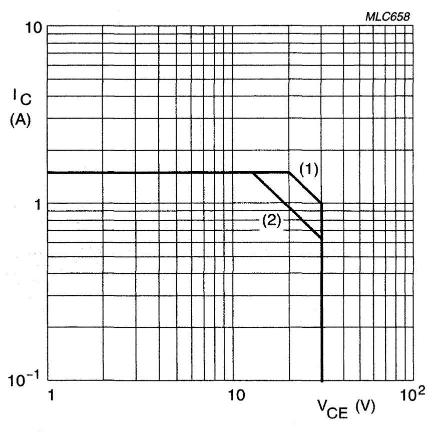
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	70	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	1.5	A
$I_{C(AV)}$	average collector current		–	1.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	30	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

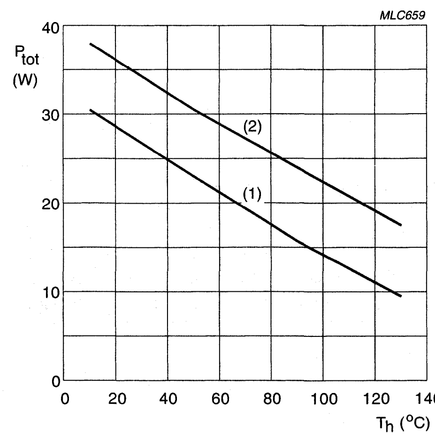
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 30 W; T_{mb} = 25 °C	5.85	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W



(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.



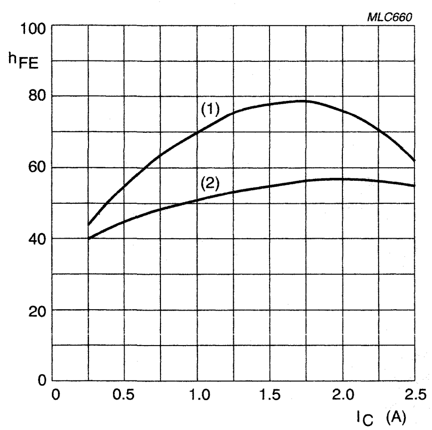
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

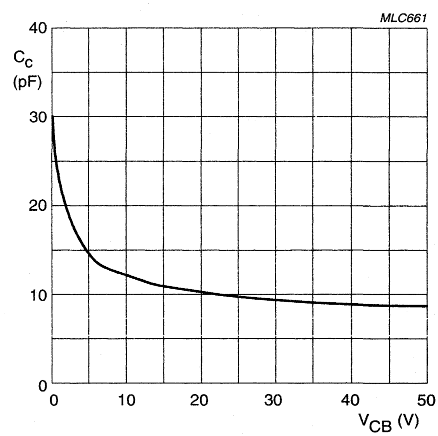
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 5 mA	70	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 15 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.3 mA	3	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0; V_{CE} = 28 V	–	–	0.75	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 0.5 A;	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; I_E = i_e = 0; f = 1 MHz	–	10	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	6	–	pF



(1) V_{CE} = 26 V: measured under pulsed conditions; $t_p \leq 500\ \mu s$; $\delta < 0.01$.

(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.



$I_E = i_e = 0$; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage; typical values.

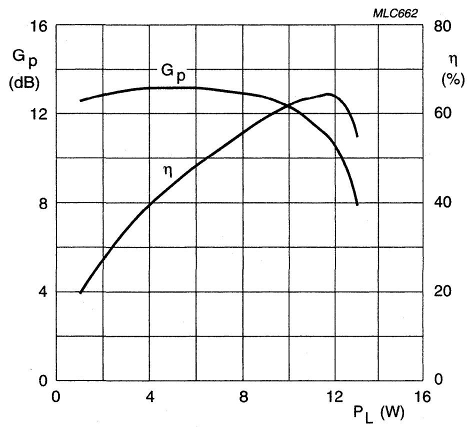
APPLICATION INFORMATION

RF performance at $T_h = 25$ °C in a common emitter, class-AB test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	960	26	25	10	≥11	≥55

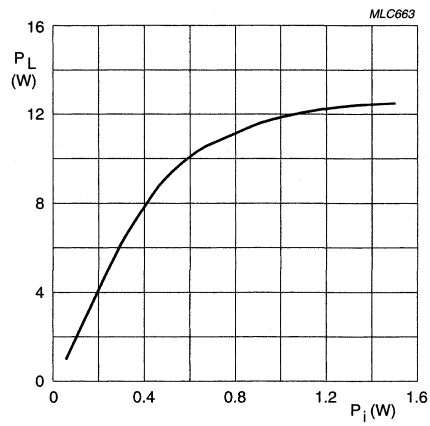
Ruggedness in class-AB operation

The BLV910 is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases at rated output power, under the following conditions: $V_{CE} = 26$ V; f = 960 MHz; $I_{CQ} = 25$ mA; $T_{mb} = 25$ °C.



$V_{CE} = 26$ V.
$I_{CQ} = 25$ mA.
f = 960 MHz.

Fig.6 Power gain and efficiency as functions of load power; typical values.



$V_{CE} = 26$ V.
$I_{CQ} = 25$ mA.
f = 960 MHz.

Fig.7 Load power as a function of input power; typical values.

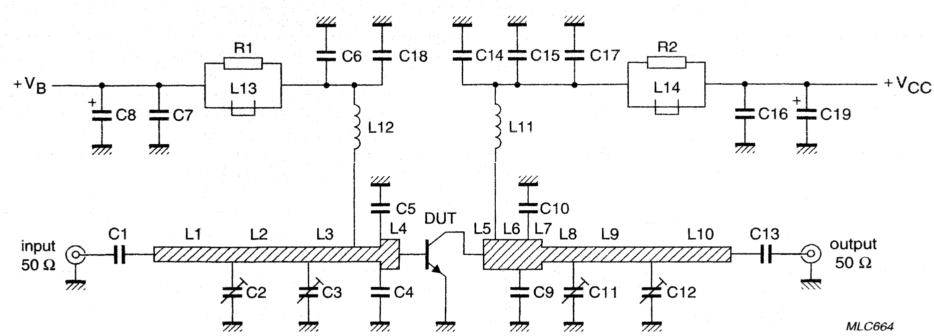


Fig.8 Class-AB test circuit at f = 960 MHz.

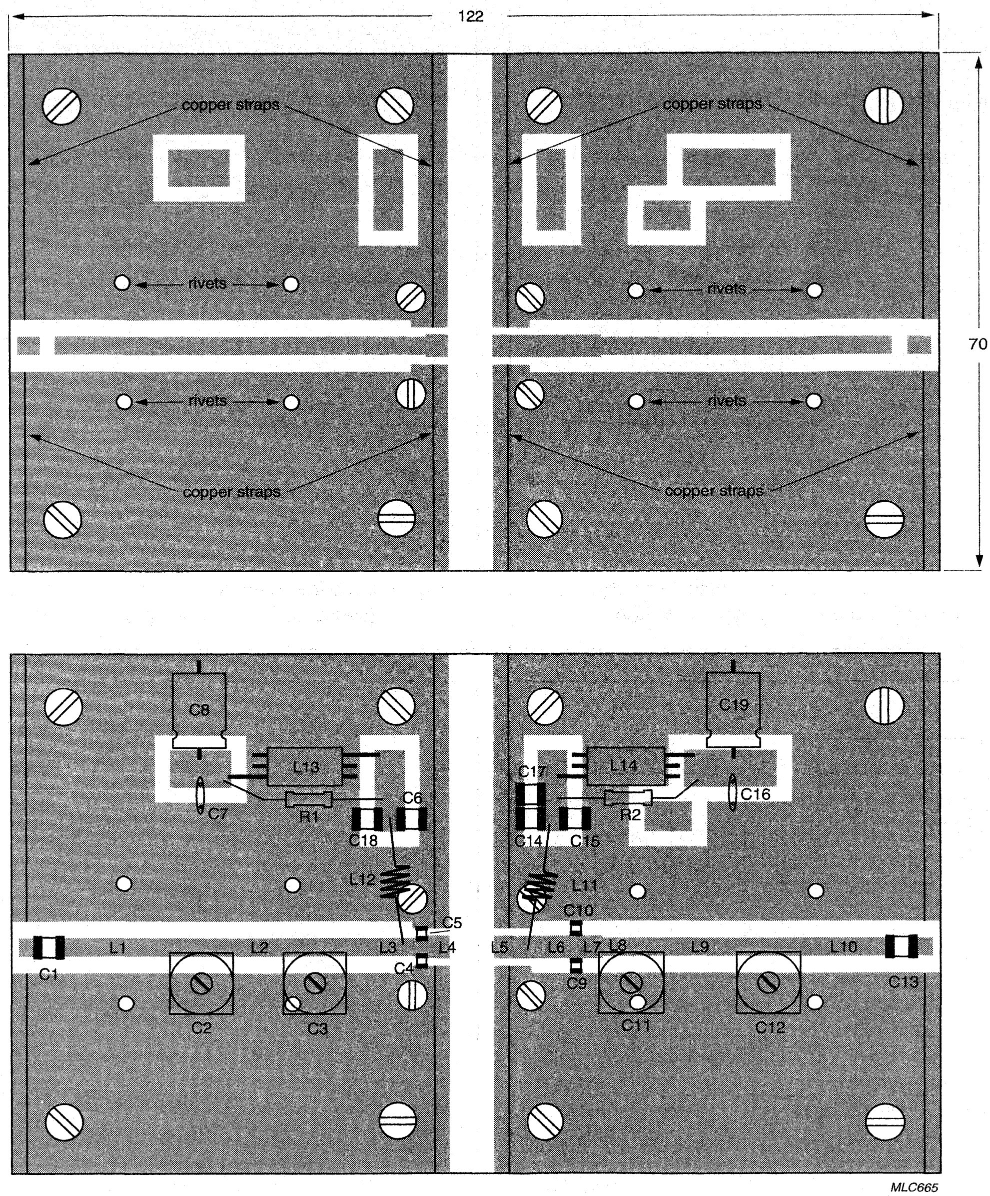
List of components (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C13	multilayer ceramic chip capacitor; note 1	43 pF		
C2, C3, C11, C12	film dielectric trimmer	1.4 pF to 5.5 pF		2222 809 09001
C4, C5	multilayer ceramic chip capacitor; note 2	10 pF		
C6	multilayer ceramic chip capacitor; note 1	150 pF		
C7, C16	ceramic capacitor	22 nF		2222 640 08223
C8, C19	solid aluminium capacitor	10 μF, 63 V		2222 030 38109
C14	multilayer ceramic chip capacitor; note 1	20 pF		
C9, C10	multilayer ceramic chip capacitor; note 2	8.2 pF		
C17	multilayer ceramic chip capacitor; note 1	220 pF		
C15, C18	multilayer ceramic chip capacitor; note 1	62 pF		
L1	stripline; note 3	50 Ω	length 17 mm width 2.4 mm	
L2, L3	stripline; note 3	50 Ω	length 14 mm width 2.4 mm	
L4	stripline; note 3	43 Ω	length 4 mm width 3 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
L5, L6	stripline; note 3	43 Ω	length 3 mm width 3 mm	
L7	stripline; note 3	43 Ω	length 3.4 mm width 3 mm	
L8	stripline; note 3	50 Ω	length 6.3 mm width 2.4 mm	
L9	stripline; note 3	50 Ω	length 18 mm width 2.4 mm	
L10	stripline; note 3	50 Ω	length 15 mm width 2.4 mm	
L11	4 turns enamelled 0.8 mm copper wire		int. diameter 4mm length 5 mm leads 2 × 5 mm	
L12	3 turns enamelled 0.8 mm copper wire		int. diameter 3mm length 5 mm leads 2 × 5 mm	
L13, L14	grade 3B Ferroxcube wideband RF choke			4312 020 36642
R1, R2	metal film resistor	10 Ω, 0.4 W		2322 151 71009

Notes

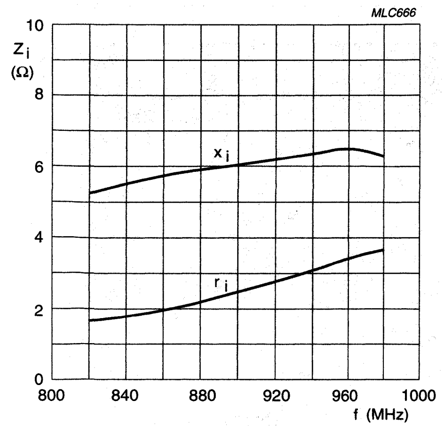
1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on double-clad PCB with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$); thickness $^1/_{32}$".



Dimensions in mm.

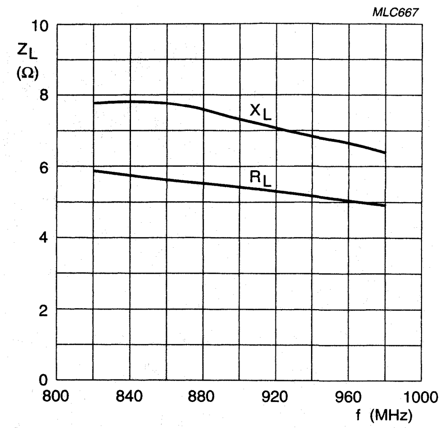
The components are located on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the emitters to provide a direct contact between the component side and the ground plane.

Fig.9 Component layout for 960 MHz class-AB test circuit.



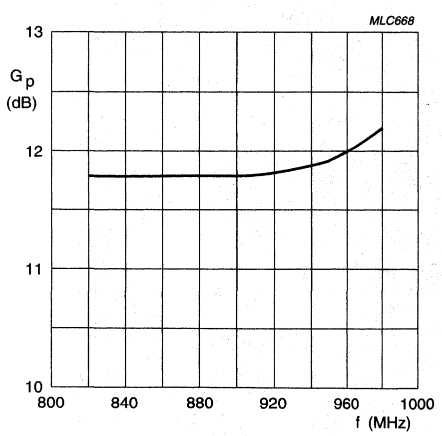
V_{CE} = 26 V.
I_{CQ} = 25 mA.
T_{mb} = 25 °C.
P_L = 10 W.

Fig.10 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V.
I_{CQ} = 25 mA.
T_{mb} = 25 °C.
P_L = 10 W.

Fig.11 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V.
I_{CQ} = 25 mA.
T_{mb} = 25 °C.
P_L = 10 W.

Fig.12 Power gain as a function of frequency; typical values.

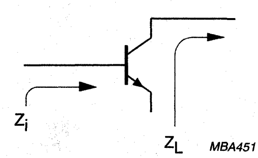


Fig.13 Definition of transistor impedance.

UHF power transistor | BLV920

FEATURES

- Internal input matching to achieve high power gain and easy design of wideband circuits
- Emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Base station transmitters in the 820 to 960 MHz range.

PINNING - SOT171A

PIN	SYMBOL	DESCRIPTION
1	e	emitter
2	e	emitter
3	b	base
4	c	collector
5	e	emitter
6	e	emitter

DESCRIPTION

NPN silicon planar epitaxial transistor intended for common emitter class-AB operation. The transistor is encapsulated in a 6-lead SOT171A flange envelope with a ceramic cap. All leads are isolated from the flange.

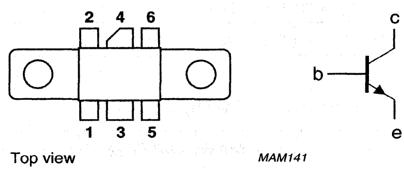


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	960	26	20	≥10	≥ 55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

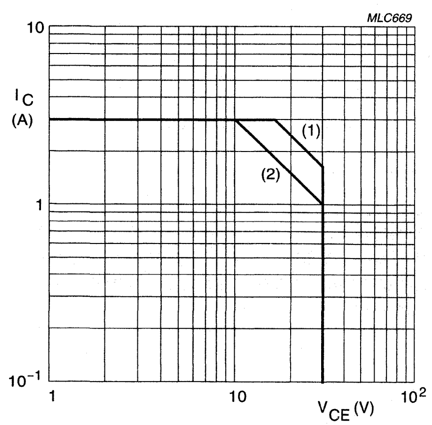
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	70	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	50	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	200	°C

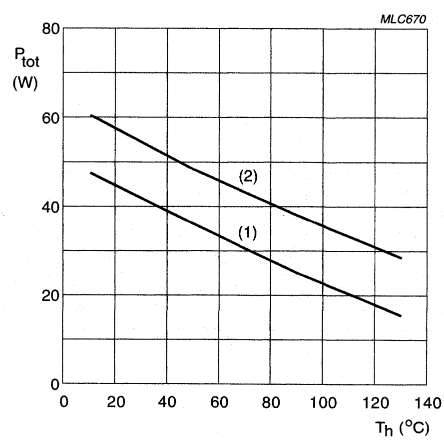
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 49 W; T_{mb} = 25 °C	3.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W



(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

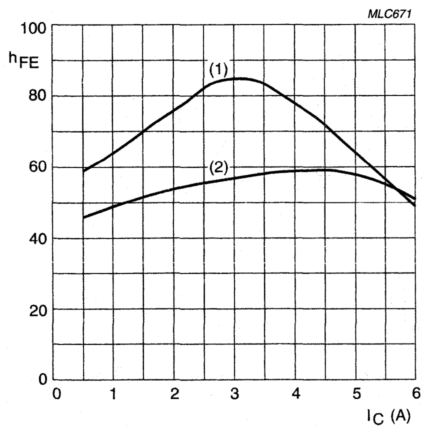
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 15 mA	70	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 30 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.6 mA	3	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0; V_{CE} = 28 V	–	–	1.5	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 1 A; note 1	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; I_E = i_e = 0; f = 1 MHz	–	17	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	11	–	pF

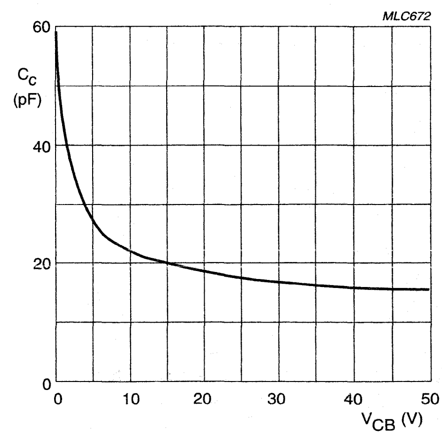
Note

1. Measured under pulsed conditions: $t_p \leq 500$ µs; $\delta \leq 0.01$.



Measured under pulsed conditions; $t_p \leq 500$ µs; $\delta \leq 0.01$.
(1) V_{CE} = 26 V.
(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.



I_E = i_e = 0; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage; typical values.

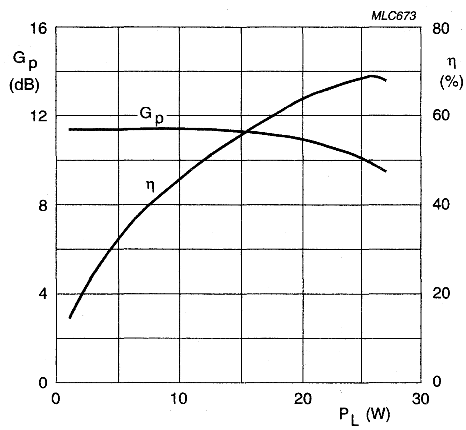
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter, class-AB test circuit; $R_{th\ mb\text{-}h}$ = 0.4 K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	960	26	50	20	≥10	≥55

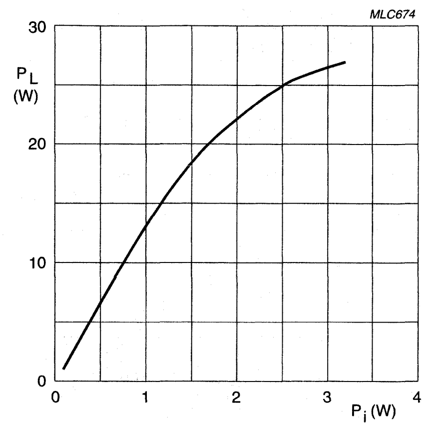
Ruggedness in class-AB operation

The BLV920 is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases at rated output power, under the following conditions: V_{CE} = 26 V; f = 960 MHz; I_{CQ} = 50 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W.



V_{CE} = 26 V.
I_{CQ} = 50 mA.
f = 960 MHz.

Fig.6 Power gain and efficiency as functions of load power; typical values.



V_{CE} = 26 V.
I_{CQ} = 50 mA.
f = 960 MHz.

Fig.7 Load power as a function of input power; typical values.

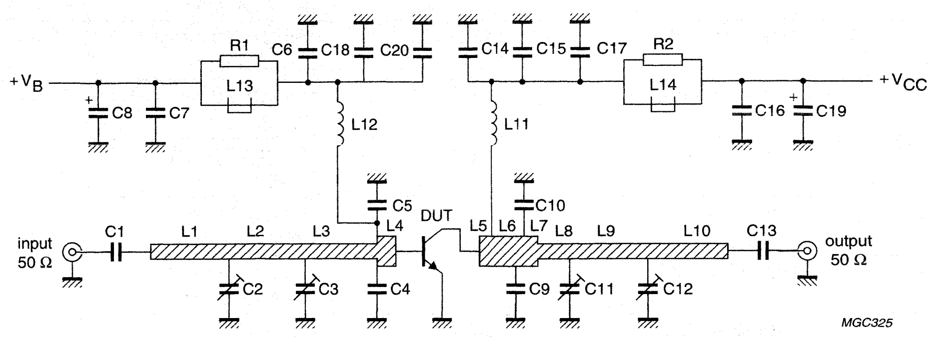


Fig.8 Class-AB test circuit at f = 960 MHz.

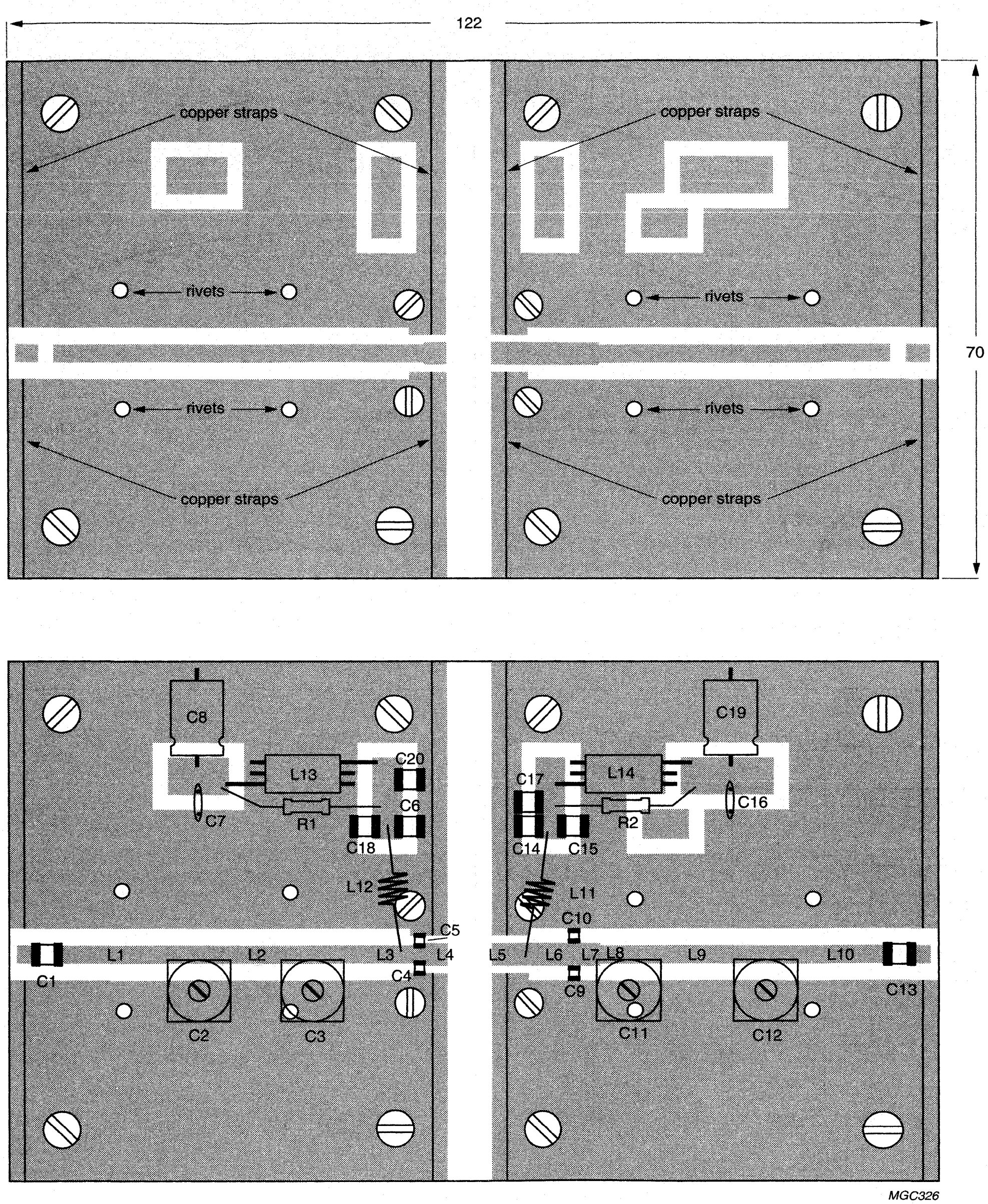
List of components (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C13	multilayer ceramic chip capacitor; note 1	43 pF		
C2, C3, C11, C12	film dielectric trimmer	1.4 pF to 5.5 pF		2222 809 09001
C4, C5	multilayer ceramic chip capacitor; note 2	10 pF		
C6, C17	multilayer ceramic chip capacitor; note 1	150 pF		
C7, C16	ceramic capacitor	22 nF		2222 640 08223
C8, C19	solid aluminium capacitor	10 μF, 63 V		2222 030 38109
C14	multilayer ceramic chip capacitor; note 1	20 pF		
C9, C10	multilayer ceramic chip capacitor; note 2	11 pF		
C20	multilayer ceramic chip capacitor; note 1	1 nF		
C15, C18	multilayer ceramic chip capacitor; note 1	62 pF		
L1	stripline; note 3	50 Ω	length 16.8 mm width 2.4 mm	
L2	stripline; note 3	50 Ω	length 14.8 mm width 2.4 mm	
L3	stripline; note 3	50 Ω	length 13.7 mm width 2.4 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
L4	stripline; note 3	43 Ω	length 3.5 mm width 3 mm	
L5	stripline; note 3	43 Ω	length 6.4 mm width 3 mm	
L6	stripline; note 3	43 Ω	length 5.8 mm width 3 mm	
L7	stripline; note 3	43 Ω	length 2.4 mm width 3 mm	
L8	stripline; note 3	50 Ω	length 3 mm width 2.4 mm	
L9	stripline; note 3	50 Ω	length 15.5 mm width 2.4 mm	
L10	stripline; note 3	50 Ω	length 20 mm width 2.4 mm	
L11	4 turns enamelled 0.8 mm copper wire	45 nH	int. diameter 4mm length 5 mm leads 2 × 5 mm	
L12	3 turns enamelled 0.8 mm copper wire	30 nH	int. diameter 3mm length 5 mm leads 2 × 5 mm	
L13, L14	grade 3B Ferroxcube wideband RF choke			4312 020 36642
R1, R2	metal film resistor	10 Ω, 0.4 W		2322 151 71009

Notes

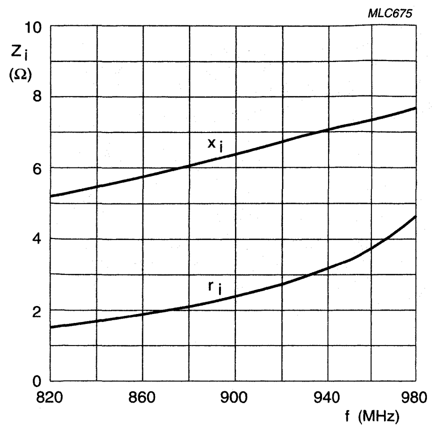
1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on double-clad PCB with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$); thickness $\frac{1}{32}$".



Dimensions in mm.

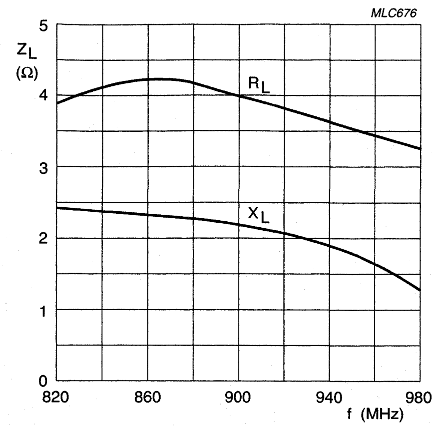
The components are located on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the emitters to provide a direct contact between the component side and the ground plane.

Fig.9 Component layout for 960 MHz class-AB test circuit.



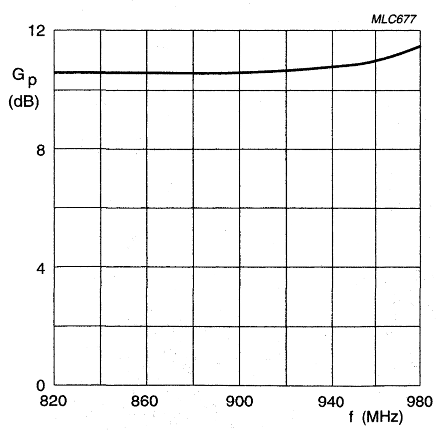
V_{CE} = 26 V; I_{CQ} = 50 mA; P_L = 20 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W.

Fig.10 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 50 mA; P_L = 20 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W.

Fig.11 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 50 mA; P_L = 20 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W.

Fig.12 Power gain as a function of frequency; typical values.

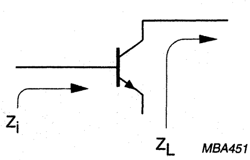


Fig.13 Definition of transistor impedance.

UHF power transistor BLV946

FEATURES

- Internal input and output matching for easy matching, high gain and efficiency
- Poly-silicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Base stations in the 850 to 960 MHz frequency range.

DESCRIPTION

NPN silicon planar transistor intended for common emitter class-AB operation. The transistor has internal input and output matching by means of MOS capacitors.
The encapsulation is a SOT273A flange envelope with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT273A

PIN	DESCRIPTION
1	emitter
2	emitter
3	collector
4	base
5	emitter
6	emitter

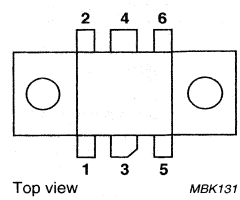


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	960	26	40	≥9	≥55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

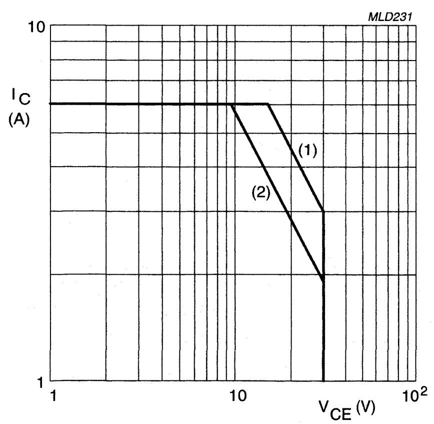
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	70	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	6	A
$I_{C(AV)}$	average collector current		–	6	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	90	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	operating junction temperature		–	+200	°C

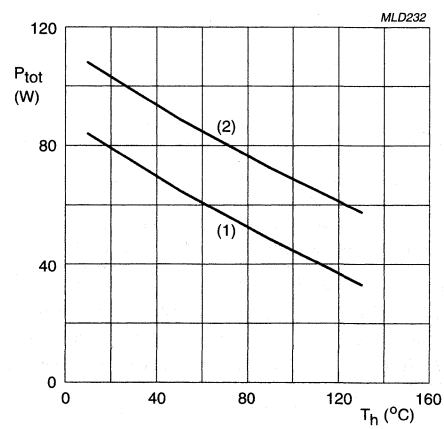
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 90 W; T_{mb} = 25 °C	1.94	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.3	K/W



(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curve.

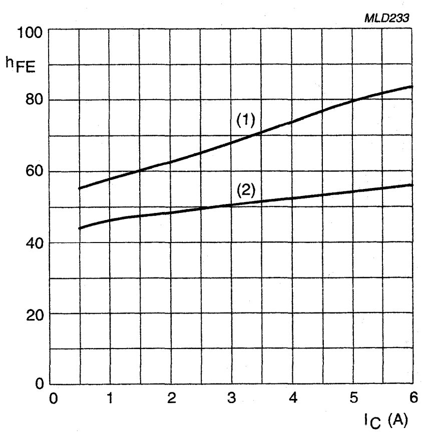
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 30 mA	70	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 60 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 1.2 mA	3	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0; V_{CE} = 28 V	–	–	3	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 2 A; note 1	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; I_E = i_e = 0; f = 1 MHz; note 2	–	33	–	pF

Notes

1. Measured under pulsed conditions: $t_p \leq 500$ µs; $\delta \leq 0.01$.
2. C_C value is that of the die only; it is not measurable because of internal matching network.



Measured under pulsed conditions; $t_p \leq 500$ µs; $\delta \leq 0.01$.
(1) V_{CE} = 26 V.
(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.

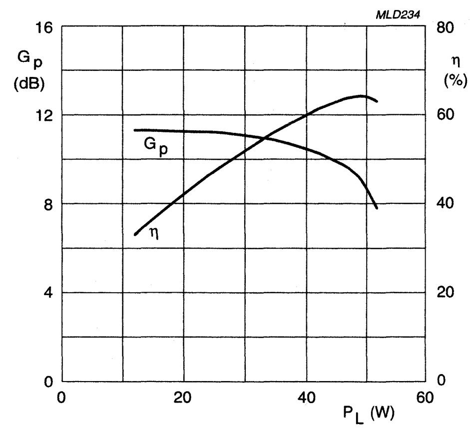
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter, class-AB test circuit; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	960	26	130	40	≥9 typ. 11	≥55 typ. 60

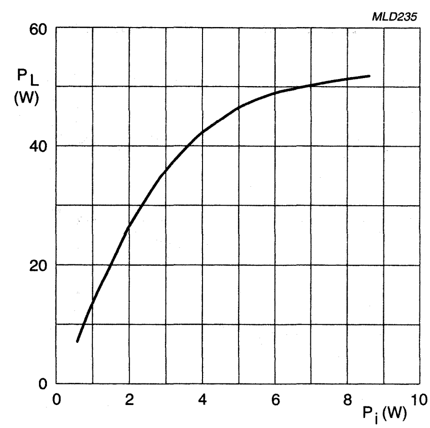
Ruggedness in class-AB operation

The BLV946 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases at rated output power, under the following conditions: V_{CE} = 26 V; f = 960 MHz; I_{CQ} = 130 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.



V_{CE} = 26 V.
I_{CQ} = 130 mA.
f = 960 MHz.

Fig.5 Power gain and efficiency as functions of load power; typical values.



V_{CE} = 26 V.
I_{CQ} = 130 mA.
f = 960 MHz.

Fig.6 Load power as a function of input power; typical values.

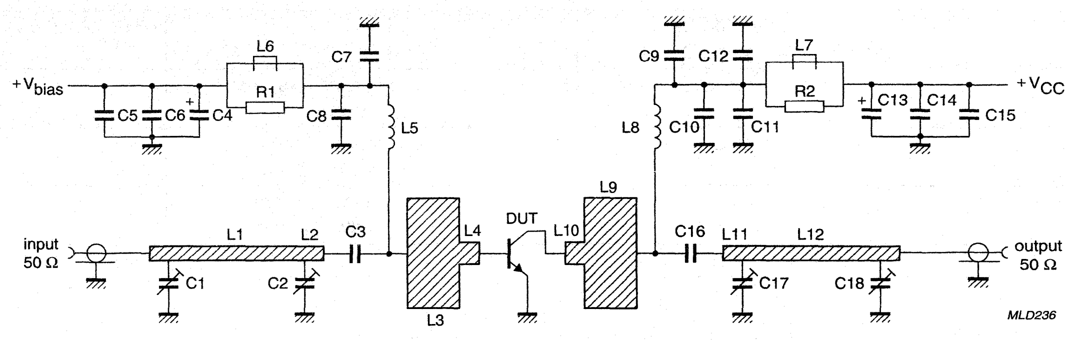


Fig.7 Class-AB test circuit at 960 MHz.

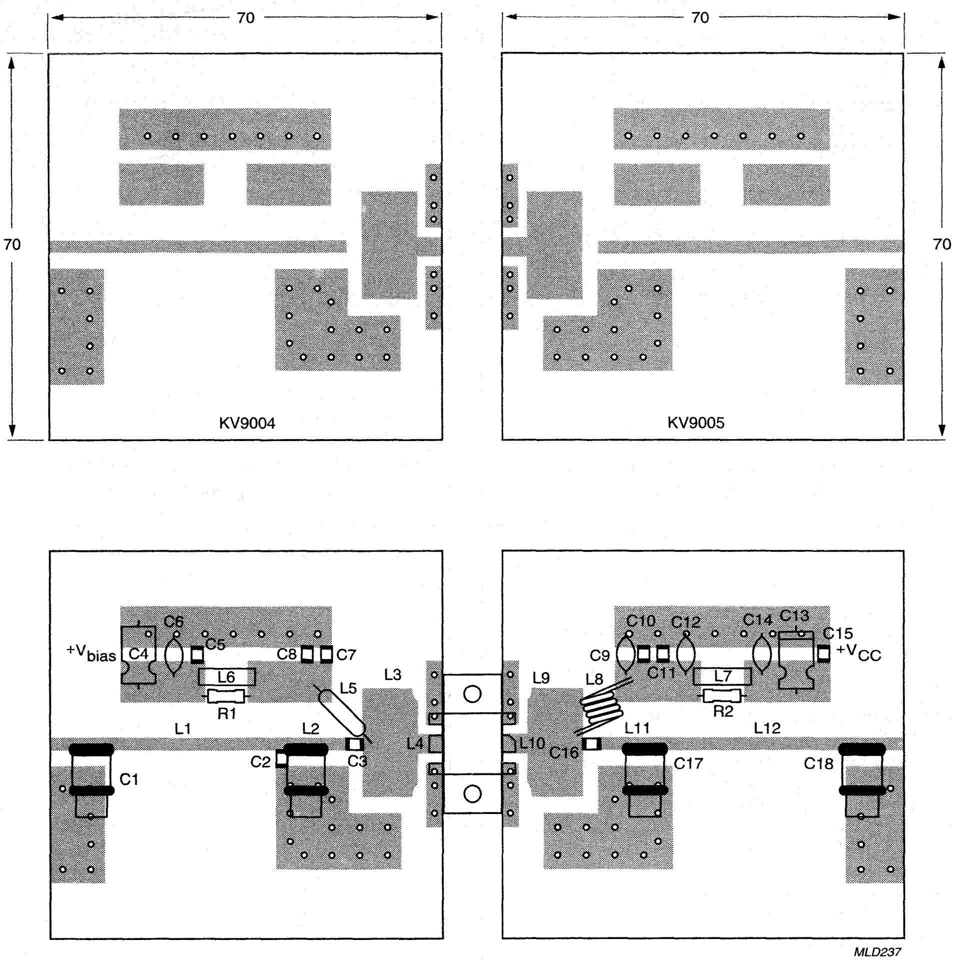
List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C17, C18	TEKELEC variable capacitor type 6451	12 pF		
C3, C16	multilayer ceramic chip capacitor; note 1	68 pF, 500 V		
C4, C13	electrolytic capacitor	10 μF, 63 V		2222 030 28109
C5, C8, C10, C13, C15	multilayer ceramic chip capacitor; note 1	20 pF, 500 V		
C6	multilayer ceramic chip capacitor	100 nF, 50 V		2222 581 76641
C7, C11	multilayer ceramic chip capacitor; note 1	100 pF, 500 V		
C9	multilayer ceramic chip capacitor	470 pF, 50 V		2222 731 18471
C12	multilayer ceramic chip capacitor	10 nF, 50 V		2222 731 18103
C14	multilayer ceramic chip capacitor	22 nF, 50 V		2222 731 18223
L1	stripline; note 2	50 Ω	length 36 mm width 2.2 mm	
L2	stripline; note 2	50 Ω	length 8 mm width 2.2 mm	
L3, L9	stripline; note 2	8 Ω	length 10 mm width 20 mm	
L4, L10	stripline; note 2	37 Ω	length 4.5 mm width 3.5 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
L5	microchoke	2.2 μH		4322 057 02281
L6, L7	Ferroxcube wide band HF choke, grade 3B			4312 020 36642
L8	4.5 turns enamelled 1 mm copper wire	50 nH	internal dia. 4 mm close wound	
L11	stripline; note 2	50 Ω	length 7 mm width 2.2 mm	
L12	stripline; note 2	50 Ω	length 37 mm width 2.2 mm	
R1, R2	metal film resistor	100 Ω; 0.4 W		2322 171 11001

Notes

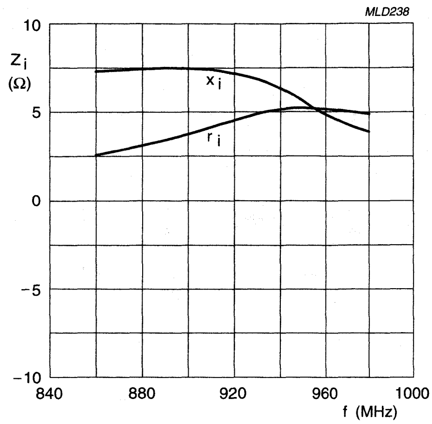
1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board, with PTFE microfibre-glass dielectric ($\varepsilon_r = 2.2$); thickness $^1\!/_{32}$"; thickness of the copper sheet 2 × 35 μm.



Dimensions in mm.

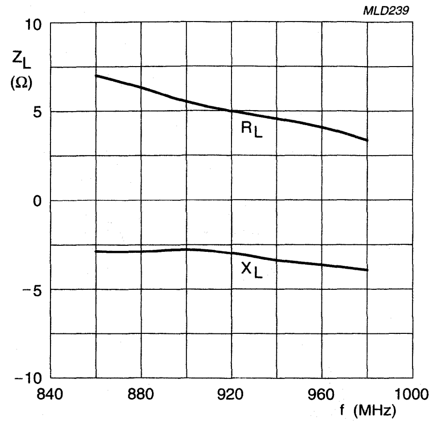
The components are located on one side of the copper-clad PTFE microfibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.8 Component layout and printed circuit board for 960 MHz class-AB test circuit.



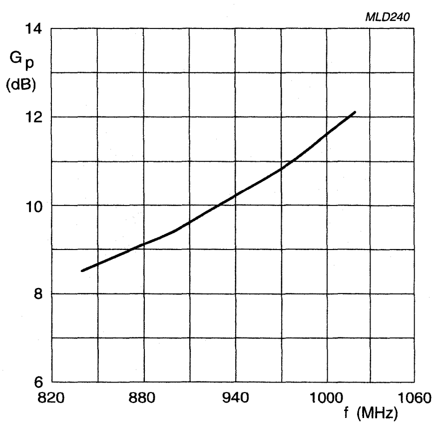
V_{CE} = 26 V; I_{CQ} = 130 mA; P_L = 40 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.9 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 130 mA; P_L = 40 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.10 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 130 mA; P_L = 40 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.11 Power gain as a function of frequency; typical values.

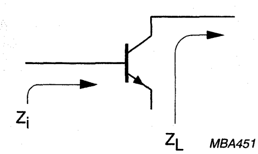


Fig.12 Definition of transistor impedance.

UHF push-pull power transistor

BLV950

FEATURES

- Internal input and output matching for easy matching, high gain and efficiency
- Poly-silicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Base station transmitters in the 800 to 960 MHz range.

DESCRIPTION

Two NPN silicon planar epitaxial transistors in push-pull configuration, intended for linear common emitter class-AB operation. The transistors are encapsulated in a 4-lead SOT262A2 flange package with 2 ceramic caps. The flange provides the common emitter connection for both transistors.

PINNING - SOT262A2

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1
2	c2	collector 2
3	b1	base 1
4	b2	base 2
5	e	common emitter; connected to flange

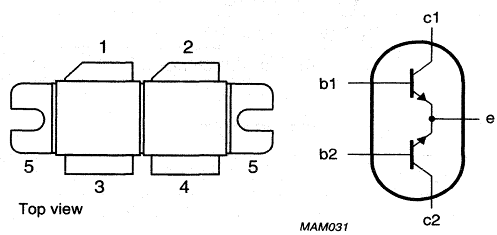


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_3 (dBc)
CW, class-AB	900	26	150	≥8	≥45	–
	960	26	150	≥7.5	≥45	–
2-tone, class-AB	900	26	150 (PEP)	≥8.5	≥35	≤–30
	960	26	150 (PEP)	≥8	≥35	≤–30

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section					
V_{CBO}	collector-base voltage	open emitter	–	70	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	12	A
$I_{C(AV)}$	average collector current		–	12	A
P_{tot}	total power dissipation (DC)	T_{mb} = 25 °C	–	340	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 340 W; T_{mb} = 25 °C; note 1	0.52	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.15	K/W

Note

1. Total device; both sections equally loaded; thermal resistance is determined under specified RF operating conditions.

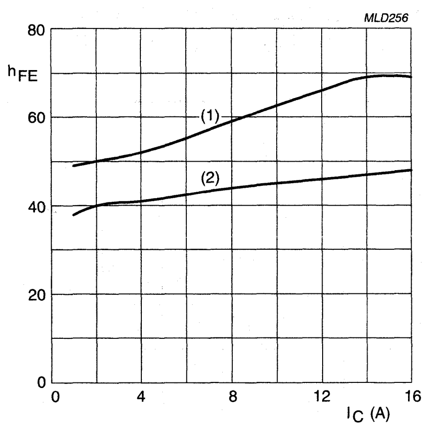
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 60 mA	70	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 150 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 3 mA	3	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0; V_{CE} = 28 V	–	–	5	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 4.5 A; note 1	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; $I_E = i_e$ = 0; f = 1 MHz; note 2	–	75	–	pF

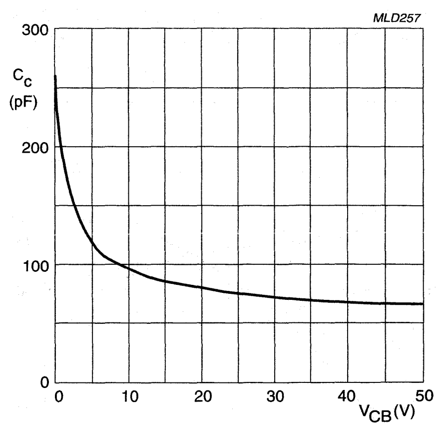
Notes

1. Measured under pulse conditions: $t_p \leq 300\ \mu s$; $\delta \leq 0.01$.
2. Value C_c is that of the die only, it is not measurable because of internal matching network.



Measured under pulsed conditions; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$.
(1) V_{CE} = 26 V.
(2) V_{CE} = 10 V.

Fig.2 DC current gain as a function of collector current; typical values.



Value C_c is that of the die only, it is not measurable because of internal matching network.
$I_E = i_e$ = 0; f = 1 MHz.

Fig.3 Collector capacitance as a function of collector-base voltage; typical values.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull test circuit; $R_{th\ mb\text{-}h}$ = 0.15 K/W.

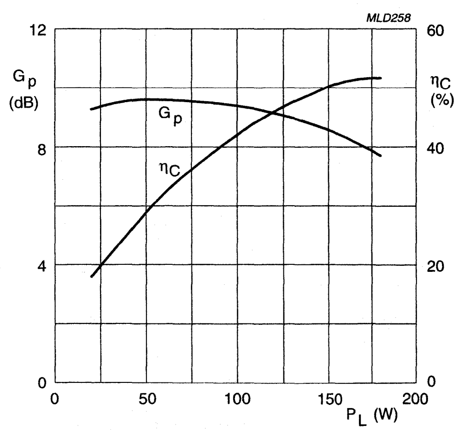
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_3 (dBc)
CW, class-AB	900	26	2 × 100	150	≥8 typ. 9	≥45 typ. 50	–
	960	26	2 × 100	150	≥7.5 typ. 8.5	≥45 typ. 50	–
2-tone, class-AB	note 1	26	2 × 100	150 (PEP)	≥8.5 typ. 9.5	≥35 typ. 40	≤–28 typ. –31
	note 2	26	2 × 100	150 (PEP)	≥8 typ. 9	≥35 typ. 40	≤–30 typ. –33

Notes

1. f_1 = 900.0 MHz; f_2 = 900.1 MHz.
2. f_1 = 960.0 MHz; f_2 = 960.1 MHz.

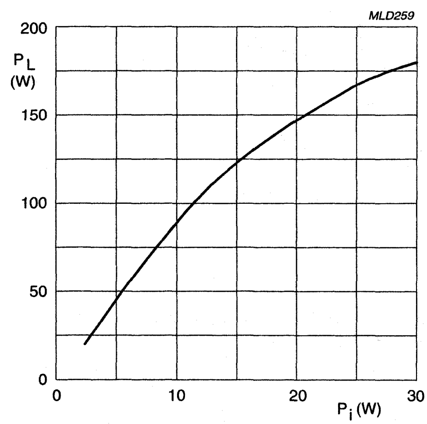
Ruggedness in class-AB operation

The BLV950 is capable of withstanding a load mismatch corresponding to VSWR = 2 : 1 through all phases under the conditions: P_L = 150 W; f = 960 MHz; V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W and also a load mismatch of VSWR = 5 : 1 through all phases at P_L = 150 W (PEP) and f_1 = 960.0 MHz and f_2 = 960.1 MHz.



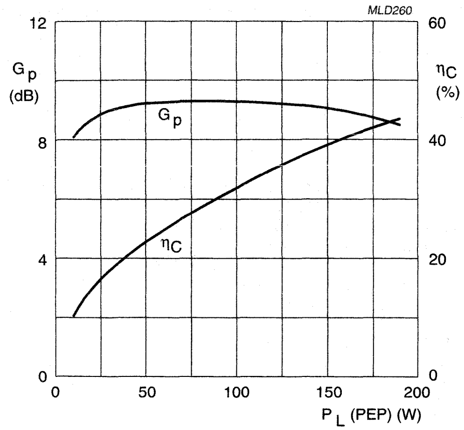
V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; f = 960 MHz.

Fig.4 Power gain and efficiency as functions of load power; typical values.



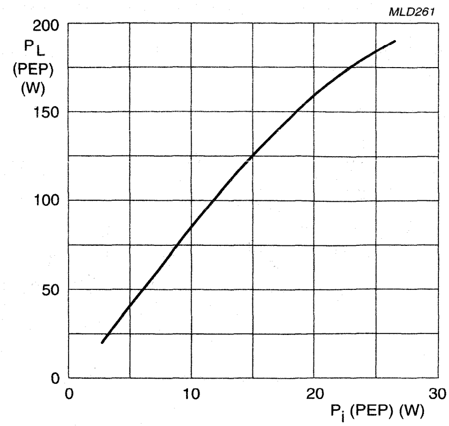
V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; f = 960 MHz.

Fig.5 Load power as a function of input power; typical values.



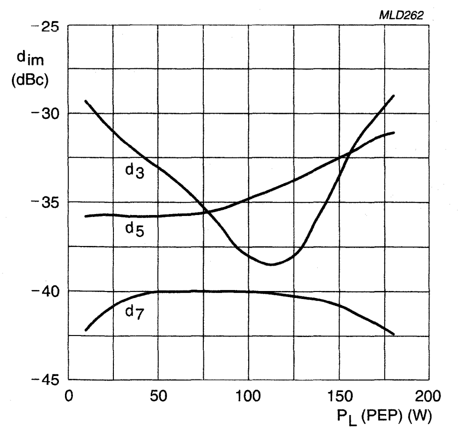
V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; f_1 = 960.0 MHz; f_2 = 960.1 MHz.

Fig.6 Power gain and efficiency as functions of load power; typical values.



V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; f_1 = 960.0 MHz; f_2 = 960.1 MHz.

Fig.7 Load power as a function of input power; typical values.



V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; f_1 = 960.0 MHz; f_2 = 960.1 MHz.

Fig.8 Intermodulation distortion as a function of load power; typical values.

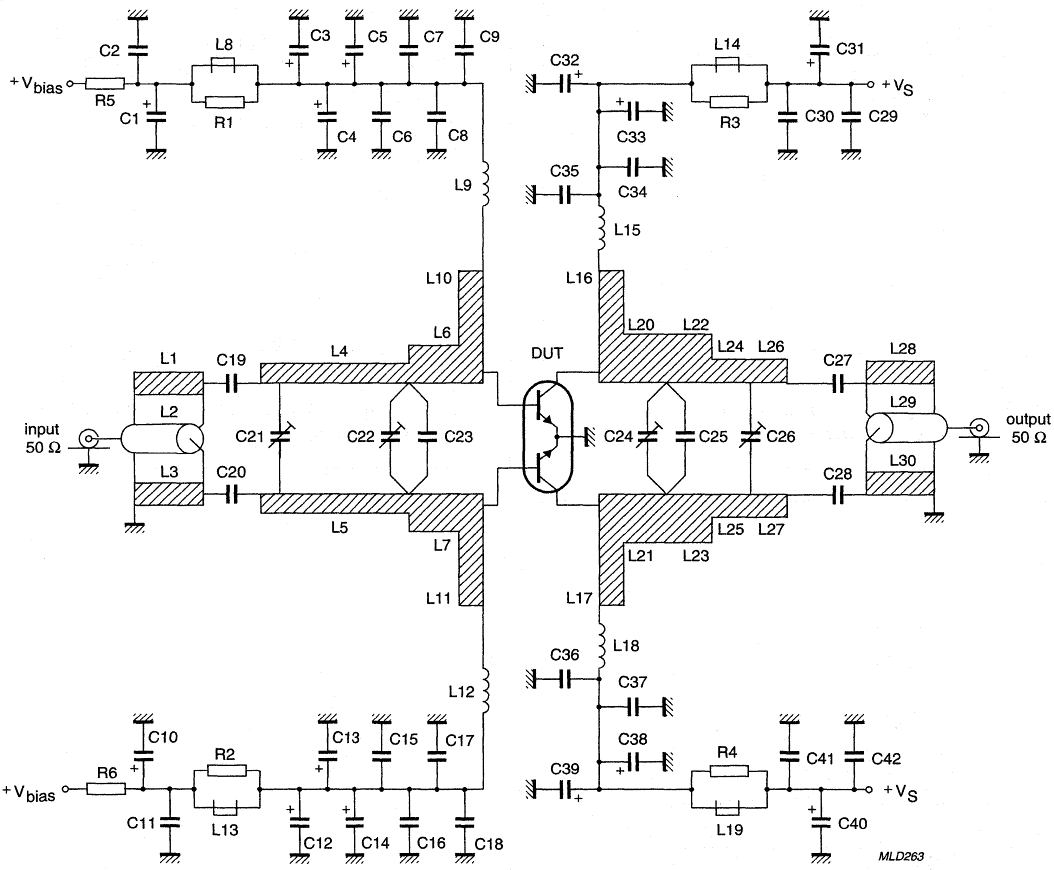


Fig.9 Class-AB test circuit at 900 to 960 MHz.

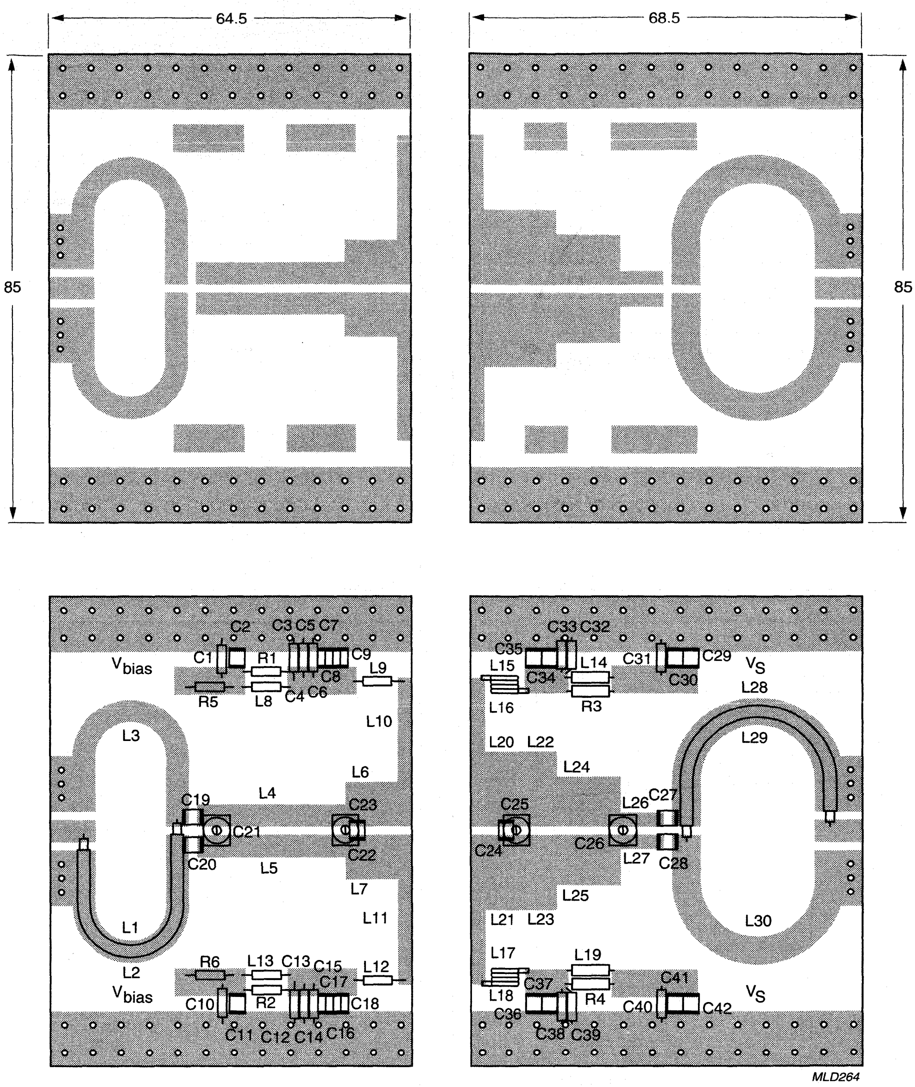
List of components (see Figs 9 and 10)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C10	tantalum capacitor	2.2 μF, 35 V		2022 019 00058
C2, C11, C30, C34, C37, C41	multilayer ceramic chip capacitor; note 1	300 pF, 200 V		
C3, C12	electrolytic capacitor	1 μF, 63 V		2222 085 78108
C4, C13	electrolytic capacitor	10 μF, 16 V		2222 085 75109
C5, C14, C31, C40	tantalum capacitor	1 μF, 35 V		2022 019 00056
C6, C15, C29, C42	multilayer ceramic chip capacitor	100 nF, 50 V		2222 581 76641
C7, C16	multilayer ceramic chip capacitor	10 nF, 50 V		2222 581 76627
C8, C17	multilayer ceramic chip capacitor; note 1	330 pF, 200 V		
C9, C18, C19, C20, C35, C36	multilayer ceramic chip capacitor; note 1	39 pF, 500 V		
C23	multilayer ceramic chip capacitor; note 1	2 pF, 500 V		
C25	multilayer ceramic chip capacitor; note 1	3.9 pF, 500 V		
C21, C22	film dielectric trimmer	9 pF		2222 809 09005
C24, C26	film dielectric trimmer	3.5 pF		2222 809 05215
C27, C28	multilayer ceramic chip capacitor; note 1	68 pF, 500 V		
C32, C39	electrolytic capacitor	10 μF, 63 V		2222 030 28109
C33, C38	electrolytic capacitor	1 μF, 63 V		2222 030 38108
L1, L3	stripline; note 2	35 Ω	length 50.7 mm width 4 mm	
L2	semi-rigid cable; note 3	50 Ω	ext. conductor length 50.7 mm ext. diameter 2.2 mm	
L4, L5	stripline; note 2	35 Ω	length 26.5 mm width 4 mm	
L6, L7	stripline; note 2	20 Ω	length 9.2 mm width 8 mm	
L10, L11, L16, L17	stripline; note 2	7 Ω	length 2.5 mm width 27 mm	
L8, L13, L14, L19	grade 4S2 Ferroxcube chip-bead			4330 030 36300
L9, L12	microchoke	4.7 μH		4322 057 04781
L15, L18	4 turns enamelled 1 mm copper wire	100 nH	int. diameter 6 mm close wound	
L20, L21	stripline; note 2	14 Ω	length 6 mm width 12.5 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
L22, L23	stripline; note 2	14 Ω	length 7 mm width 12.5 mm	
L24, L25	stripline; note 2	18 Ω	length 11 mm width 9 mm	
L26, L27	stripline; note 2	50 Ω	length 6.5 mm width 2.5 mm	
L28, L30	stripline; note 2	30 Ω	length 49.3 mm width 5 mm	
L29	semi-rigid cable; note 3	50 Ω	ext. conductor length 49.3 mm ext. diameter 3.6 mm	
R5, R6	metal film resistor	0.4 W, 1 Ω		2322 151 71008
R1, R2	metal film resistor	0.4 W, 5.11 Ω		2322 151 75118
R3, R4	metal resistor	1 W, 5.11 Ω		2322 153 75118

Notes

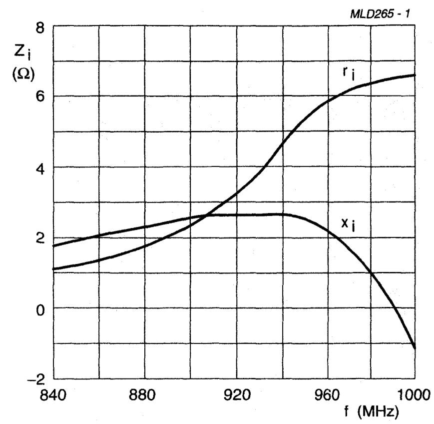
1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board, with PTFE microfibre-glass dielectric ($\varepsilon_r = 2.2$); thickness $^1/_{32}$"; thickness of the copper sheet 2×35 μm.
3. Semi-rigid cables soldered respectively on striplines L1 and L28.



Dimensions in mm.

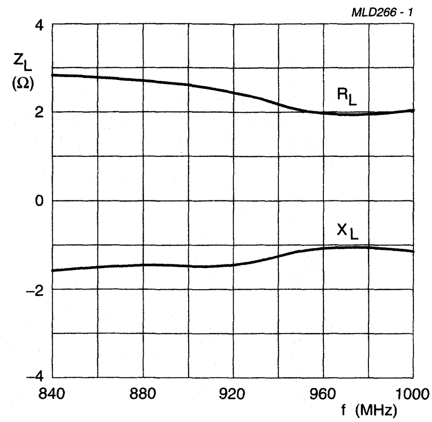
The components are situated on one side of the copper-clad PTFE microfibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.10 Component layout and printed-circuit board for 900 to 960 MHz class-AB test circuit.



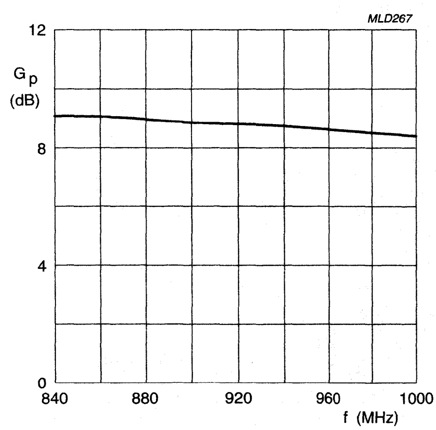
V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; P_L = 150 W (total device);
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W.

Fig.11 Input impedance as a function of frequency (series components); typical values per section.



V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; P_L = 150 W (total device);
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W.

Fig.12 Load impedance as a function of frequency (series components); typical values per section.



V_{CE} = 26 V; I_{CQ} = 2 × 100 mA; P_L = 150 W (total device);
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W.

Fig.13 Power gain as a function of frequency; typical values.

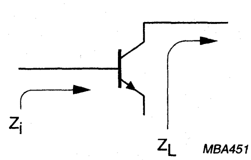


Fig.14 Definition of transistor impedance.

UHF power transistors BLV958; BLV958FL

FEATURES

- Internal input and output matching for easy matching, high gain and efficiency
- Poly-silicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Base stations in the 800 to 960 MHz frequency range.

DESCRIPTION

NPN silicon planar epitaxial transistors primarily intended for common emitter class-AB operation. The transistors have internal input and output matching by means of MOS capacitors. The encapsulations are a 2-lead rectangular SOT391A flange package and a SOT391B flangeless package, both with a ceramic cap.

PINNING - SOT391A

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	b	base
3	e	emitter; connected to flange

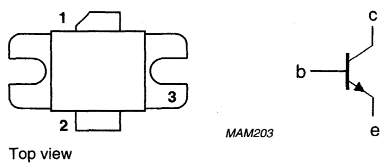


Fig.1 Simplified outline (SOT391A) and symbol.

PINNING - SOT391B

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	b	base
Ground plane	e	emitter

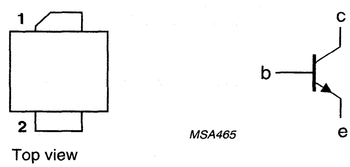


Fig.2 Simplified outline (SOT391B) and symbol.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	900	26	75	≥8	≥50
	960	26	75	≥8.5	≥50

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	70	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	15	A
$I_{C(AV)}$	average collector current		–	15	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	250	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$P_{tot} = 250$ W; $T_{mb} = 25$ °C; note 1	0.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.2	K/W

Note

1. Thermal resistance is determined under specified RF operating conditions.

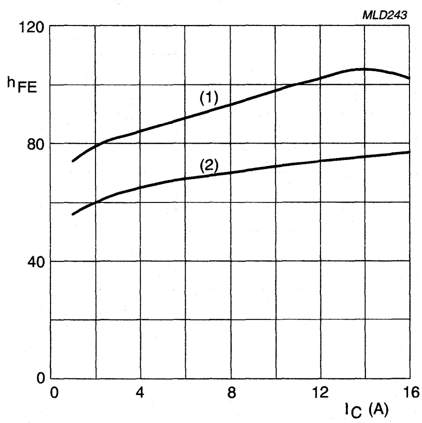
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 60 mA	70	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 150 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 3 mA	3	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0; V_{CE} = 28 V	–	–	5	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 4.5 A; note 1; see Fig 3	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; $I_E = i_e$ = 0; f = 1 MHz; note 2; see Fig 4	–	75	–	pF

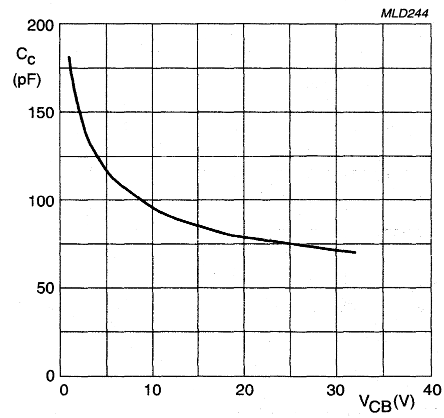
Notes

1. Measured under pulsed conditions: $t_p \leq 500$ µs; $\delta \leq 0.01$.
2. Value of C_c is that of the die only, it is not measurable because of internal matching network.



Measured under pulsed conditions; $t_p \leq 500$ µs; $\delta \leq 0.01$.
(1) V_{CE} = 26 V.
(2) V_{CE} = 10 V.

Fig.3 DC current gain as a function of collector current; typical values.



Value C_c is that of the die only, it is not measurable because of internal matching network.
$I_E = i_e$ = 0; f = 1 MHz.

Fig.4 Collector capacitance as a function of collector-base voltage; typical values.

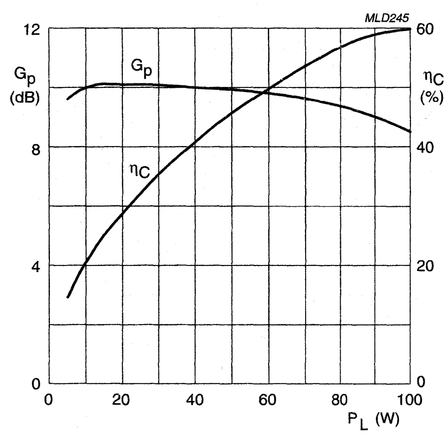
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter, class-AB test circuit; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	900	26	200	75	≥8 typ. 9.5	≥50 typ. 55
	960	26	200	75	≥8.5 typ. 9.5	≥50 typ. 55

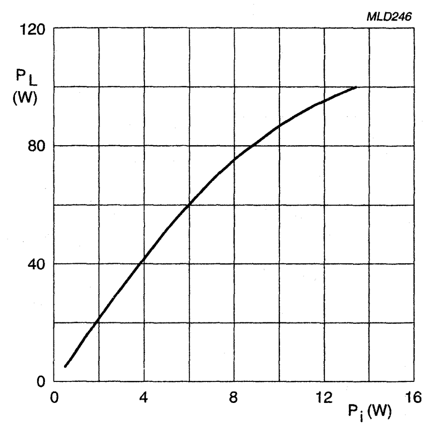
Ruggedness in class-AB operation

The transistors are capable of withstanding a load mismatch corresponding to VSWR = 4 : 1 through all phases at rated output power, under the following conditions: V_{CE} = 26 V; f = 960 MHz; I_{CQ} = 200 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.



V_{CE} = 26 V; I_{CQ} = 200 mA; f = 960 MHz.

Fig.5 Power gain and collector efficiency as functions of load power; typical values.



V_{CE} = 26 V; I_{CQ} = 200 mA; f = 960 MHz.

Fig.6 Load power as a function of input power; typical values.

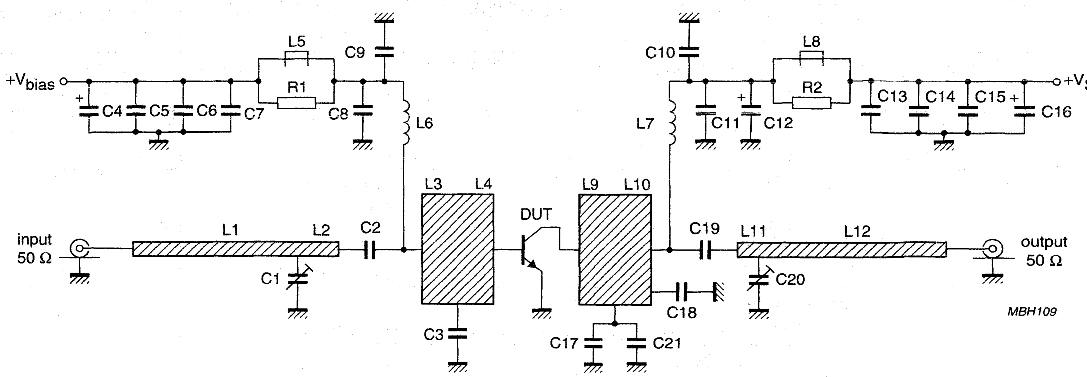


Fig.7 Class-AB test circuit at f = 960 MHz.

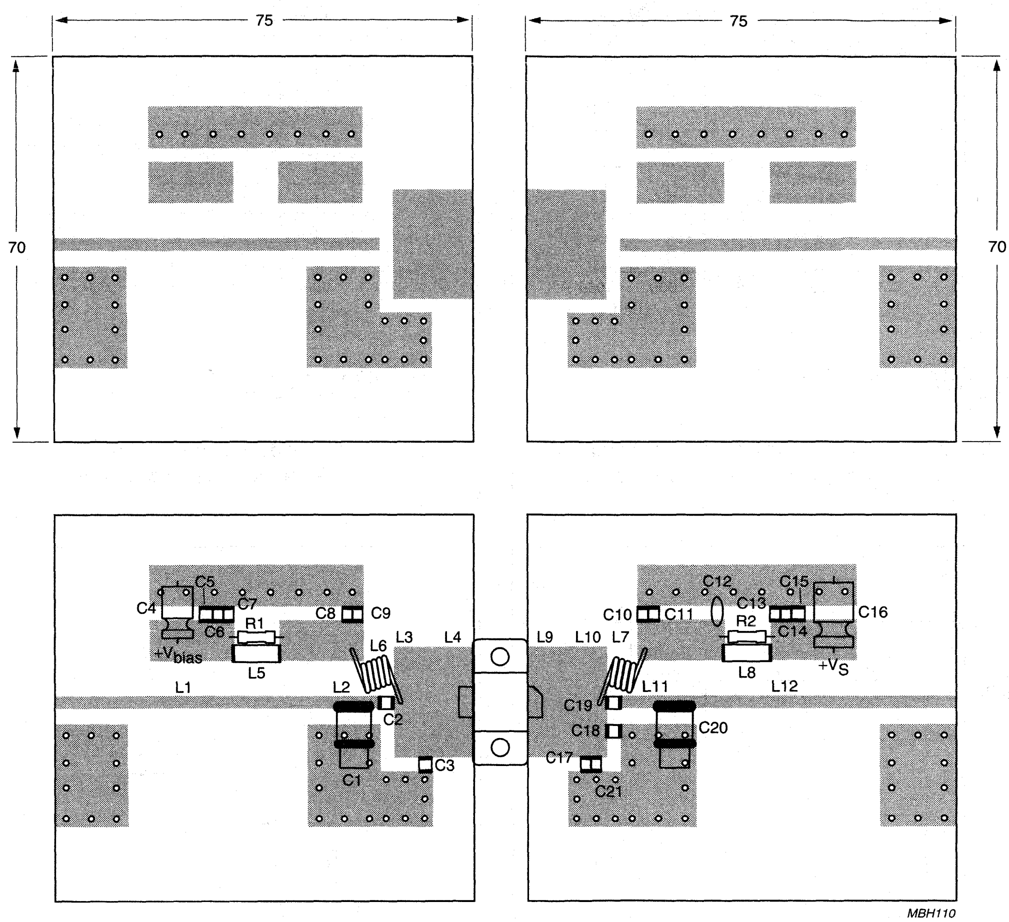
List of components (see Figs 7 and 8)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C20	Tekelec, type 5201	0.8 to 10 pF		
C2, C19	multilayer ceramic chip capacitor; note 1	15 pF; 500 V		
C3	multilayer ceramic chip capacitor; note 1	6.2 pF; 500 V		
C4	electrolytic capacitor	10 μF; 63 V		
C5	multilayer ceramic chip capacitor	22 nF; 50 V		
C6	multilayer ceramic chip capacitor; note 1	1 nF; 500 V		
C7	multilayer ceramic chip capacitor; note 1	33 pF; 500 V		2222 030 28109
C8, C11, C14	multilayer ceramic chip capacitor; note 1	100 pF; 500 V		
C9, C10, C13	multilayer ceramic chip capacitor; note 1	20 pF; 500 V		
C12	solid tantalum capacitor	1 μF; 35 V		
C15	multilayer ceramic chip capacitor	100 nF; 50 V		
C16	electrolytic capacitor	47 μF; 40 V		2222 036 68479

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C17	multilayer ceramic chip capacitor; note 1	4.7 pF; 500 V		
C18	multilayer ceramic chip capacitor; note 1	3.3 pF; 500 V		
C21	multilayer ceramic chip capacitor; note 1	2.7 pF; 500 V		
L1	stripline; note 2		length 51 mm width 2.2 mm	
L2	stripline; note 2		length 7 mm width 2.2 mm	
L3	stripline; note 2		length 5.5 mm width 20 mm	
L4	stripline; note 2		length 9 mm width 20 mm	
L5, L8	Ferroxcube chip-bead grade 4S2			4330 030 36300
L6	5 turns enamelled 1 mm copper wire		int. diameter 4 mm close wound	
L7	4 turns enamelled 1 mm copper wire		int. diameter 4 mm close wound	
L9	stripline; note 2		length 12.5 mm width 20 mm	
L10	stripline; note 2		length 2 mm width 20 mm	
L11	stripline; note 2		length 17 mm width 2.2 mm	
L12	stripline; note 2		length 41 mm width 2.2 mm	
R1, R2	metal film resistor	100 Ω; 0.4 W		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on double-clad printed-circuit board with PTFE fibre-glass dielectric ($\varepsilon_r = 2.25$); thickness $\frac{1}{32}$ inch.

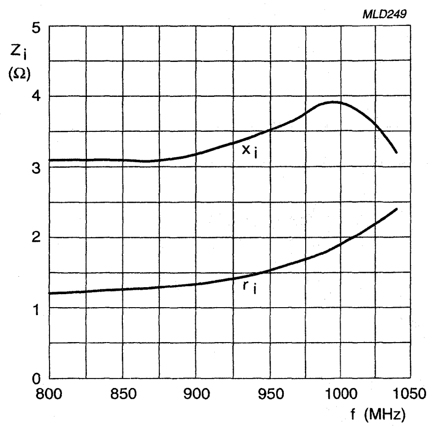


The same printed-circuit board can also be used for the flangeless version FL.

Dimensions in mm.

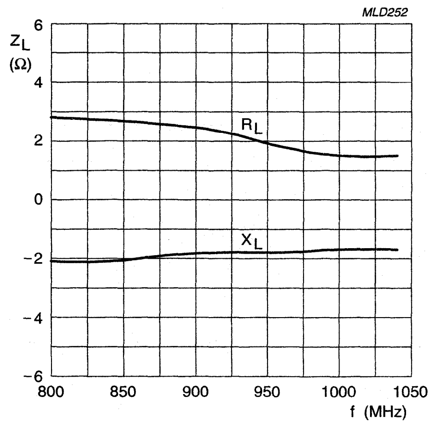
The components are located on one side of the copper-clad PTFE microfibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.8 Component layout and printed-circuit board for 960 MHz class-AB test circuit.



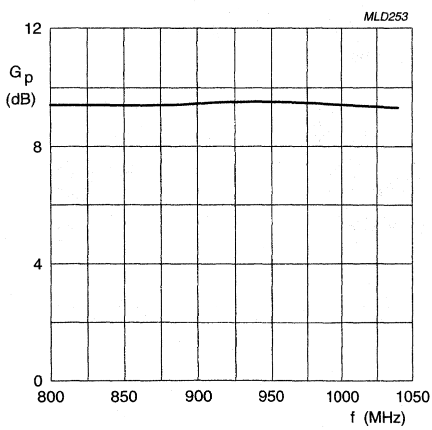
V_{CE} = 26 V; I_{CQ} = 200 mA; P_L = 75 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.9 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 200 mA; P_L = 75 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.10 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 200 mA; P_L = 75 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.11 Power gain as a function of frequency; typical values.

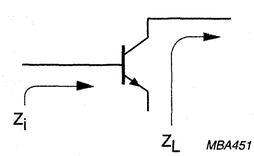


Fig.12 Definition of transistor impedance.

FEATURES

- Emitter ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability
- Internal input matching to achieve high power gain and easy design of wideband circuits.

APPLICATIONS

- Common emitter class-AB operation in base stations in the 1 800 to 1 990 MHz frequency range.

DESCRIPTION

NPN silicon planar epitaxial power transistor in an 8-lead SOT409B SMD package with ceramic cap.
All leads are isolated from the mounting base.

PINNING - SOT409B

PIN	DESCRIPTION
1, 4, 5, 8	emitter
2, 3	base
6, 7	collector

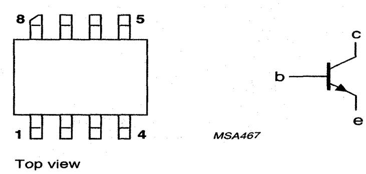


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1 950	26	4	≥11	≥40	–
CW, class-AB	1 990	26	4	≥11	≥40	–
2-tone, class-AB	f_1 = 1 950; f_2 = 1 950.1	26	4 (PEP)	typ. 14	typ. 35	typ. –30

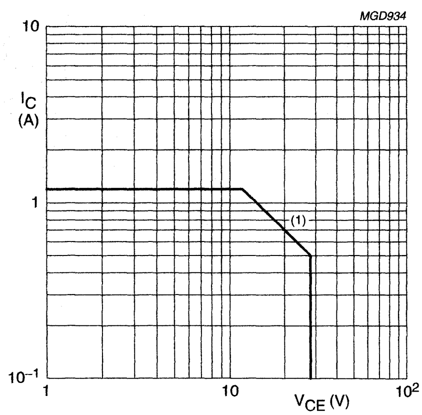
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current (DC)		–	1.2	A
$I_{C(AV)}$	collector current (average)		–	1.2	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; note 1	–	17	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

Note

1. Transistor with metallized ground plane mounted on a printed-circuit board, see *"Mounting and soldering recommendations in the General part of handbook SC19a"*.



(1) T_s = 60 °C.

Fig.2 DC SOAR.

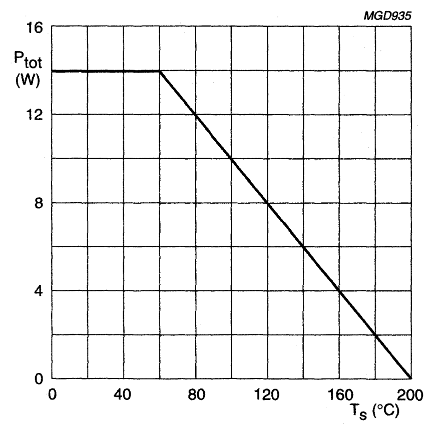


Fig.3 Total power dissipation as a function of the soldering point temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 17 W; T_{mb} = 25 °C; note 1	10	K/W

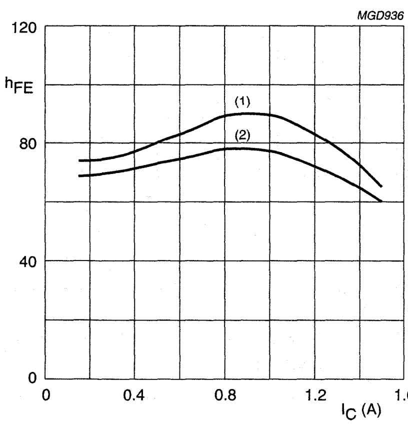
Note

1. Transistor with metallized ground plane mounted on a printed-circuit board, see *"Mounting and soldering recommendations in the General part of handbook SC19a".*

CHARACTERISTICS

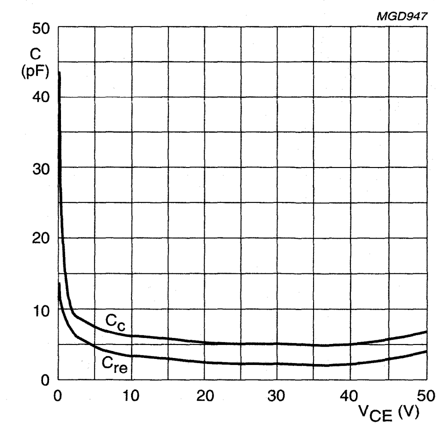
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 5 mA	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 10 mA	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.5 mA	4	–	–	V
I_{CES}	collector leakage current	V_{CE} = 26 V; V_{BE} = 0	–	–	1.3	mA
h_{FE}	DC current gain	V_{CE} = 26 V; I_C = 600 mA	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; $I_E = i_e$ = 0; f = 1 MHz	–	6	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	2.5	–	pF



(1) V_{CE} = 26 V; t_p = 500 μs; δ = < 1 %.
(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.



f = 1 MHz.

Fig.5 Capacitance as a function of collector-emitter voltage; typical values.

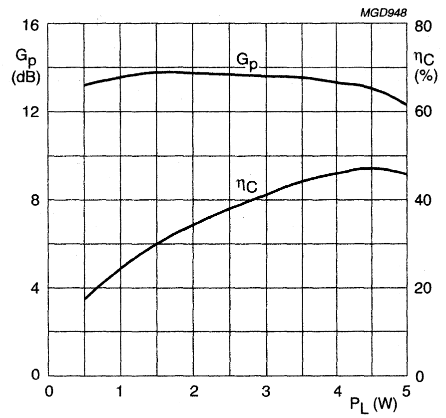
APPLICATION INFORMATION

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1950	26	15	4	≥11 typ. 13	≥40 typ. 45	–
CW, class-AB	1990	26	15	4	≥11	≥40	–
2-tone, class-AB	f_1 = 1950; f_2 = 1950.1	26	15	4 (PEP)	typ. 14	typ. 35	typ. −30

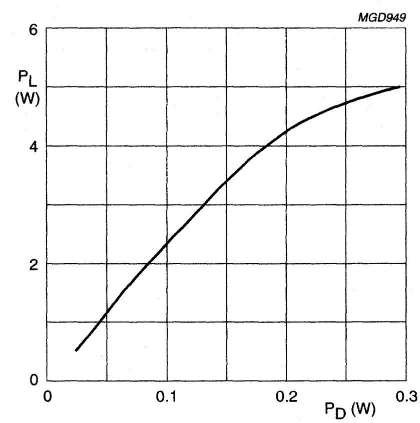
Ruggedness in class-AB operation

The BLV2042 is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: f = 1950 MHz; V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.



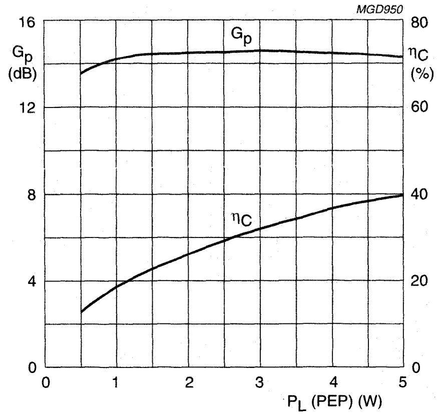
CW, class-AB; V_{CE} = 26 V; I_{CQ} = 15 mA; f = 1950 MHz; T_{mb} = 25 °C.

Fig.6 Power gain and collector efficiency as functions of load power; typical values.



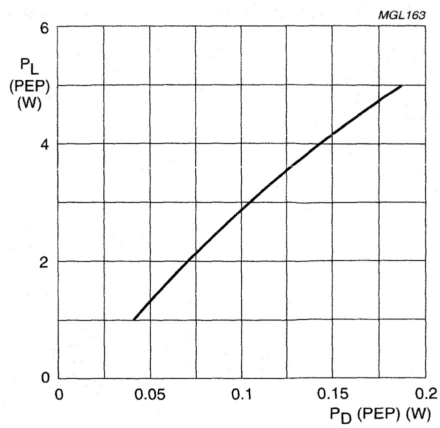
CW, class-AB; V_{CE} = 26 V; I_{CQ} = 15 mA; f = 1950 MHz; T_{mb} = 25 °C.

Fig.7 Load power as a function of drive power; typical values.



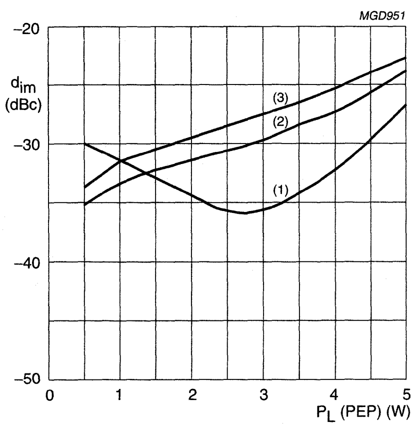
V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.8 Power gain and collector efficiency as functions of peak envelope load power; typical values.



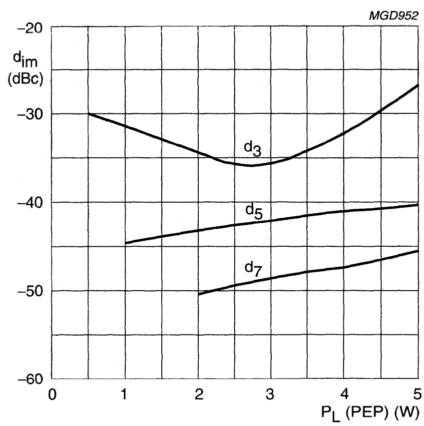
V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.9 Peak envelope load power as a function of peak envelope drive power; typical values.



V_{CE} = 26 V; f_1 = 1950 MHz; f_2 = 1950.1 MHz.
(1) I_{CQ} = 15 mA. (2) I_{CQ} = 40 mA. (3) I_{CQ} = 60 mA.

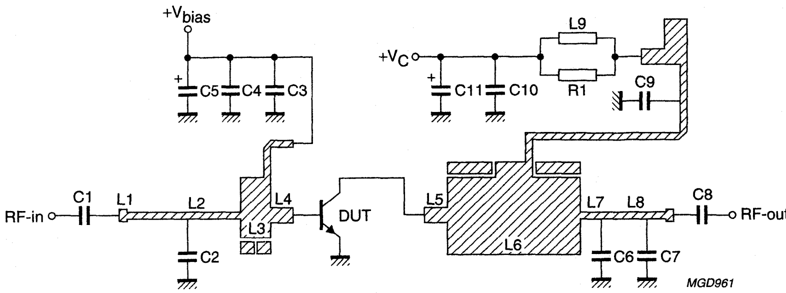
Fig.10 Third order intermodulation distortion as a function of peak envelope load power; typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.11 Intermodulation distortion as a function of peak envelope load power; typical values.

Test circuit information



f = 1950 MHz.

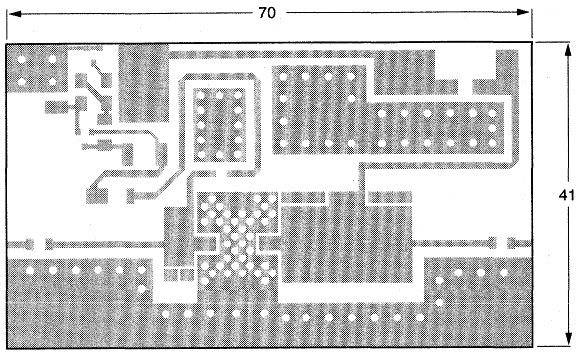
Fig.12 Class-AB test circuit.

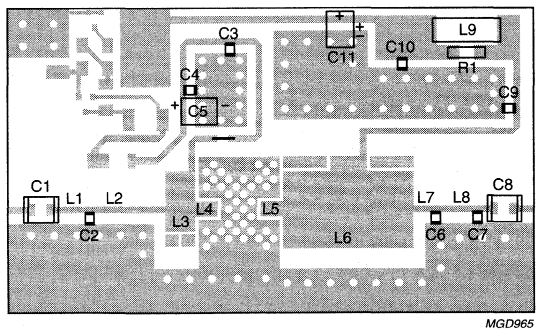
List of components (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C9	multilayer ceramic chip capacitor; note 1	100 pF		
C2, C6	multilayer ceramic chip capacitor; note 2	3 pF		
C3, C8	multilayer ceramic chip capacitor; note 2	27 pF		
C4, C10	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C5, C11	tantalum SMD capacitor	47 μF; 35 V		
C7	multilayer ceramic chip capacitor; note 2	1.2 pF		
L1	stripline; note 3	50 Ω	length 9.9 mm width 0.91 mm	
L2	stripline; note 3	50 Ω	length 6.66 mm width 0.91 mm	
L3	stripline; note 3	10 Ω	length 4 mm width 8 mm	
L4	stripline; note 3	31 Ω	length 3 mm width 2 mm	
L5	stripline; note 3	31 Ω	length 3 mm width 2 mm	
L6	stripline; note 3	8.3 Ω	length 17.25 mm width 10.3 mm	
L7	stripline; note 3	50 Ω	length 2.42 mm width 0.91 mm	
L8	stripline; note 3	50 Ω	length 6.14 mm width 0.91 mm	
L9	grade 4S2 ferroxcube chip-bead			4330 030 36301
R1	metal film resistor	100 Ω; 0.4 W		
DUT	transistor	BLV2042		

Notes

1. American Technical Ceramics type 100B or capacitor of the same quality.
2. American Technical Ceramics type 100A or capacitor of the same quality.
3. The striplines are on a double copper-clad printed-circuit board with epoxy fibreglass dielectric ($\varepsilon_r = 6.15$); thickness 0.64 mm.



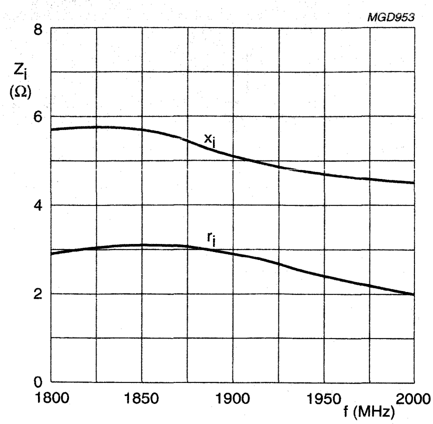


Dimensions in mm.

f = 1 950 MHz.

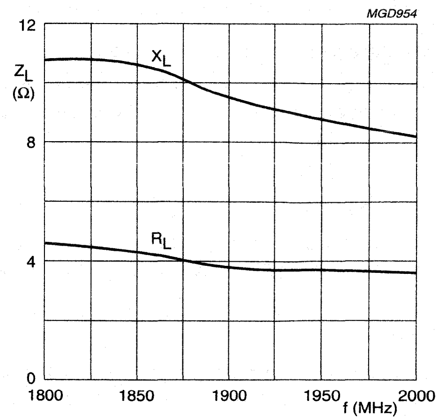
The components are situated on one side of the copper-clad epoxy fibreglass board, the other side is not etched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.13 Component layout for class-AB test circuit.



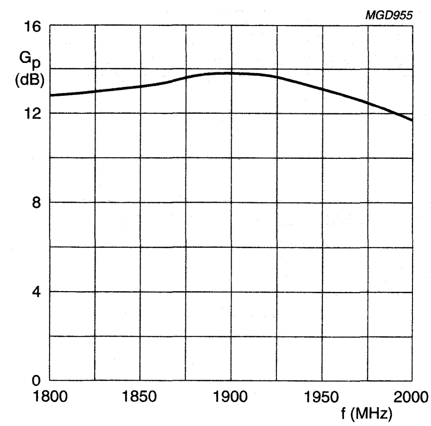
V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.

Fig.14 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.

Fig.15 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.

Fig.16 Power gain as a function of frequency; typical values.

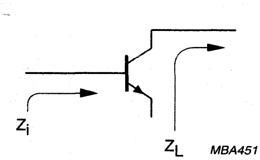


Fig.17 Definition of transistor impedance.

MOUNTING RECOMMENDATIONS

Heat from the device is transferred via the leads and the metallized underside. For optimum heat transfer it is recommended that the transistor be mounted on a grounded metallized area on the component side of the printed-circuit board. This metallized area should contain a large number of metallized, solder-filled through-holes. The non-component side of the printed-circuit board forms a ground plane. When the printed-circuit board is mounted on the heatsink using heatsink compound, a thermal resistance from mounting base to heatsink of 0.9 K/W can be attained.

UHF power transistor BLV2044

FEATURES

- Emitter ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability
- Internal input and output matching to achieve high power gain and collector efficiency for an easy design of wideband circuits.

APPLICATIONS

- Common emitter class-AB operation in base station transmitters in the 1800 to 2000 MHz frequency range.

DESCRIPTION

NPN silicon planar transistor in a 2-lead SOT437A flange package with a ceramic cap. The emitter is connected to the flange.

PINNING - SOT437A

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	b	base
3	e	emitter, connected to flange

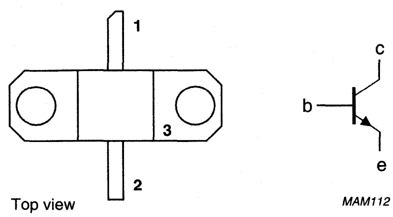


Fig.1 SOT437A.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1950	26	15	≥8	≥40	–
CW, class-AB	1990	26	15	≥8	≥40	–
2-tone, class-AB	f_1 = 1950; f_2 = 1950.1	26	15 (PEP)	typ. 8.5	typ. 35	typ. −30

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

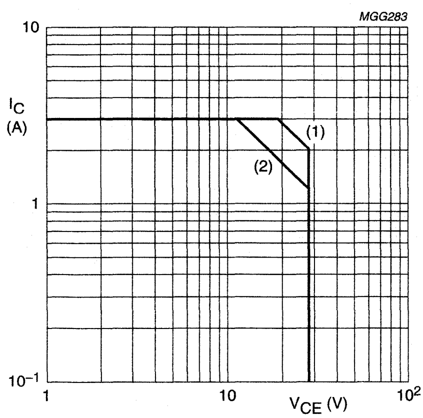
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	collector current (DC)		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	57	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	200	°C

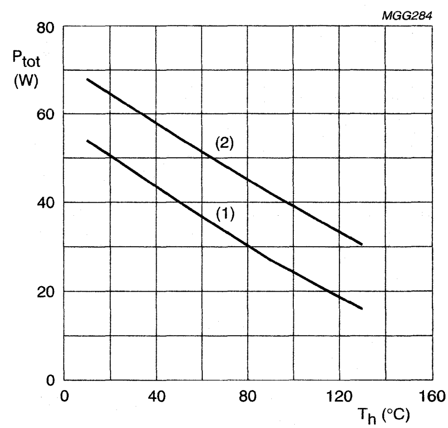
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 57 W; T_{mb} = 25 °C	3.07	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W



(1) T_{mb} =25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

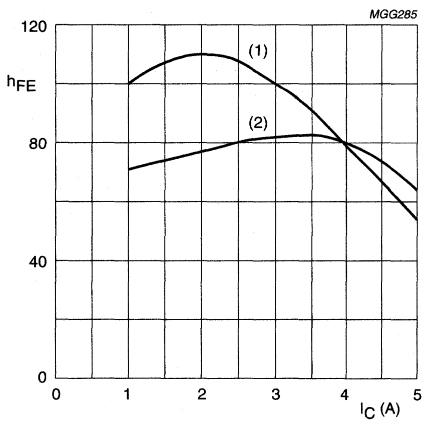
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 20 mA	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 10 mA	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.5 mA	2.5	–	–	V
I_{CES}	collector leakage current	V_{CE} = 12.5 V; V_{BE} = 0	–	–	4	mA
h_{FE}	DC current gain	V_{CE} = 26 V; I_C = 1 A	45	100	120	
C_c	collector capacitance	V_{CB} = 26 V; $I_E = i_e$ = 0; f = 1 MHz; note 1	–	16	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	8	–	pF

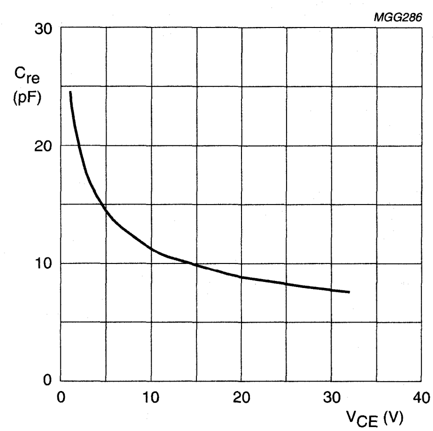
Note

1. Capacitance of die only.



(1) V_{CE} = 26 V; t_p = 500 μs; δ = < 1 %.
(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.



f = 1 MHz.

Fig.5 Feedback capacitance as a function of collector-emitter voltage; typical values.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter test circuit.

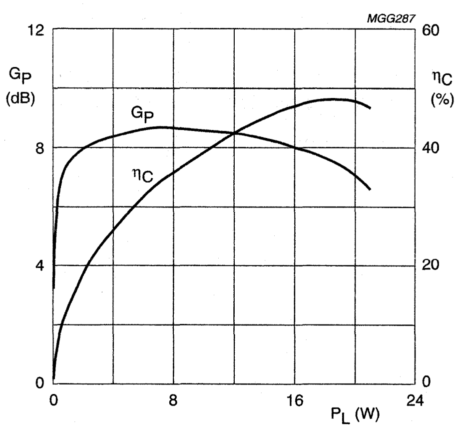
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1950	26	40	15	≥8 typ. 8.5	≥40 typ. 45	–
CW, class-AB (note 1)	1990	26	40	15	≥8	≥40	–
2-tone, class-AB	f_1 = 1950, f_2 = 1950.1	26	40	15 (PEP)	typ. 8.5	typ. 35	typ. –30

Note

1. See application note BLV2044.

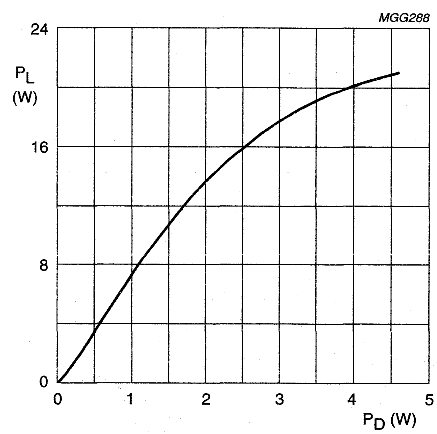
Ruggedness in class-AB operation

The BLV2044 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: f = 1950 MHz; V_{CE} = 26 V; I_{CQ} = 40 mA; P_L = 15 W; T_{mb} = 25 °C.



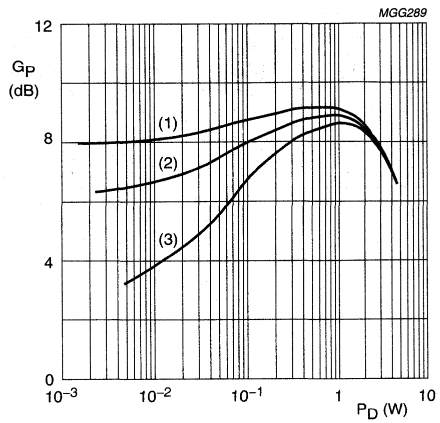
V_{CE} = 26 V; I_{CQ} = 40 mA; f = 1950 MHz.

Fig.6 Power gain and collector efficiency as functions of load power; typical values.



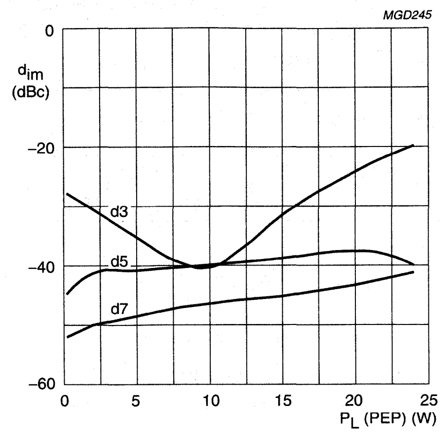
V_{CE} = 26 V; I_{CQ} = 40 mA; f = 1950 MHz.

Fig.7 Load power as a function of drive power; typical values.



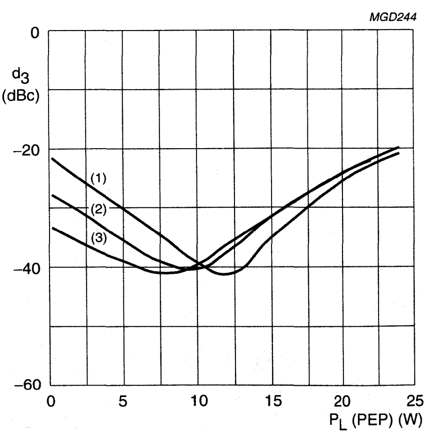
V_{CE} = 26 V; f = 1950 MHz.
(1) I_{CQ} = 120 mA. (2) I_{CQ} = 80 mA. (3) I_{CQ} = 40 mA.

Fig.8 Power gain as a function of drive power; typical values.



V_{CE} = 26 V; I_{CQ} = 40 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.9 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{CE} = 26 V; f_1 = 1950 MHz; f_2 = 1950.1 MHz.
(1) I_{CQ} = 20 mA. (2) I_{CQ} = 40 mA. (3) I_{CQ} = 60 mA.

Fig.10 Third order intermodulation distortion as a function of peak envelope load power; typical values.

Test circuit information

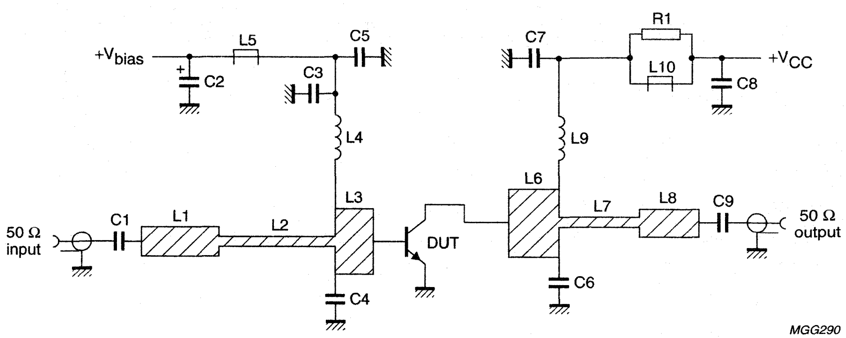


Fig.11 Class-AB test circuit for 1.8 to 2 GHz.

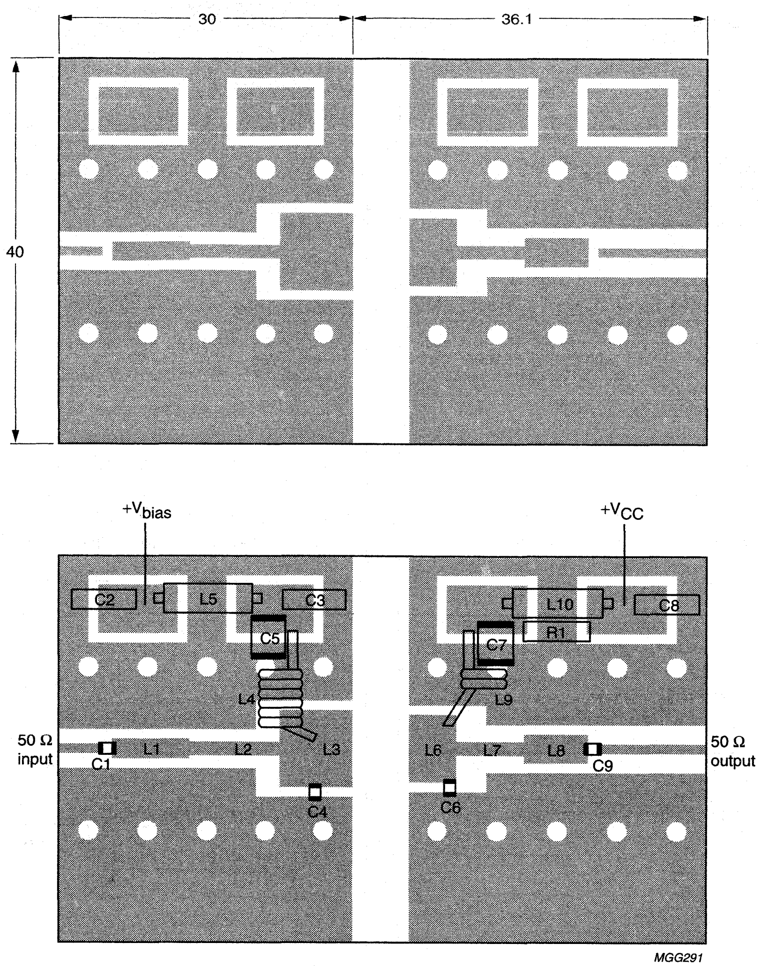
List of components (see Figs 11 and 12)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C9	multilayer ceramic chip capacitor; note 1	30 pF		
C2	tantalum SMD capacitor	10 μF; 35 V		
C3	multilayer ceramic chip capacitor	22 nF		2222 629 08223
C4	multilayer ceramic chip capacitor; note 1	1.1 pF		
C5, C7	multilayer ceramic chip capacitor; note 2	20 pF		
C6	multilayer ceramic chip capacitor; note 1	1.2 pF		
C8	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	stripline; note 3	31 Ω	length 7.8 mm width 2 mm	
L2	stripline; note 3	40 Ω	length 8.8 mm width 1.4 mm	
L3	stripline; note 3	10 Ω	length 8 mm width 8 mm	
L4	5 turns enamelled 1 mm copper wire	38 nH	length 8 mm int. dia. 3 mm	
L5, L10	grade 4S2 ferroxcube chip-bead			4330 030 36301
L6	stripline; note 3	12 Ω	length 5 mm width 7 mm	
L7	stripline; note 3	40 Ω	length 6.7 mm width 1.4 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L8	stripline; note 3	23 Ω	length 6.4 mm width 3 mm	
L9	2 turns enamelled 1 mm copper wire	9 nH	length 4 mm int. dia. 3 mm	
R1	metal film resistor	10 Ω; 0.4 W		2311 153 51009

Notes

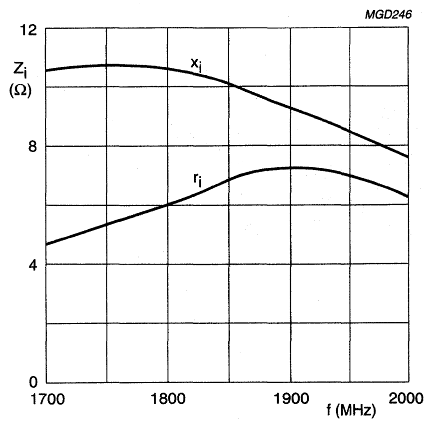
1. American Technical Ceramics type 100A or capacitor of the same quality.
2. American Technical Ceramics type 100B or capacitor of the same quality.
3. The striplines are on a double copper-clad printed-circuit board with epoxy fibre-glass dielectric (ε_r = 6.15); thickness 0.64 mm.



Dimensions in mm.

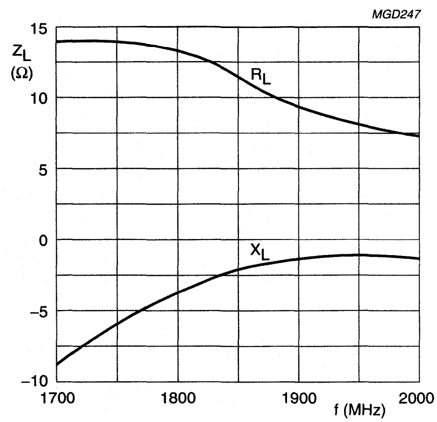
The components are situated on one side of the copper-clad epoxy fibre-glass board, the other side is not etched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.12 Component layout and printed-circuit board for 1.8 to 2 GHz class-AB test circuit.



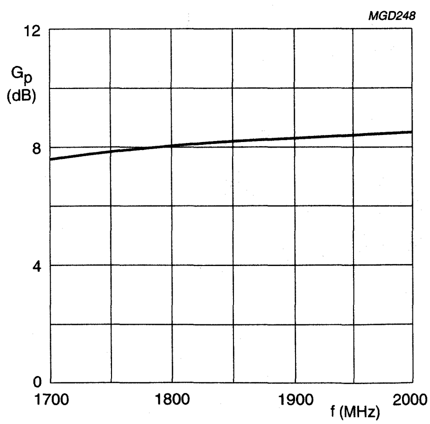
V_{CE} = 26 V; I_{CQ} = 40 mA; P_L = 15 W; T_{mb} = 25 °C.

Fig.13 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 40 mA; P_L = 15 W; T_{mb} = 25 °C.

Fig.14 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 40 mA; P_L = 15 W; T_{mb} = 25 °C.

Fig.15 Power gain as a function of frequency; typical values.

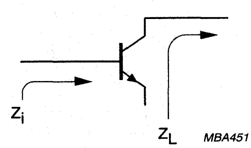


Fig.16 Definition of transistor impedance.

UHF power transistor BLV2045N

FEATURES

- Emitter ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability
- Internal input and output matching for an easy design of wideband circuits.

APPLICATIONS

- Common emitter class-AB operation in PCN and PCS applications in the 1800 to 2000 MHz frequency range.

DESCRIPTION

NPN silicon planar UHF power transistor in a 2-lead SOT390A flange package with a ceramic cap. The emitter is connected to the flange.

PINNING - SOT390A

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	b	base
3	e	emitter, connected to flange

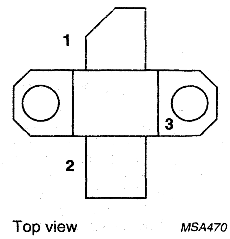


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1990	26	35	typ. 9.5	typ. 43	–
2-tone, class-AB	f_1 = 1990.0; f_2 = 1990.1	26	35 (PEP)	≥9.5	≥33	≤–30

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	4	A
$I_{C(AV)}$	average collector current		–	4	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$P_L = 35$ W; $\eta_C = 40\%$; $T_{mb} = 25$ °C	1.4	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; $I_C = 20$ mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; $I_C = 60$ mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 40$ mA	3	–	–	V
I_{CES}	collector leakage current	$V_{CE} = 26$ V; $V_{BE} = 0$	–	–	4	mA
h_{FE}	DC current gain	$V_{CE} = 10$ V; $I_C = 2$ A	45	–	100	
C_c	collector capacitance	$V_{CB} = 26$ V; $I_E = i_e = 0$; f = 1 MHz; note 1	–	t.b.f.	–	pF
C_{re}	feedback capacitance	$V_{CE} = 26$ V; $I_C = 0$; f = 1 MHz	–	t.b.f.	–	pF

Note

1. Capacitance of die only.

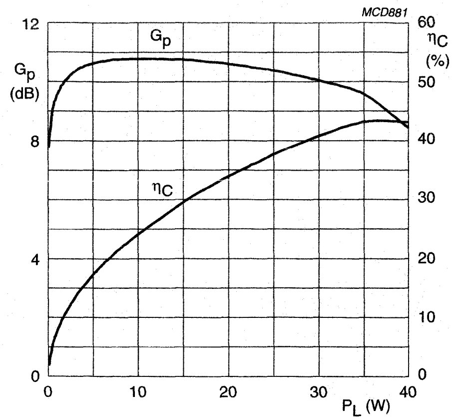
APPLICATION INFORMATION

RF performance at $T_h = 25$ °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1990	26	150	35	typ. 9.5	typ. 43	–
2-tone, class-AB	$f_1 = 1990.0$; $f_2 = 1990.1$	26	150	35 (PEP)	≥9.5 typ. 10.2	≥33 typ. 35	≤–30 typ. –32

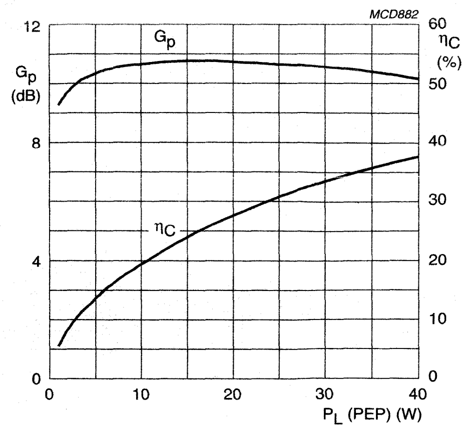
Ruggedness in class-AB operation

The BLV2045N is capable of withstanding a load mismatch corresponding to VSWR = 3 : 1 through all phases under the following conditions: $f_1 = 1990.0$ MHz; $f_2 = 1990.1$ MHz; $V_{CE} = 26$ V; $I_{CQ} = 150$ mA; $P_L = 35$ W (PEP); $T_{mb} = 25$ °C.



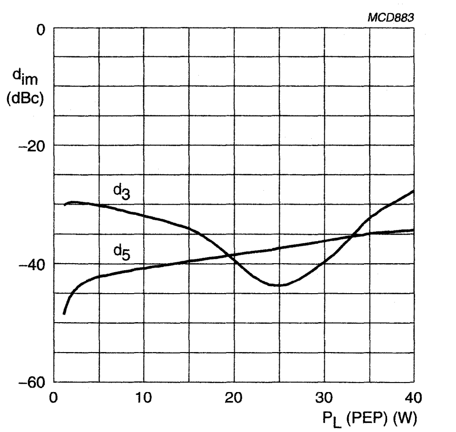
V_{CE} = 26 V; I_{CQ} = 150 mA; f = 1990 MHz.

Fig.2 Power gain and collector efficiency as functions of load power; typical values.



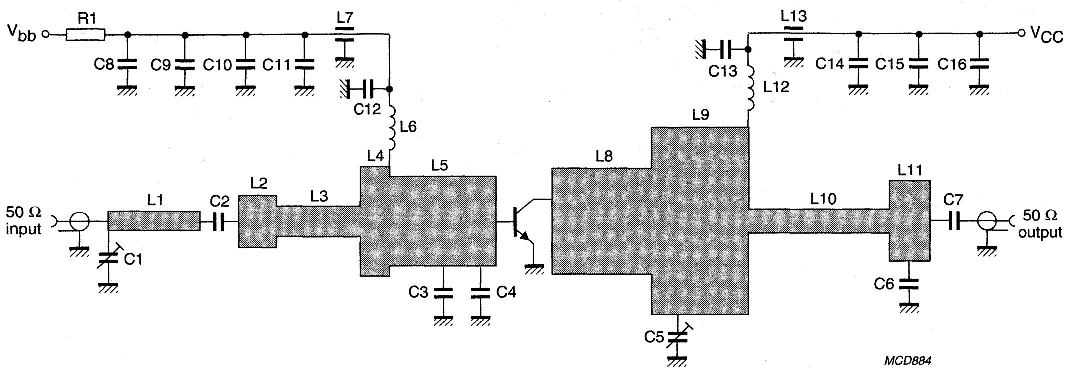
V_{CE} = 26 V; I_{CQ} = 150 mA; f_1 = 1990 MHz; f_2 = 1990.1 MHz

Fig.3 Power gain and collector efficiency as functions of peak envelope load power; typical values.



V_{CE} = 26 V; I_{CQ} = 150 mA; f_1 = 1990 MHz; f_2 = 1990.1 MHz.

Fig.4 Intermodulation distortion as a function of peak envelope load power; typical values.



Dimensions in mm.

The components are situated on one side of the copper-clad board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

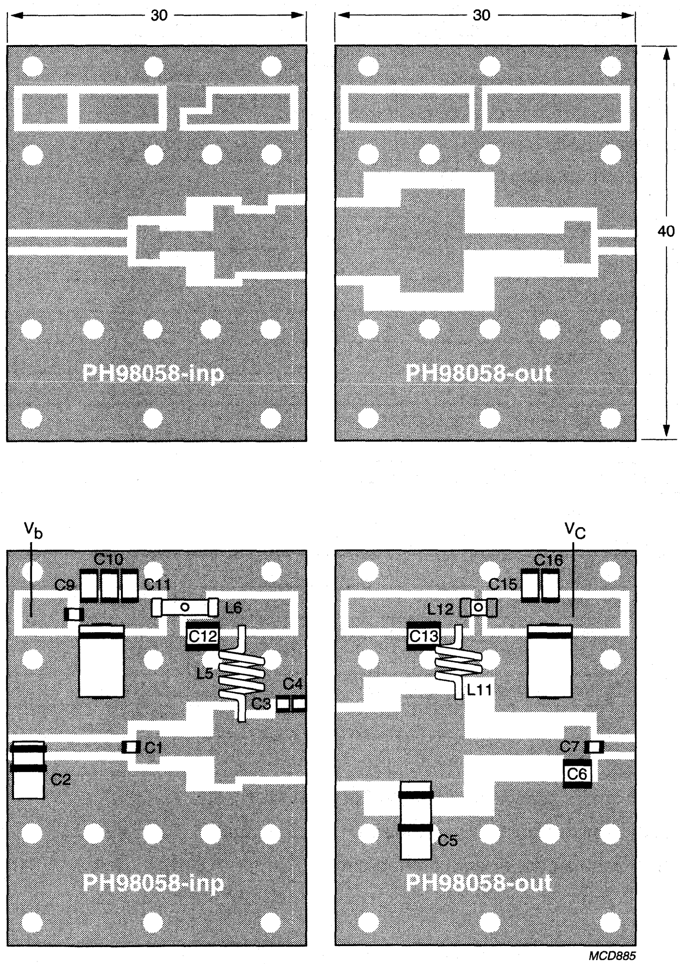
Fig.5 Class-AB test circuit for 1990 MHz.

List of components (see Figs 5 and 6)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	Tekelec variable capacitor; type AT37281	0.4 to 2.5 pF	
C2, C7	multilayer ceramic chip capacitor; note1	30 pF	
C3	multilayer ceramic chip capacitor; note 2	2.4 pF	
C4	multilayer ceramic chip capacitor; note 2	1.8 pF	
C5	Tekelec variable capacitor; type AT37271	0.6 to 4.5 pF	
C6	multilayer ceramic chip capacitor; note 2	1.3 pF	
C8, C14	tantalum SMD capacitor	35 V; 10 μF	
C9, C10, C11, C15, C16	multilayer ceramic chip capacitor	100 nF	
C12, C13	multilayer ceramic chip capacitor; note 2	20 pF	
L1	stripline; note 3	50 Ω	8 x 1 mm
L2	stripline; note 3	20.5 Ω	2.5 x 3.5 mm
L3	stripline; note 3	29.8 Ω	5.6 x 2.1 mm
L4	stripline; note 3	11 Ω	2.0 x 7.4 mm
L5	stripline; note 3	13.2 Ω	7.2 x 6.0 mm
L6	5 turns enamelled 1 mm copper wire		int. dia. = 3.3 mm; length = 6 mm
L7	EMI filter; type NFM61RH20T332	3300 pF	
L8	stripline; note 3	11.5 Ω	6.6 x 7.1 mm
L9	stripline; note 3	6.9 Ω	6.4 x 12.6 mm
L10	stripline; note 3	35.8 Ω	9.9 x 1.6 mm
L11	stripline; note 3	14.4 Ω	2.7 x 5.4 mm
L12	2 turns enamelled 1 mm copper wire		int. dia. = 3.3 mm; length = 2.5 mm
L13	EMI filter; type NFM60RH20T152	1500 pF	
R1	chip resistor	2.2 Ω	

Notes

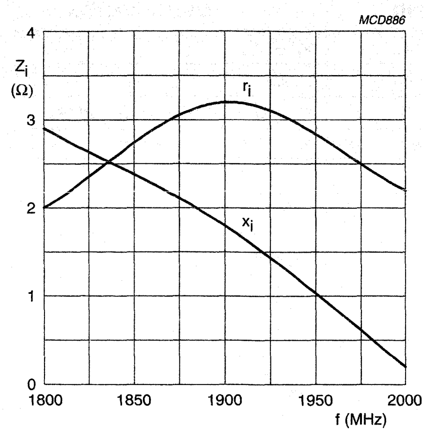
1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board: $\varepsilon_r = 6.15$; thickness 0.64mm.



Dimensions in mm.

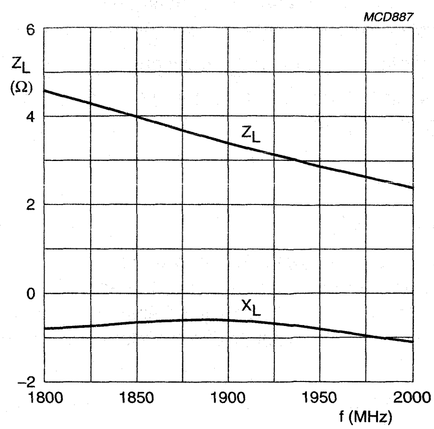
The components are situated on one side of the copper-clad board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.6 Printed-circuit board and component layout for class-AB broadband test circuit.



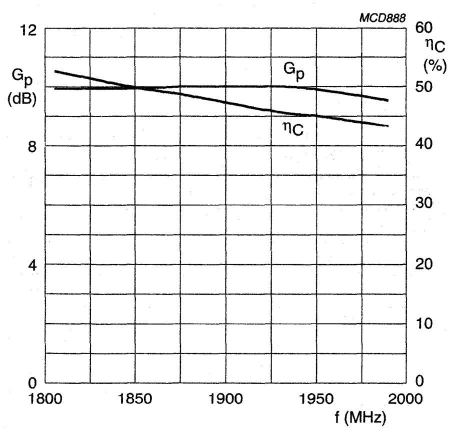
V_{CE} = 26 V; I_{CQ} = 150 mA; P_L = 35 W; T_{mb} = 25 °C.

Fig.7 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 150 mA; P_L = 35 W; T_{mb} = 25 °C.

Fig.8 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 150 mA; P_L = 35 W; T_{mb} = 25 °C.

Fig.9 Power gain and collector efficiency as functions of frequency; typical values.

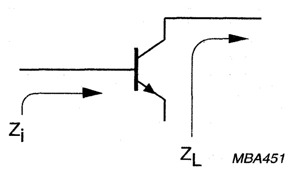


Fig.10 Definition of transistor impedance.

UHF power transistor BLV2047

FEATURES

- Emitter ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability
- Internal input and output matching for easy design of wideband circuits
- AlN substrate package for environmental safety.

APPLICATIONS

- Common emitter class-AB operation for PCN (Personal Communication Networks) and PCS (Personal Communication Services) base station applications in the 1800 to 2000 MHz frequency range.

DESCRIPTION

NPN silicon planar power transistor in a 2-lead SOT468A flange package with ceramic cap. The emitter is connected to the flange.

PINNING - SOT468A

PIN	DESCRIPTION
1	collector
2	base
3	emitter; connected to flange

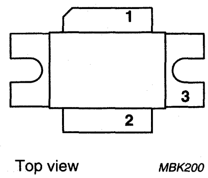


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	2000	26	60	≥8.5	≥40	–
2-tone, class-AB	f_1 = 2000.0; f_2 = 2000.1	26	60 (PEP)	≥9	≥33	≤–30

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	10	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	270	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 270 W; T_{mb} = 25 °C; note 1	0.65	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.25	K/W

Note

1. Thermal resistance is determined under specified RF operating conditions.

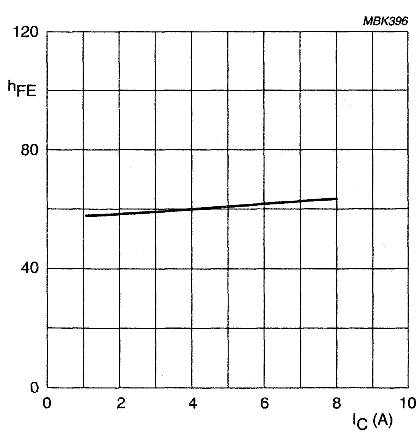
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 40 mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 120 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 40 mA	3	–	–	V
I_{CES}	collector leakage current	V_{CE} = 26 V; V_{BE} = 0	–	–	8	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 4 A	45	–	100	
C_c	collector capacitance	V_{CB} = 26 V; $I_E = i_e$ = 0; f = 1 MHz; note 1	–	72	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	41	–	pF

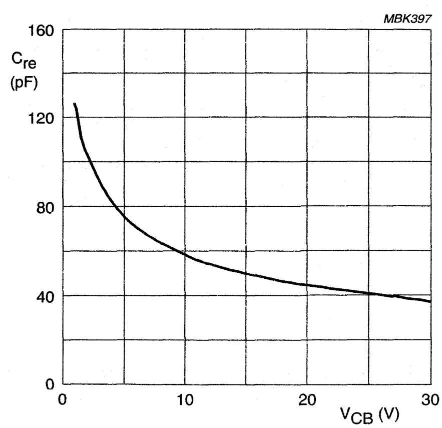
Note

1. Capacitance of die only.



V_{CE} = 10 V.

Fig.2 DC current gain as a function of collector current; typical values.



f = 1 MHz.

Fig.3 Feedback capacitance as a function of collector-base voltage; typical values.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter test circuit.

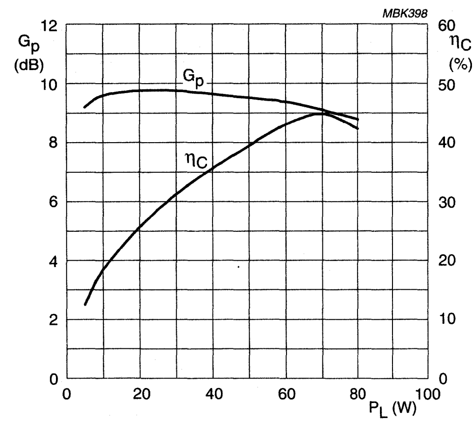
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	2000	26	300	60	≥8.5	≥40	–
2-tone, class-AB	f_1 = 2000.0 f_2 = 2000.1	26	300	60 (PEP)	≥9	≥33	≤–30
CDMA, class-AB	2000	26	500	12.5	typ. 9	typ. 22	≤–46(1)

Note

1. CDMA test signal with peak to average ratio of 11.9 dB. Adjacent Channel Power (ACP) is measured at ±885 kHz offset from the centre of the channel (2000 MHz) using a spectrum analyzer with the resolution set to 30 kHz.

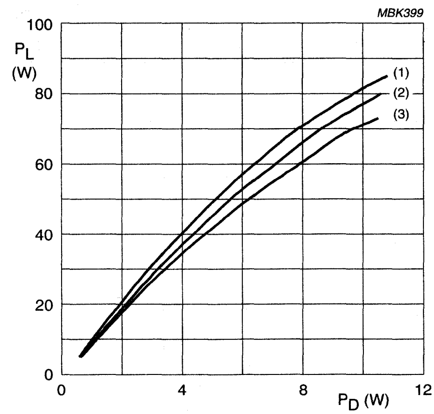
Ruggedness in class-AB operation

The BLV2047 is capable of withstanding a load mismatch corresponding to VSWR = 3 : 1 through all phases under the following conditions: f_1 = 2000.0 MHz; f_2 = 2000.1 MHz; V_{CE} = 26 V; I_{CQ} = 300 mA; P_L = 60 W (PEP); T_{mb} = 25 °C.



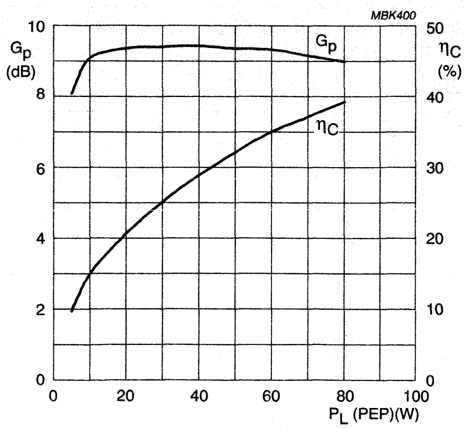
V_{CE} = 26 V; I_{CQ} = 300 mA; f = 2000 MHz.

Fig.4 Power gain and collector efficiency as a function of load power; typical values.



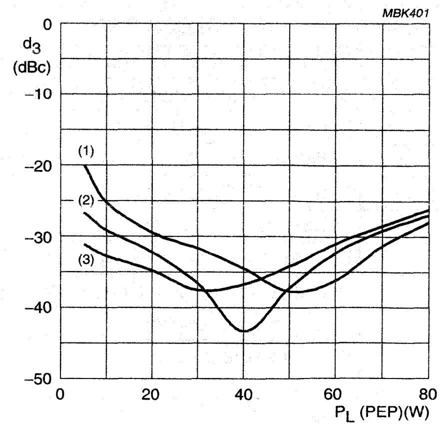
I_{CQ} = 300 mA; f = 2000 MHz.
(1) V_{CE} = 28 V.
(2) V_{CE} = 26 V.
(3) V_{CE} = 24 V.

Fig.5 Load power as a function of drive power; typical values.



V_{CE} = 26 V; I_{CQ} = 300 mA; f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.6 Power gain and collector efficiency as functions of peak envelope load power; typical values.



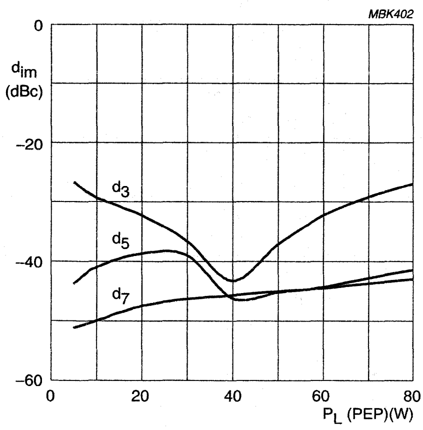
V_{CE} = 26 V; f_1 = 2000 MHz; f_2 = 2000.1 MHz.

(1) I_{CQ} = 100 mA.

(2) I_{CQ} = 300 mA.

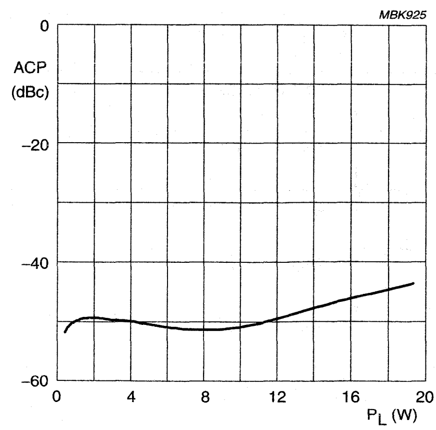
(3) I_{CQ} = 500 mA.

Fig.7 Intermodulation products as a function of peak envelope load power; typical values.



V_{CE} = 26 V; I_{CQ} = 300 mA; f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.8 Intermodulation products as a function of peak envelope load power; typical values.



V_{CE} = 26 V; I_{CQ} = 500 mA.
Measured at 885 kHz offset with 30 kHz bandwidth.
CDMA test signal with 11.9 dB peak to average ratio.

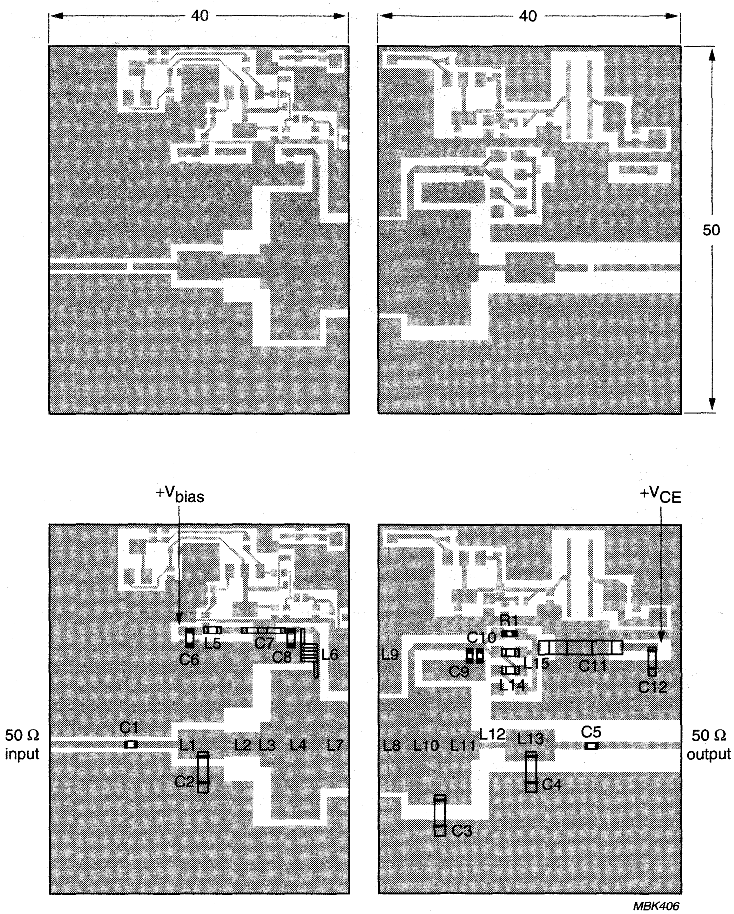
Fig.9 Adjacent channel power as a function of load power; typical values.

List of components (see Figs 10 and 11)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8	multilayer ceramic chip capacitor; note 1	22 pF		
C2	Tekelec variable capacitor; type 37291	0.8 to 8 pF		
C3, C4	Tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C5	multilayer ceramic chip capacitor, note 2	22 pF		
C6, C12	tantalum SMD capacitor	10 μF, 35 V		
C7	feedthrough capacitor	1.5 nF		
C9	multilayer ceramic chip capacitor, note 3	13 pF		
C10	multilayer ceramic chip capacitor, note 3	10 nF		
C11	feedthrough capacitor	3.3 nF		
L1	stripline; note 4	18.8 Ω	length 6.1 mm; width 3.9 mm	
L2	stripline; note 4	21.9 Ω	length 5 mm; width 3.2 mm	
L3	stripline; note 4	13 Ω	length 1.4 mm; width 6.1 mm	
L4	stripline; note 4	4.5 Ω	length 6.6 mm; width 20.2 mm	
L5, L14, L15	grade 4B1 ferroxcube chip-bead			4322 020 34420
L6	4 turns enamelled 1 mm copper wire	30 nH	int.dia. 3 mm; length 7 mm	
L7	stripline; note 4	7.3 Ω	length 4 mm; width 11.8 mm	
L8	stripline; note 4	6.8 Ω	length 4 mm; width 12.8 mm	
L9	stripline; note 4	43.7 Ω	length 12.5 mm; width 1 mm	
L10	stripline; note 4	5.6 Ω	length 8.5 mm; width 15.9 mm	
L11	stripline; note 4	18.8 Ω	length 1 mm; width 3.9 mm	
L12	stripline; note 4	53.3 Ω	length 3.4 mm; width 0.8 mm	
L13	stripline; note 4	17.4 Ω	length 6.5 mm; width 4.3 mm	
R1	standard chip resistor	10 Ω	type 0603	

Notes

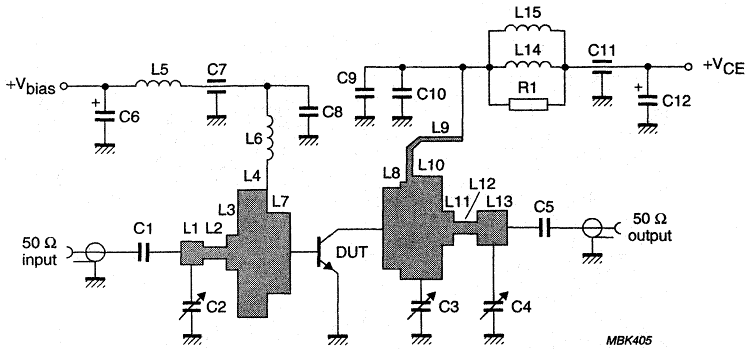
1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 175B or capacitor of same quality.
3. American Technical Ceramics type 100B or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15); thickness 0.64 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad Teflon board, the other side is unetched and serves as a ground plane.
Earth connections from the component side to the ground plane are made by through metallization.

Fig.10 Component layout for 2000 MHz class-AB test circuit.

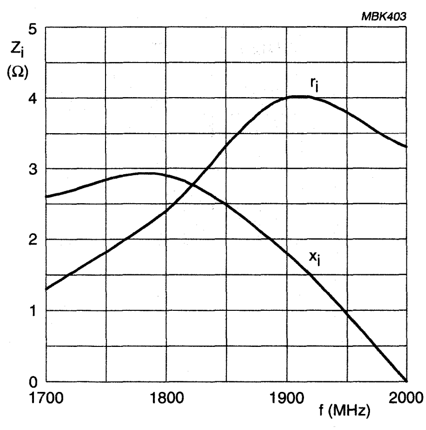


For CDMA measurements:
Replace L5, C7 and C11 by a bridging wire.
Change L6 from 6 turns to 2 turns (same diameter).
Add 4.7 μF, 50 V tantalum capacitor to C12.
Add 100 pF ATC type 100A capacitor to C8.

Fig.11 Class-AB test circuit for 2000 MHz.

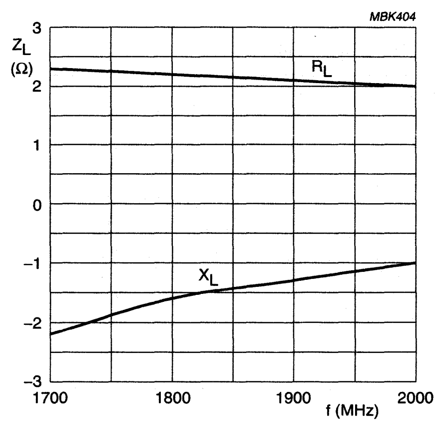
Scattering parameters: V_{CE} = 26 V; I_C = 1 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
1500	0.982	173.3	0.169	131.8	0.031	106.4	0.967	174.6
1600	0.970	172.0	0.227	126.1	0.035	96.0	0.953	174.0
1700	0.947	170.4	0.349	114.3	0.037	93.3	0.929	173.8
1800	0.870	167.5	0.633	85.8	0.036	74.7	0.879	174.2
1850	0.779	169.9	0.838	59.5	0.034	60.4	0.845	178.0
1900	0.775	179.3	0.833	22.7	0.018	47.4	0.902	−177.4
1950	0.863	−178.0	0.644	−6.9	0.011	103.7	0.967	−178.7
2000	0.913	−179.4	0.456	−24.5	0.018	121.2	0.990	179.3
2100	0.950	178.0	0.285	−40.8	0.028	114.7	0.995	176.9
2200	0.955	176.4	0.190	−54.0	0.031	115.2	0.987	175.5
2300	0.955	175.0	0.145	−53.6	0.034	114.7	0.983	175.0
2400	0.948	173.7	0.162	−60.4	0.036	116.7	0.975	174.4
2500	0.937	172.4	0.143	−84.2	0.038	116.8	0.973	173.9



V_{CE} = 26 V; I_{CQ} = 300 mA; P_L = 60 W; T_{mb} = 25 °C.

Fig.12 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 300 mA; P_L = 60 W; T_{mb} = 25 °C.

Fig.13 Load impedance as a function of frequency (series components); typical values.

UHF linear power transistor — BLW32

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in linear **u.h.f. amplifiers** for television transmitters and transposers. The **excellent d.c. dissipation properties** for class-A operation are obtained by means of diffused emitter ballasting resistors and a multi-base structure, providing an optimum temperature profile on the crystal area. The combination of optimum thermal design and the application of **gold sandwich metallization** realizes excellent reliability properties.

The transistor has a ¼" capstan envelope with ceramic cap.

QUICK REFERENCE DATA

R.F. performance

MODE OF OPERATION	f_{vision} MHz	V_{CE} V	I_C mA	T_h °C	d_{im} (1) dB	$P_{o\ sync}$ (1) W	G_p dB
class-A; linear amplifier	860	25	150	70	−60	> 0,5	> 11
	860	25	150	25	−60	typ. 0,63	typ. 12,2

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

PIN CONFIGURATION

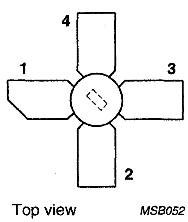


Fig.1 Simplified outline. SOT122A.

PINNING - SOT122A.

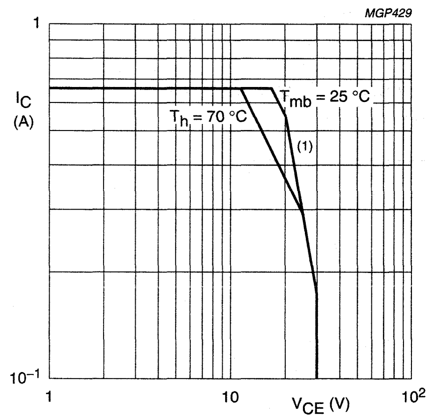
PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage				
(peak value); $V_{BE} = 0$	V_{CESM}	max.	50	V
open base	V_{CEO}	max.	30	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current				
d.c. or average	I_C	max.	650	mA
(peak value); f > 1 MHz	I_{CM}	max.	1000	mA
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	10,8	W
Storage temperature	T_{stg}		−65 to +150	°C
Operating junction temperature	T_j	max.	200	°C



(1) Second breakdown limit (independent of temperature).

Fig.2 D.C. SOAR.

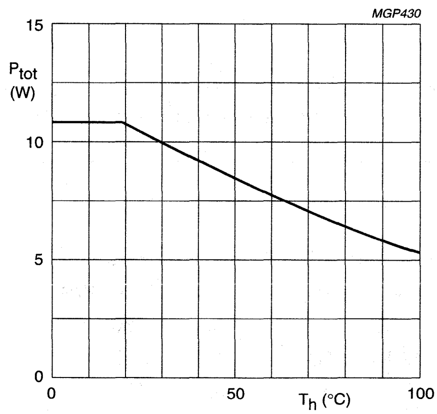


Fig.3 Power derating curve vs. temperature.

THERMAL RESISTANCE (see Fig.4)

From junction to mounting base				
(dissipation = 3,75 W; T_{mb} = 72,3 °C; i.e. T_h = 70 °C)	$R_{th\ j\text{-}mb}$	=	15,0	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,6	K/W

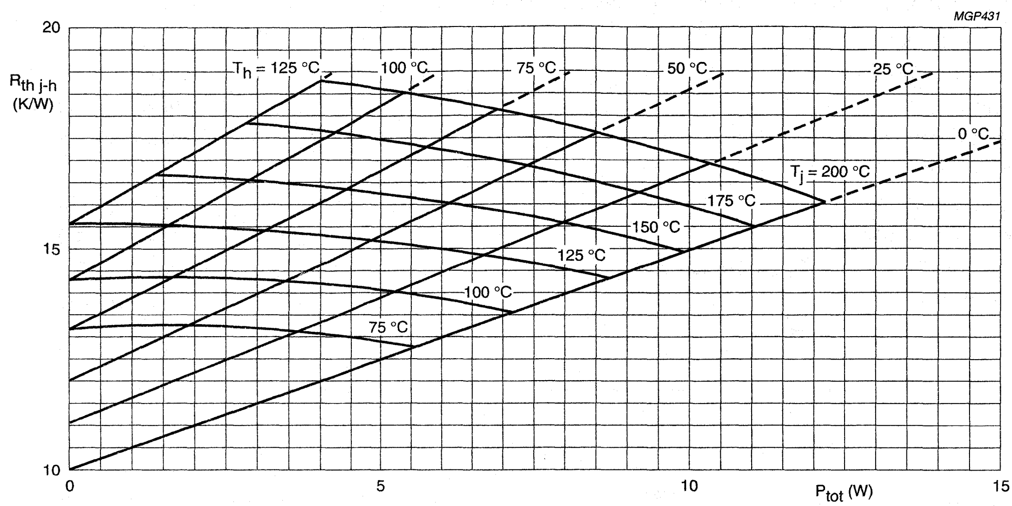


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb-h}$ = 0,6 K/W.)

Example

Nominal class-A operation: V_{CE} = 25 V; I_C = 150 mA; T_h = 70 °C.

Fig.4 shows:	$R_{th\ j-h}$	max.	15,6	K/W
	T_j	max.	130	°C
Typical device:	$R_{th\ j-h}$	typ.	13,5	K/W
	T_j	typ.	120	°C

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 2 mA	$V_{(BR)CES}$	>	50	V
open base; I_C = 15 mA	$V_{(BR)CEO}$	>	30	V
Emitter-base breakdown voltage				
open collector; I_E = 1 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 30 V	I_{CES}	<	0,5	mA
V_{BE} = 0; V_{CE} = 30 V; T_j = 175 °C	I_{CES}	<	1,2	mA
D.C. current gain (1)				
I_C = 150 mA; V_{CE} = 25 V	h_{FE}	> typ.	20 40	
I_C = 150 mA; V_{CE} = 25 V; T_j = 175 °C	h_{FE}	<	120	
Collector-emitter saturation voltage (1)				
I_C = 300 mA; I_B = 30 mA	V_{CEsat}	typ.	500	mV
Transition frequency at f = 500 MHz (2)				
$-I_E$ = 150 mA; V_{CB} = 25 V	f_T	typ.	3,5	GHz
$-I_E$ = 300 mA; V_{CB} = 25 V	f_T	typ.	3,4	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ.	3,7	pF
Feedback capacitance at f = 1 MHz				
I_C = 10 mA; V_{CE} = 25 V	C_{re}	typ.	1,9	pF
Collector-stud capacitance	C_{cs}	typ.	1,2	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0{,}01$.

UHF linear power transistor BLW32

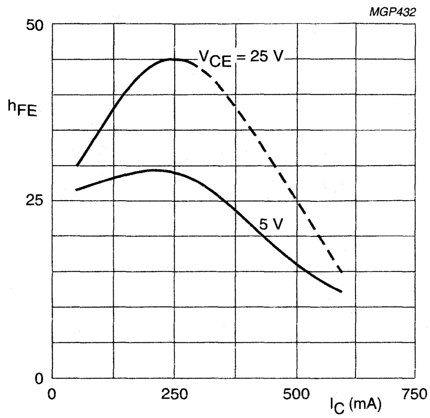


Fig.5 Typical values; T_j = 25 °C.

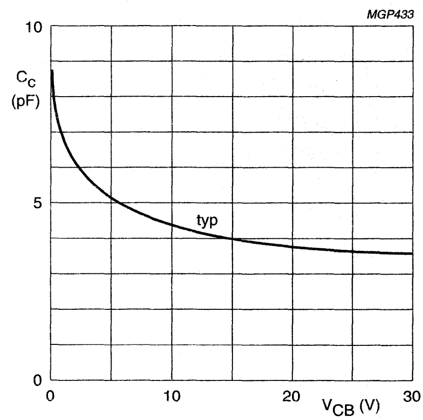


Fig.6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

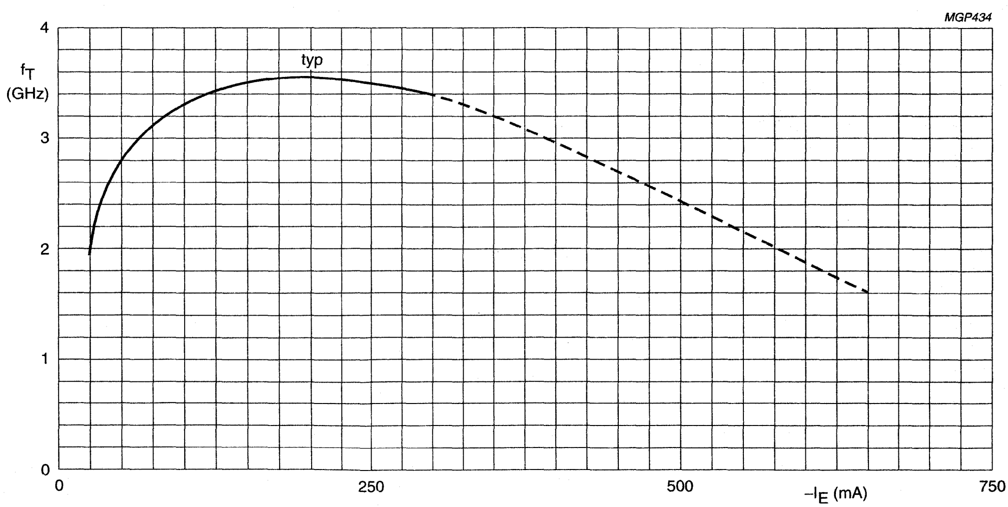


Fig.7 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C.

APPLICATION INFORMATION

f_{vision} (MHz)	V_{CE} (V)	I_C (mA)	T_h (°C)	d_{im}(dB) (1)	$P_{o\ sync}$ (W) (1)	G_p (dB)
860	25	150	70	−60	> 0,5	> 11
860	25	150	70	−60	typ. 0,58	typ. 12,2
860	25	150	25	−60	typ. 0,63	typ. 12,2

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

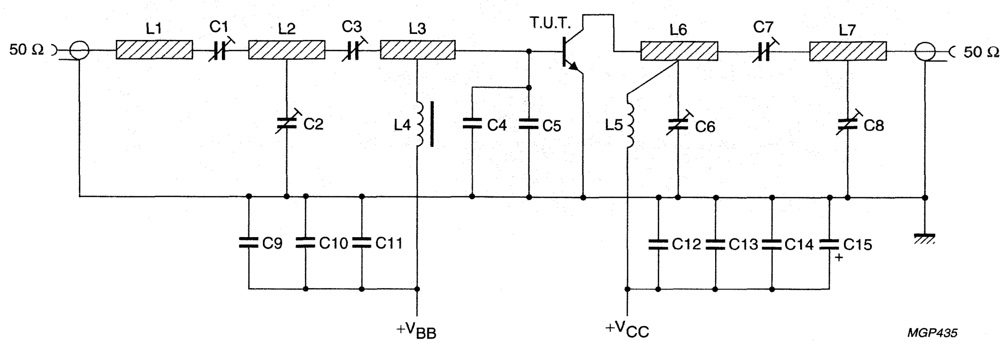


Fig.8 Test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C7 = 2 to 18 pF film dielectric trimmer (cat. no. 2222 809 05003)

C2 = C6 = C8 = 1 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001) placed 24 mm, 17 mm and 45 mm respectively from transistor edge

C3 = 1,8 to 10 pF film dielectric trimmer (cat. no. 2222 809 05002)

C4 = C5 = 3 pF multilayer chip capacitor (ATC 100A-3RO-C-PX-50)

C9 = C12 = 1 nF chip capacitor

C10 = 100 nF polyester capacitor

C11 = C13 = 470 nF polyester capacitor

C14 = 10 nF polyester capacitor

C15 = 3,3 μF/40 V solid aluminium electrolytic capacitor

L1 = stripline (5,0 mm × 4,5 mm)

L2 = stripline (13,2 mm × 4,5 mm)

L3 = stripline (15,0 mm × 4,5 mm)

L4 = micro choke 0,47 μH (cat. no. 4322 057 04770)

L5 = 4 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 × 4 mm

L6 = stripline (37,0 mm × 4,5 mm)

L7 = stripline (13,5 mm × 4,5 mm)

L1; L2; L3; L6 and L7 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ε_r = 2,74); thickness 1/16".

Component layout and printed-circuit board for 860 MHz test circuit are shown in Fig.9. For bias circuit see Fig.10.

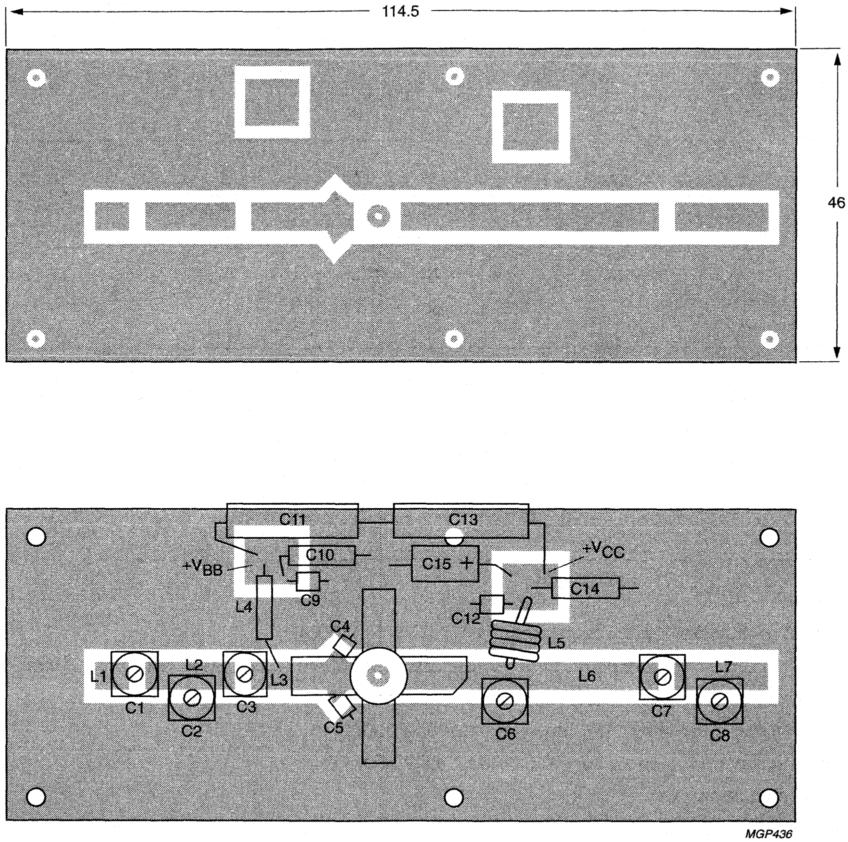


Fig.9 Component layout and printed-circuit board for 860 MHz test circuit.

The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

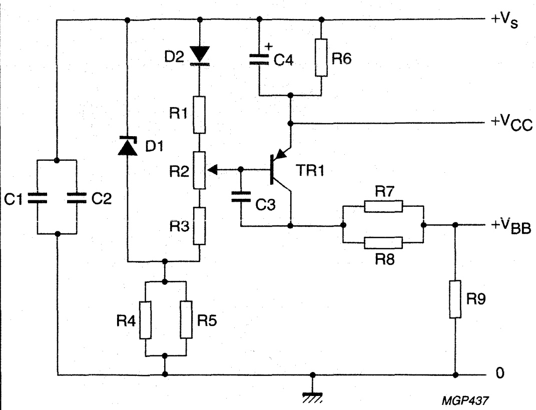


Fig.10 Bias circuit for class-A amplifier at f_{vision} = 860 MHz.

List of components:

C1 = 100 pF ceramic capacitor
C2 = C3 = 100 nF polyester capacitor
C4 = 10 µF/25 V solid aluminium electrolytic capacitor
R1 = 150 Ω carbon resistor (0,25 W)
R2 = 100 Ω preset potentiometer (0,1 W)
R3 = 82 Ω carbon resistor (0,25 W)
R4 = R5 = 2,2 kΩ carbon resistor (0,25 W)
R6 = 12 Ω carbon resistor (0,5 W)
R7 = R8 = 820 Ω carbon resistor (0,25 W)
R9 = 33 Ω carbon resistor (0,25 W)
D1 = BZY88-C3V3
D2 = BY206
TR1 = BD136

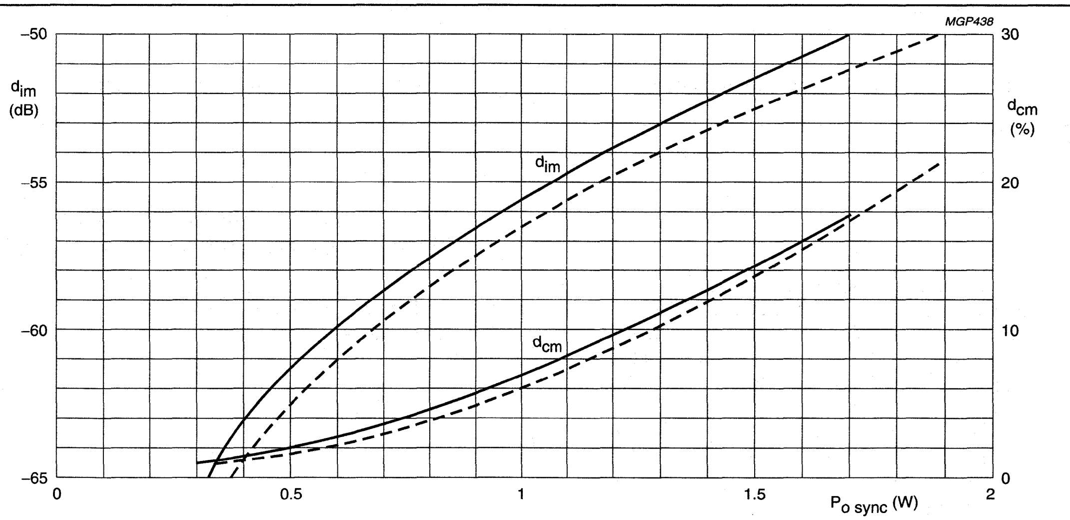
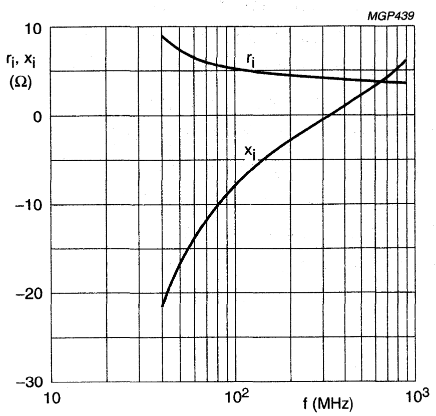


Fig.11 Intermodulation distortion (d_{im})(1.) and cross-modulation distortion (d_{cm})(2.) as a function of output power. Typical values; V_{CE} = 25 V; I_C = 150 mA; f_{vision} = 860 MHz; – – – T_h = 25 °C; —— T_h = 70 °C.

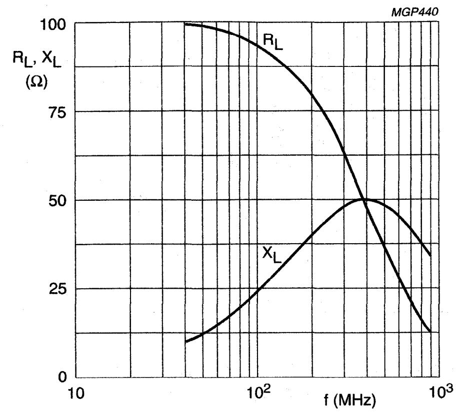
Information for wideband application from 470 to 860 MHz available on request.

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
   Intermodulation distortion of input signal ≤ −75 dB.
2. Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level.
   Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB.



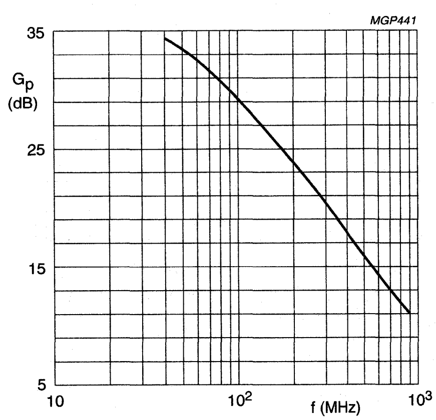
Typical values; V_{CE} = 25 V;
I_C = 150 mA; T_h = 70 °C

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 25 V;
I_C = 150 mA; T_h = 70 °C

Fig.13 Load impedance (series components).



Typical values; V_{CE} = 25 V;
I_C = 150 mA; T_h = 70 °C

Fig.14

Ruggedness

The BLW32 is capable of withstanding a load mismatch (VSWR = 50 through all phases) under the following conditions:

f = 860 MHz; V_{CE} = 25 V; I_C = 150 mA;
T_h = 70 °C and P_L = 1 W.

UHF linear power transistor | BLW33

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in **linear u.h.f. amplifiers** for television transmitters and transposers. The **excellent d.c. dissipation properties** for class-A operation are obtained by means of diffused emitter ballasting resistors and a multi-base structure, providing an optimum temperature profile on the crystal area. The combination of optimum thermal design and the application of **gold sandwich metallization** realizes excellent reliability properties.

The transistor has a ¼" capstan envelope with ceramic cap.

QUICK REFERENCE DATA

R.F. performance

MODE OF OPERATION	f_{vision} MHz	V_{CE} V	I_C mA	T_h °C	d_{im} (1) dB	$P_{o\ sync}$ (1) W	G_p dB
class-A; linear amplifier	860	25	300	70	−60	> 1,0	> 10,0
	860	25	300	25	−60	typ. 1,15	typ. 10,5

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

PIN CONFIGURATION

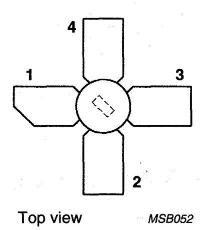


Fig.1 Simplified outline. SOT122A.

PINNING - SOT122A.

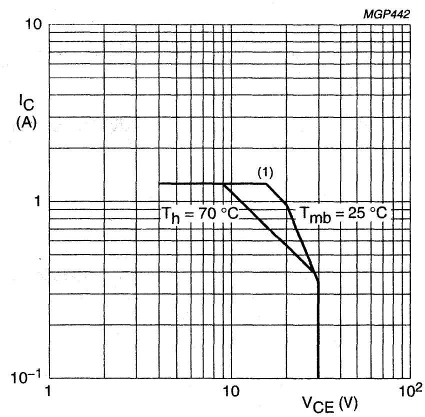
PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage				
(peak value); $V_{BE} = 0$	V_{CESM}	max.	50	V
open base	V_{CEO}	max.	30	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current				
d.c. or average	I_C	max.	1,25	A
(peak value); f > 1 MHz	I_{CM}	max.	1,9	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	19,3	W
Storage temperature	T_{stg}		−65 to +150	°C
Operating junction temperature	T_j	max.	200	°C



(1) Second breakdown limit (independent of temperature).

Fig.2 D.C. SOAR.

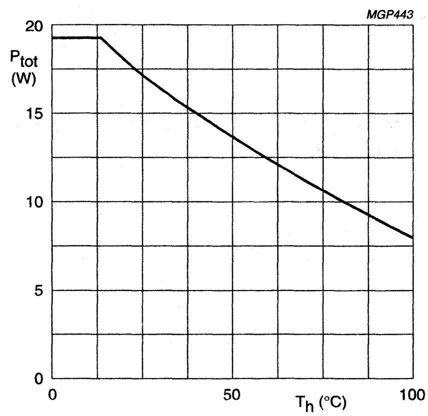


Fig.3 Power derating curve vs. temperature.

THERMAL RESISTANCE (see Fig.4)

From junction to mounting base				
(dissipation = 7,5 W; T_{mb} = 74,5 °C; i.e. T_h = 70 °C)	$R_{th\ j\text{-}mb}$	=	10,1	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,6	K/W

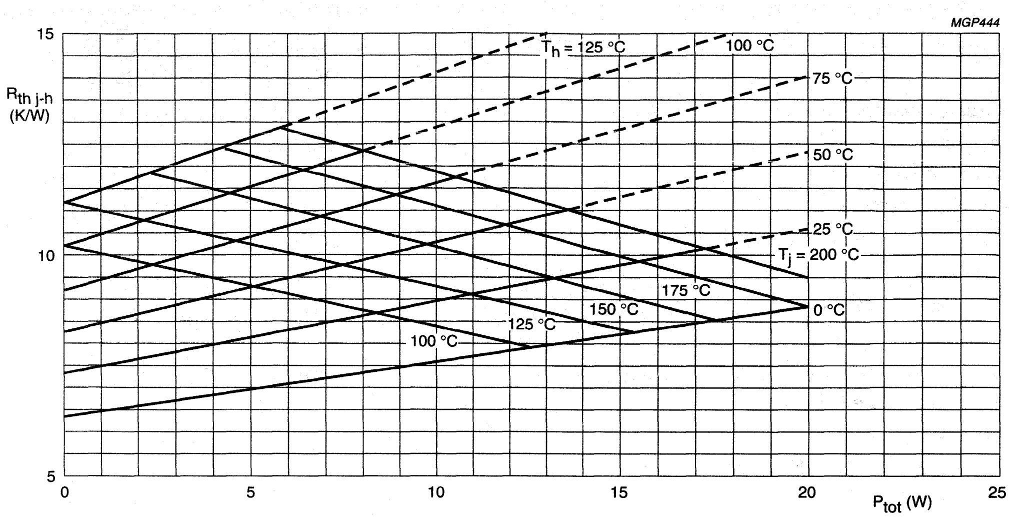


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb\text{-}h}$ = 0,6 K/W.)

Example

Nominal class-A operation: V_{CE} = 25 V; I_C = 300 mA; T_h = 70 °C.

Fig.4 shows:	$R_{th\ j-h}$	max.	10,7	K/W
	T_j	max.	150	°C
Typical device:	$R_{th\ j-h}$	typ.	8,25	K/W
	T_j	typ.	132	°C

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 4 mA	$V_{(BR)CES}$	>	50	V
open base; I_C = 30 mA	$V_{(BR)CEO}$	>	30	V
Emitter-base breakdown voltage				
open collector; I_E = 2 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 30 V	I_{CES}	<	1,0	mA
V_{BE} = 0; V_{CE} = 30 V; T_j = 175 °C	I_{CES}	<	2,5	mA
D.C. current gain				
I_C = 300 mA; V_{CE} = 25 V	h_{FE}	>	20	
		typ.	40	
I_C = 300 mA; V_{CE} = 25 V; T_j = 175 °C	h_{FE}	<	120	
Collector-emitter saturation voltage (1)				
I_C = 600 mA; I_B = 60 mA	V_{CEsat}	typ.	450	mV
Transition frequency at f = 500 MHz (2)				
$-I_E$ = 300 mA; V_{CB} = 25 V	f_T	typ.	3,4	GHz
$-I_E$ = 600 mA; V_{CB} = 25 V	f_T	typ.	3,1	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ.	6,6	pF
Feedback capacitance at f = 1 MHz				
I_C = 20 mA; V_{CE} = 25 V	C_{re}	typ.	3,5	pF
Collector-stud capacitance	C_{cs}	typ.	1,2	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0{,}01$.

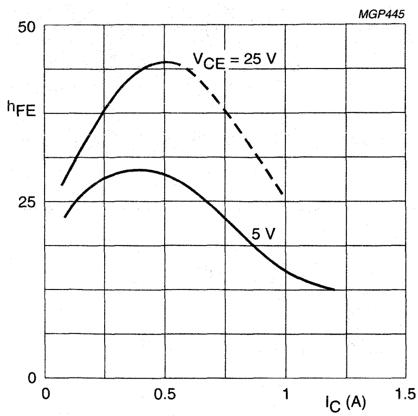


Fig.5 Typical values; T_j = 25 °C.

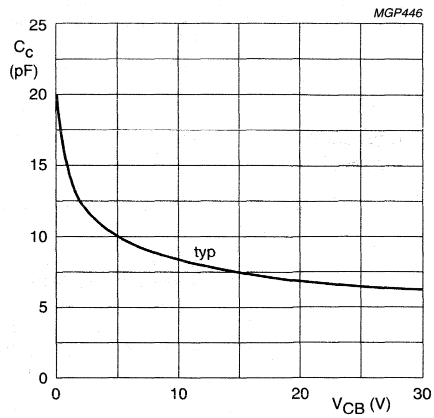


Fig.6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

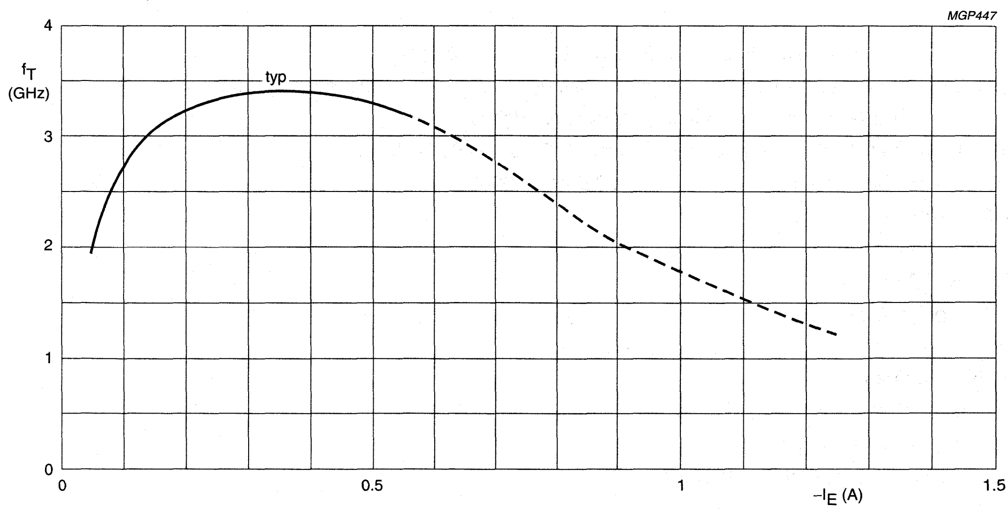


Fig.7 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C.

APPLICATION INFORMATION

f_{vision} (MHz)	V_{CE} (V)	I_C (mA)	T_h (°C)	d_{im} (dB) (1)	$P_{o\ sync}$ (W) (1)	G_P (dB)
860	25	300	70	−60	> 1,0	> 10
860	25	300	70	−60	typ. 1,07	typ. 10,5
860	25	300	25	−60	typ. 1,15	typ. 10,5

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

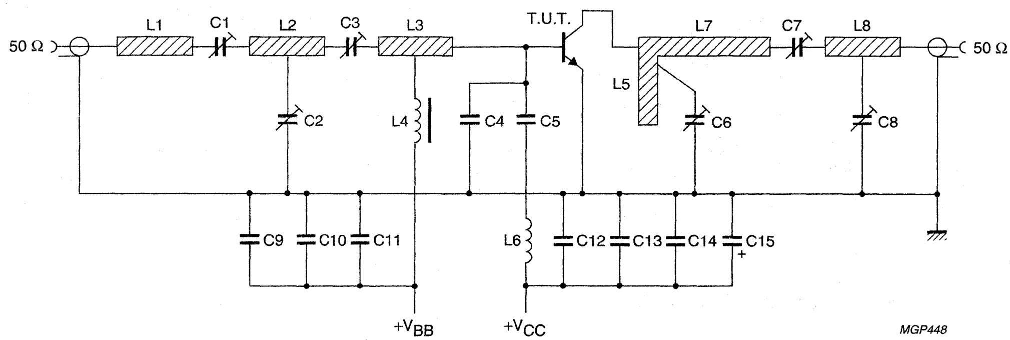


Fig.8 Test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C3 = 2 to 18 pF film dielectric trimmer (cat. no. 2222 809 05003)

C2 = C6 = C8 = 1 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001) placed 24 mm, 8 mm and 46 mm respectively from transistor edge

C4 = C5 = 4,3 pF multilayer ceramic chip capacitor (ATC 100A-4R3-C-PX-50)

C7 = 1,8 to 10 pF film dielectric trimmer (cat. no. 2222 809 05002)

C9 = C12 = 1 nF chip capacitor

C10 = 100 nF polyester capacitor

C11 = C13 = 470 nF polyester capacitor

C14 = 10 nF polyester capacitor

C15 = 3,3 µF/40 F solid aluminium electrolytic capacitor

L1 = stripline (5,2 mm × 4,5 mm)

L2 = stripline (13,2 mm × 4,5 mm)

L3 = stripline (15,0 mm × 4,5 mm)

L4 = micro choke 0,47 µH (cat. no. 4322 057 04770)

L5 = stripline (see Fig.9 printed-circuit board layout)

L6 = 4 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 × 4 mm

L7 = stripline (37,0 mm × 4,5 mm)

L8 = stripline (13,5 mm × 4,5 mm)

L1; L2; L3; L5; L7 and L8 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ε_r = 2,74); thickness 1/16".

For bias circuit see Fig.10.

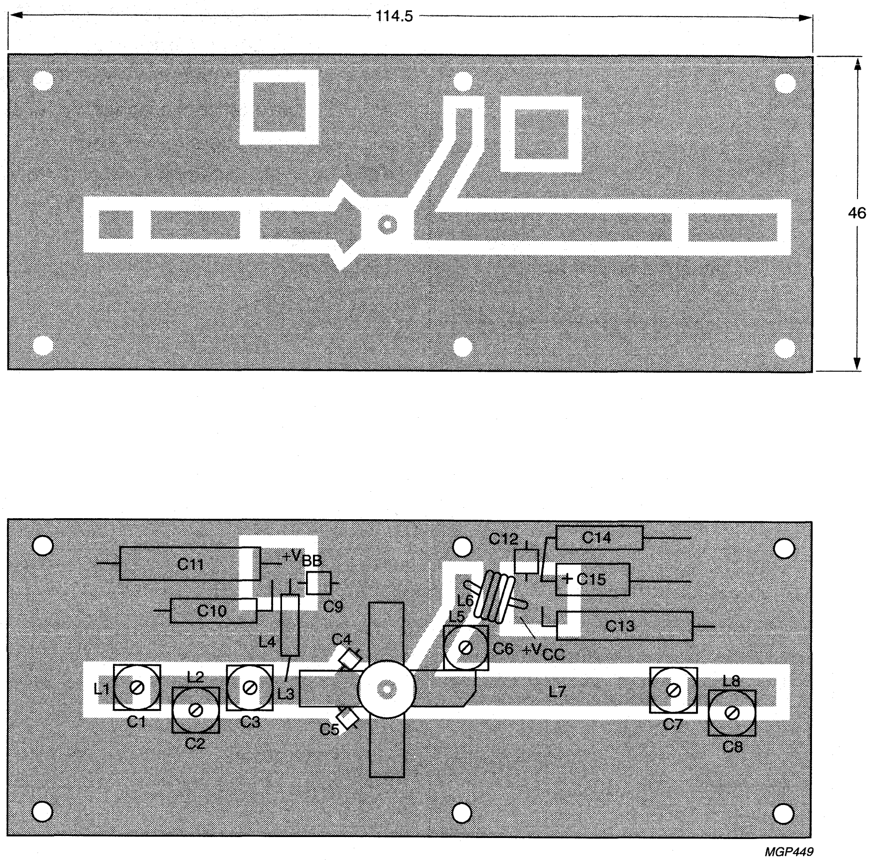


Fig.9 Component layout and printed-circuit board for 860 MHz test circuit.

The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

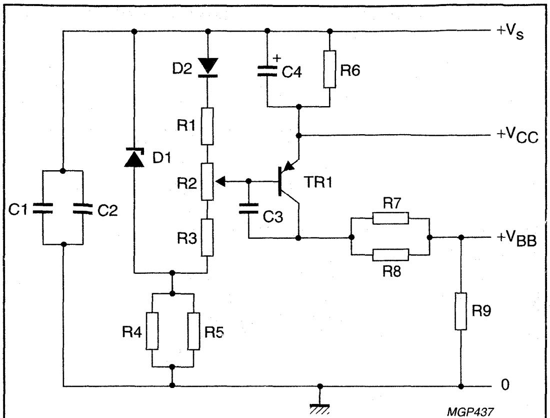


Fig.10 Bias circuit for class-A amplifier at f_{vision} = 860 MHz.

List of components:

C1 = 100 pF ceramic capacitor
C2 = C3 = 100 nF polyester capacitor
C4 = 10 μF/25 V solid aluminium electrolytic capacitor
R1 = 150 Ω carbon resistor (0,25 W)
R2 = 100 Ω preset potentiometer (0,1 W)
R3 = 82 Ω carbon resistor (0,25 W)
R4 = R5 = 2,2 kΩ carbon resistor (0,25 W)
R6 = 6 Ω; parallel connection of 2 × 12 Ω carbon resistors (0,5 W each)
R7 = R8 = 820 Ω carbon resistor (0,25 W)
R9 = 33 Ω carbon resistor (0,25 W)
D1 = BZY88-C3V3
D2 = BY206
TR1 = BD136

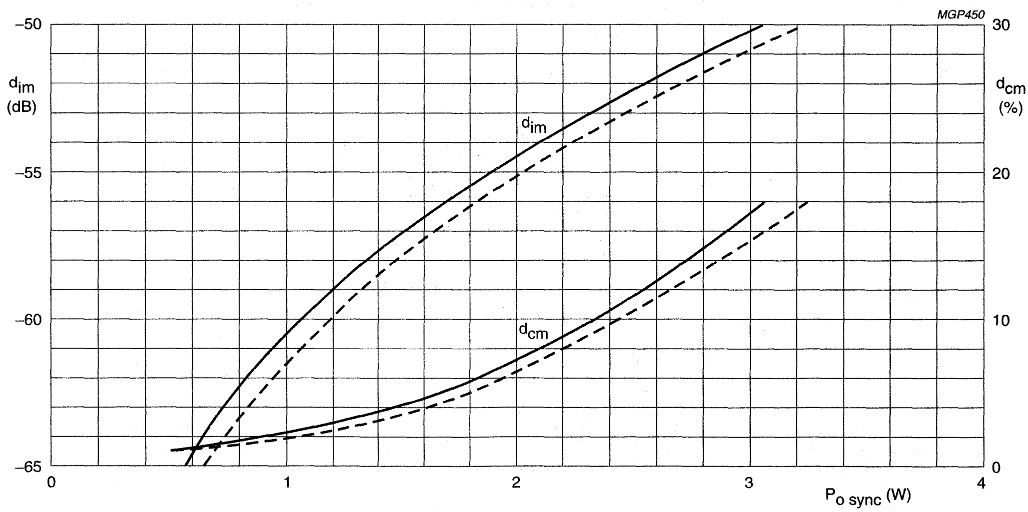
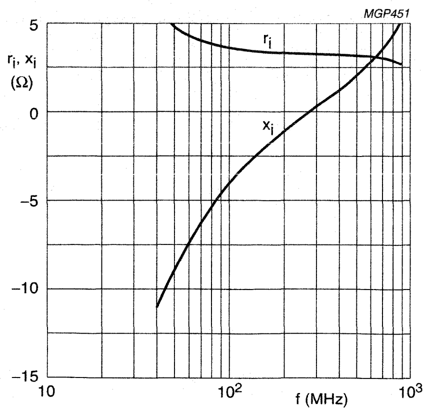


Fig.11 Intermodulation distortion (d_{im})(1.) and cross-modulation distortion (d_{cm})(2.) as a function of output power. Typical values; V_{CE} = 25 V; I_C = 300 mA; f_{vision} = 860 MHz; – – – T_h = 25 °C; —— T_h = 70 °C.

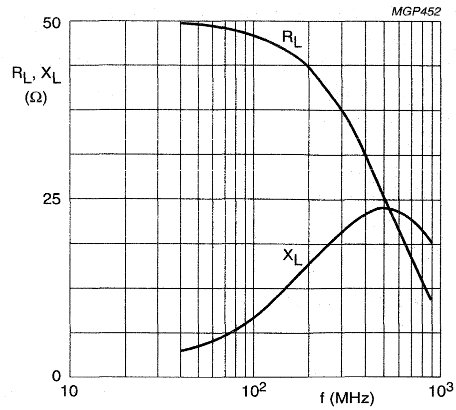
Information for wideband application from 470 to 860 MHz available on request.

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
   Intermodulation distortion of input signal ≤ −75 dB.
2. Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level.
   Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB.



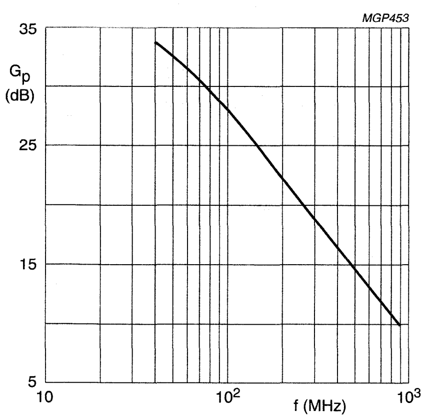
Typical values; V_{CE} = 25 V;
I_C = 300 mA; T_h = 70 °C.

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 25 V;
I_C = 300 mA; T_h = 70 °C.

Fig.13 Load impedance (series components).



Typical values; V_{CE} = 25 V;
I_C = 300 mA; T_h = 70 °C.

Fig.14

Ruggedness

The BLW33 is capable of withstanding a load mismatch (VSWR = 50 through all phases) under the following conditions:

f = 860 MHz; V_{CE} = 25 V; I_C = 300 mA;
T_h = 70 °C and P_L = 2 W.

UHF linear power transistor BLW34

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in **linear u.h.f. amplifiers** for television transmitters and transposers. The **excellent d.c. dissipation properties** for class-A operation are obtained by means of diffused emitter ballasting resistors and a multi-base structure, providing an optimum temperature profile on the crystal area. The combination of optimum thermal design and the application of **gold sandwich metallization** realizes excellent reliability properties.

The transistor has a ¼" capstan envelope with ceramic cap.

QUICK REFERENCE DATA

R.F. performance

MODE OF OPERATION	f_{vision} MHz	V_{CE} V	I_C mA	T_h °C	d_{im}(1) dB	$P_{o\ sync}$ (1) W	G_p dB
class-A; linear amplifier	860	25	600	70	−60	> 1,8	> 9
	860	25	600	25	−60	typ. 2,15	typ. 10,2

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

PIN CONFIGURATION

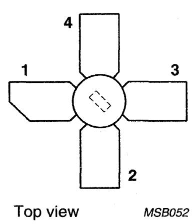


Fig.1 Simplified outline. SOT122A.

PINNING - SOT122A.

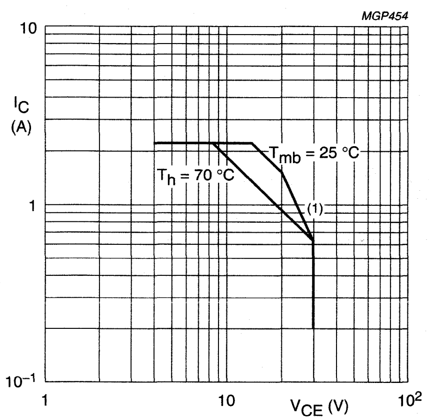
PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage				
(peak value); $V_{BE} = 0$	V_{CESM}	max.	50	V
open base	V_{CEO}	max.	30	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current				
d.c. or average	I_C	max.	2,25	A
(peak value); f > 1 MHz	I_{CM}	max.	3,5	A
Total power dissipation at T_{mb} = 25 °C	P_{tot}	max.	31	W
Storage temperature	T_{stg}		−65 to +150	°C
Operating junction temperature	T_j	max.	200	°C



(1) Second breakdown limit (independent of temperature).

Fig.2 D.C. SOAR.

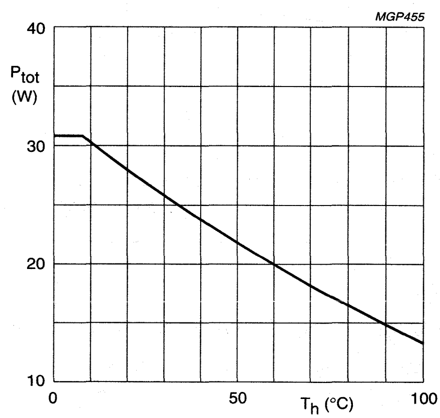


Fig.3 Power derating curve vs. temperature.

THERMAL RESISTANCE (see Fig.4)

From junction to mounting base				
(dissipation = 15 W; T_{mb} = 79 °C; i.e. T_h = 70 °C)	$R_{th\ j\text{-}mb}$	=	6,2	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,6	K/W

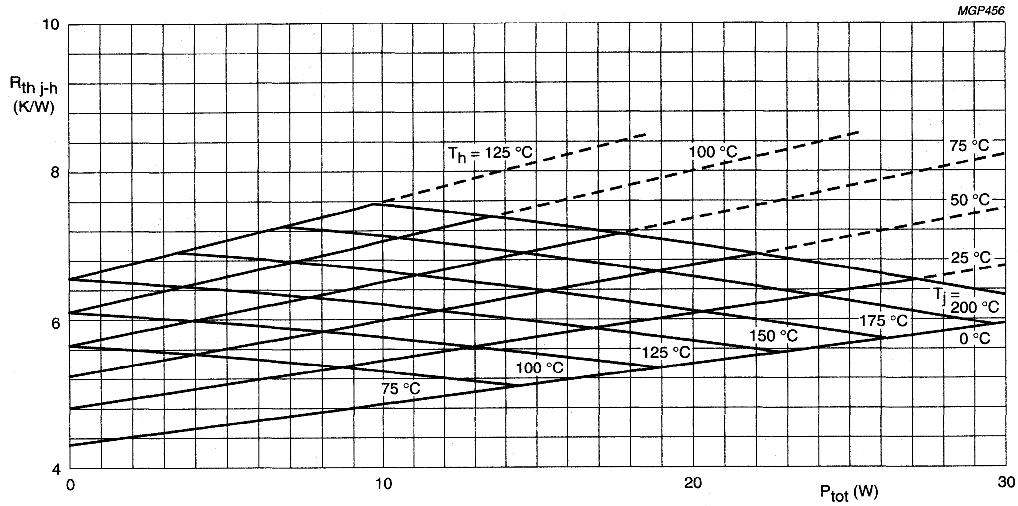


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb\text{-}h}$ = 0,6 K/W.)

Example

Nominal class-A operation: V_{CE} = 25 V; I_C = 600 mA; T_h = 70 °C.

Fig.4 shows:	$R_{th\ j\text{-}h}$	max.	6,75	K/W
	T_j	max.	170	°C
Typical device:	$R_{th\ j\text{-}h}$	typ.	5,45	K/W
	T_j	typ.	152	°C

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 8 mA	$V_{(BR)CES}$	>	50	V
open base; I_C = 60 mA	$V_{(BR)CEO}$	>	30	V
Emitter-base breakdown voltage				
open collector; I_E = 4 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 30 V	I_{CES}	<	2,0	mA
V_{BE} = 0; V_{CE} = 30 V; T_j = 175 °C	I_{CES}	<	5,0	mA
D.C. current gain				
I_C = 600 mA; V_{CE} = 25 V	h_{FE}	> typ.	20 40	
I_C = 600 mA; V_{CE} = 25 V; T_j = 175 °C	h_{FE}	<	120	
Collector-emitter saturation voltage (1)				
I_C = 1,2 A; I_B = 0,12 A	V_{CEsat}	typ.	450	mV
Transition frequency at f = 500 MHz (2)				
$-I_E$ = 0,6 A; V_{CB} = 25 V	f_T	typ.	3,3	GHz
$-I_E$ = 1,2 A; V_{CB} = 25 V	f_T	typ.	3,0	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ.	13,5	pF
Feedback capacitance at f = 1 MHz				
I_C = 40 mA; V_{CE} = 25 V	C_{re}	typ.	8,4	pF
Collector-stud capacitance	C_{cs}	typ.	1,2	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0,02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0,01$.

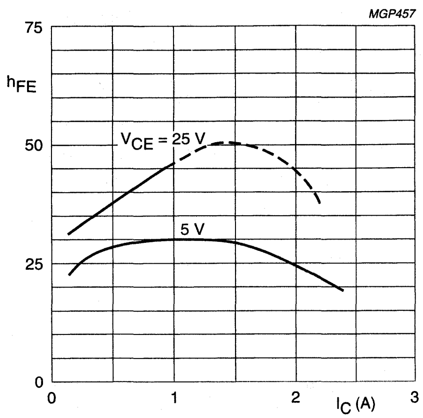


Fig.5 Typical values; T_j = 25 °C.

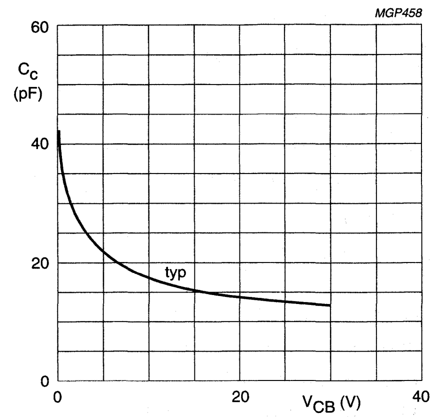


Fig.6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

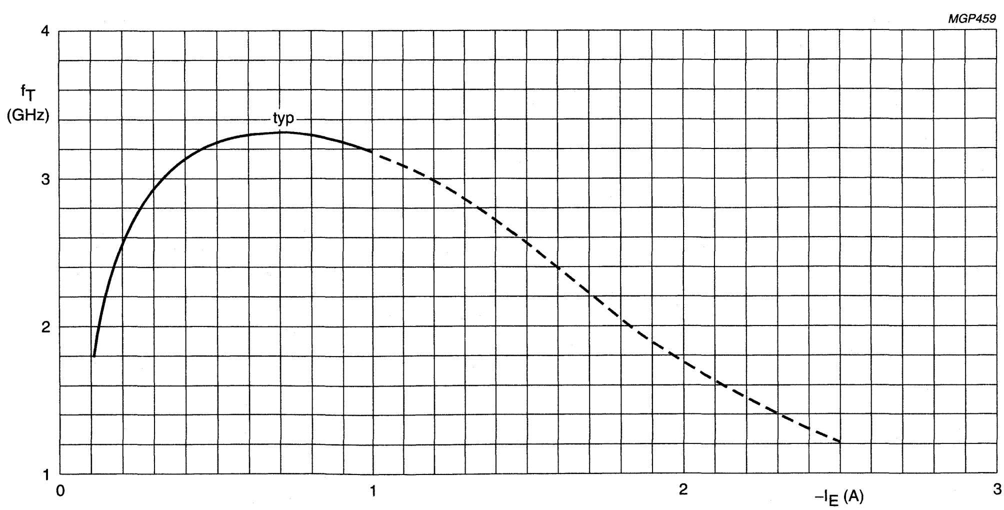


Fig.7 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C

UHF linear power transistor BLW34

APPLICATION INFORMATION

f_{vision} (MHz)	V_{CE} (V)	I_C (mA)	T_h (°C)	d_{im} (dB) (1)	$P_{o\ sync}$ (W) (1)	G_p (dB)
860	25	600	70	−60	> 1,8	> 9
860	25	600	70	−60	typ. 1,9	typ. 10,2
860	25	600	25	−60	typ. 2,15	typ. 10,2

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

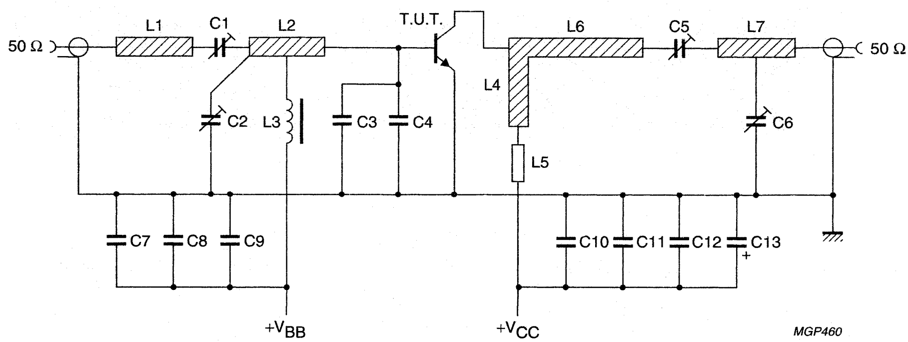


Fig.8 Test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C5 = 1,8 to 10 pF film dielectric trimmer (cat. no. 2222 809 05002)

C2 = C6 = 1 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001) placed 13,5 mm and 46 mm respectively from transistor edge

C3 = C4 = 2 pF multilayer ceramic chip capacitor (ATC 100A-2RO-C-PX-50)

C7 = C10 = 1 nF chip capacitor

C8 = 100 nF polyester capacitor

C9 = C12 = 470 nF polyester capacitor

C11 = 10 nF polyester capacitor

C13 = 3,3 μF/40 V solid aluminium electrolytic capacitor

L1 = stripline (9,2 mm × 7,0 mm)

L2 = stripline (14,2 mm × 7,0 mm)

L3 = micro choke 0,47 μH (cat. no. 4322 057 04770)

L4 = stripline (see Fig.9 printed-circuit board layout)

L5 = 34 mm straight Cu wire (1,0 mm); height above print 3,3 mm

L6 = stripline (41,0 mm × 7,0 mm)

L7 = stripline (8,7 mm × 7,0 mm)

L1; L2; L4; L6 and L7 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ε_r = 2,74); thickness 1/16".

Component layout and printed-circuit board for 860 MHz test circuit are shown in Fig.9. For bias circuit see Fig.10.

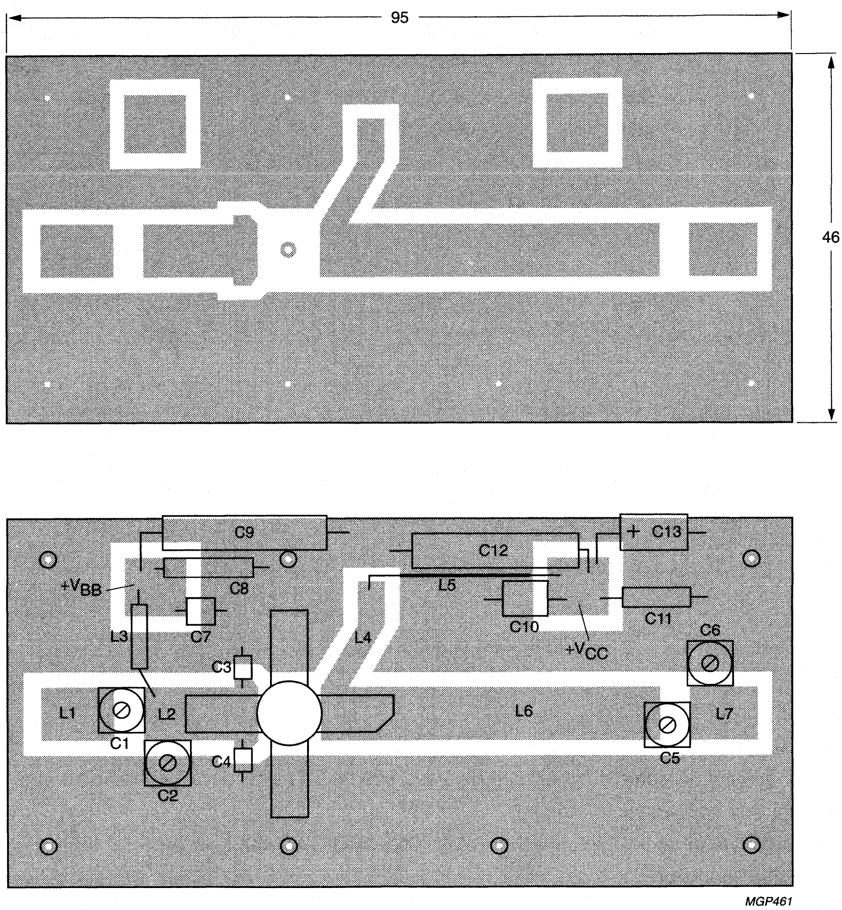


Fig.9 Component layout and printed-circuit board for 860 MHz test circuit.

The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

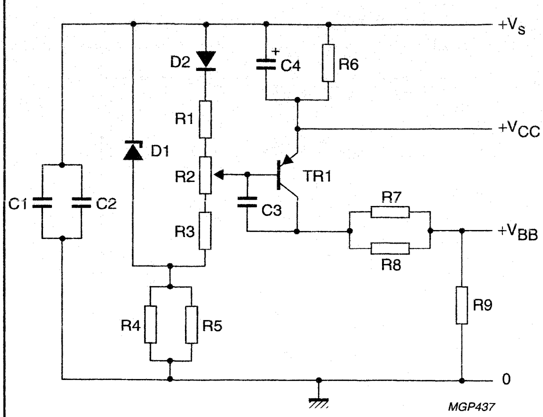


Fig.10 Bias circuit for class-A linear amplifier at f_{vision} = 860 MHz.

List of components:

C1 = 100 pF ceramic capacitor
C2 = C3 = 100 nF polyester capacitor
C4 = 10 µF/25 V solid aluminium electrolytic capacitor
R1 = 150 Ω carbon resistor (0,25 W)
R2 = 100 Ω preset potentiometer (0,1 W)
R3 = 82 Ω carbon resistor (0,25 W)
R4 = R5 = 2,2 kΩ carbon resistor (0,25 W)
R6 = 2,8 Ω; parallel connection of
2 × 5,6 Ω carbon resistors (0,5 W each)
R7 = R8 = 820 Ω carbon resistor (0,25 W)
R9 = 33 Ω carbon resistor (0,25 W)
D1 = BZY88-C3V3
D2 = BY206
TR1 = BD136

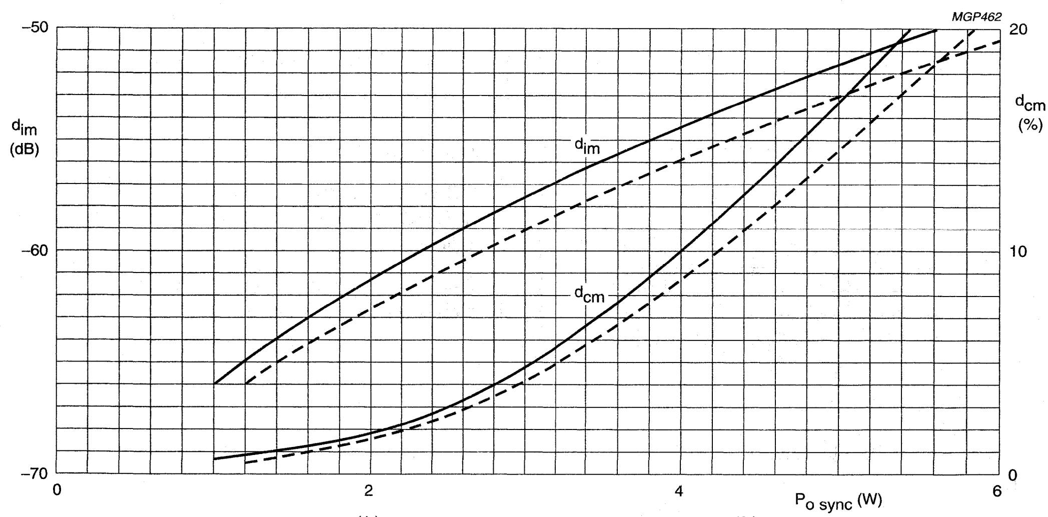
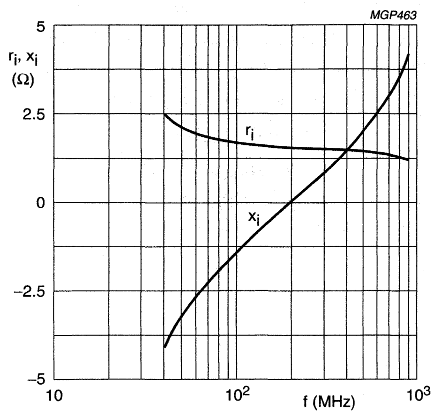


Fig.11 Intermodulation distortion $(d_{im})^{(1.)}$ and cross-modulation distortion $(d_{cm})^{(2.)}$ as a function of output power. Typical values; V_{CE} = 25 V; I_C = 600 mA; f_{vision} = 860 MHz; – – – T_h = 25 °C; —— T_h = 70 °C.

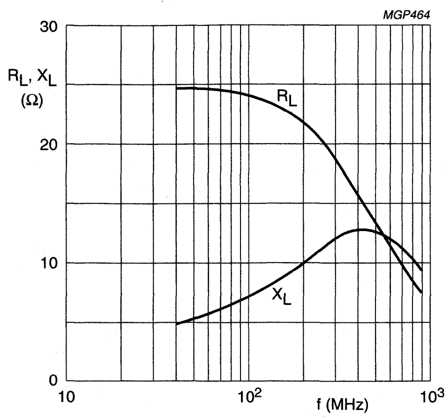
Information for wideband application from 470 to 860 MHz available on request.

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
   Intermodulation distortion of input signal ≤ −75 dB.
2. Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level.
   Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB.



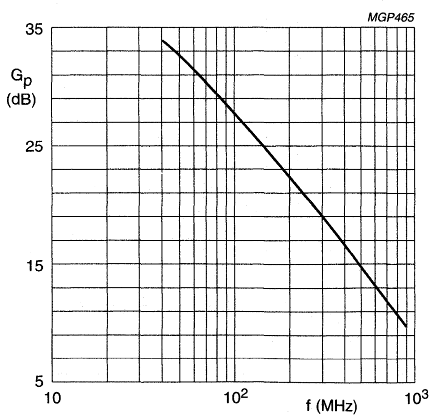
Typical values; V_{CE} = 25 V;
I_C = 600 mA; T_h = 70 °C.

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 25 V;
I_C = 600 mA; T_h = 70 °C.

Fig.13 Load impedance (series components).



Typical values; V_{CE} = 25 V;
I_C = 600 mA; T_h = 70 °C.

Fig.14

Ruggedness

The BLW34 is capable of withstanding a load mismatch (VSWR = 50 through all phases) under the following conditions:

f = 860 MHz; V_{CE} = 25 V; I_C = 600 mA;
T_h = 70 °C and P_L = 4 W.

HF/VHF power transistor — BLW50F

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in class-A, AB and B operated, industrial and military transmitters in the h.f. and v.h.f. band. Resistance stabilization provides protection against device damage at severe load mismatch conditions. Matched h_{FE} groups are available on request.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η_{dt} %	I_C A	$I_{C(ZS)}$ mA	d_3 dB	T_h °C
s.s.b. (class-A)	45	1,6 - 28	0 - 16 (P.E.P.)	> 19,5	–	1,2	–	< –40	70
s.s.b. (class-AB)	50	1,6 - 28	10 - 65 (P.E.P.)	typ. 18	typ. 45(1)	1,45	50	typ. –30	25

Note

1. At 65W P.E.P.

PIN CONFIGURATION

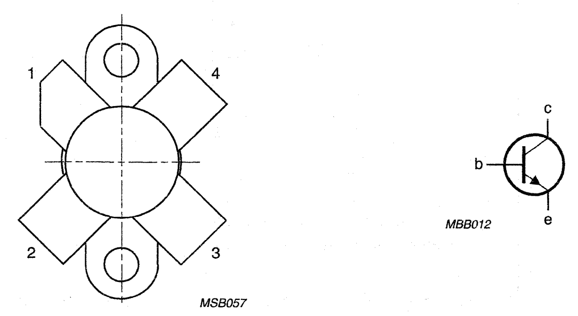


Fig.1 Simplified outline and symbol.

PINNING - SOT123

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	110	V
Collector-emitter voltage (open base)	V_{CEO}	max.	55	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	2,5	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	7,5	A
D.C. and r.f. (f > 1 MHz) power dissipation; T_{mb} = 25 °C	P_{tot}; P_{rf}	max.	94	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

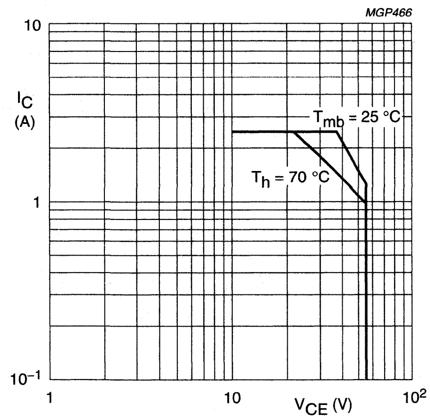
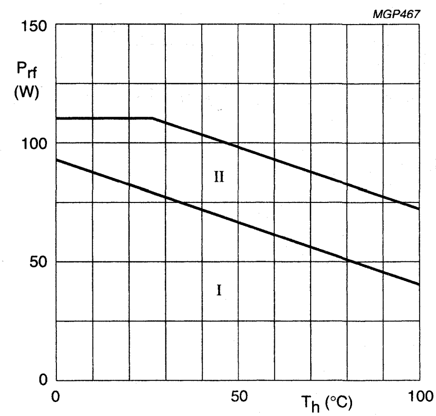


Fig.2 D.C. SOAR.



I Continuous d.c. and r.f. operation
II Short-time operation during mismatch

Fig.3 Power derating curves vs. temperature.

THERMAL RESISTANCE

(dissipation = 54 W; T_{mb} = 86 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. and r.f. dissipation)	$R_{th\ j\text{-}mb}$	=	2,1	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3	K/W

CHARACTERISTICS

$T_j = 25\ °C$

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 25$ mA	$V_{(BR)\,CES}$	>	110	V
Collector-emitter breakdown voltage				
open base; $I_C = 100$ mA	$V_{(BR)\,CEO}$	>	55	V
Emitter-base breakdown voltage				
open collector; $I_E = 10$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 55$ V	I_{CES}	<	10	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	8	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>	8	mJ
D.C. current gain[1]				
$I_C = 1{,}2$ A; $V_{CE} = 5$ V	h_{FE}	typ.	25	
			15 to 100	
D.C. current gain ratio of matched devices[1]				
$I_C = 1{,}2$ A; $V_{CE} = 5$ V	h_{FE1}/h_{FE2}	<	1,2	
Collector-emitter saturation voltage[1]				
$I_C = 3{,}0$ A; $I_B = 0{,}6$ A	V_{CEsat}	typ.	1,2	V
Transition frequency at f = 100 MHz[1]				
$-I_E = 1{,}2$ A; $V_{CB} = 45$ V	f_T	typ.	490	MHz
$-I_E = 4{,}0$ A; $V_{CB} = 45$ V	f_T	typ.	540	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 45$ V	C_c	typ.	53	pF
Feedback capacitance at f = 1 MHz				
$I_C = 50$ mA; $V_{CE} = 45$ V	C_{re}	typ.	35	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0{,}02$.

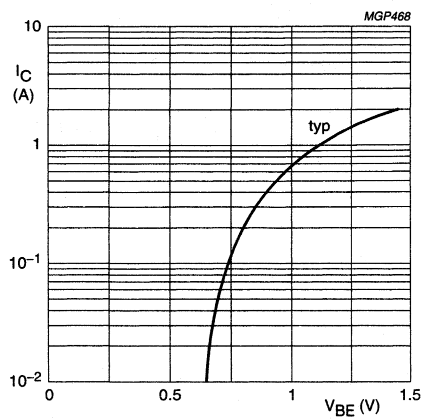


Fig.4 V_{CE} = 40 V; T_{mb} = 25 °C.

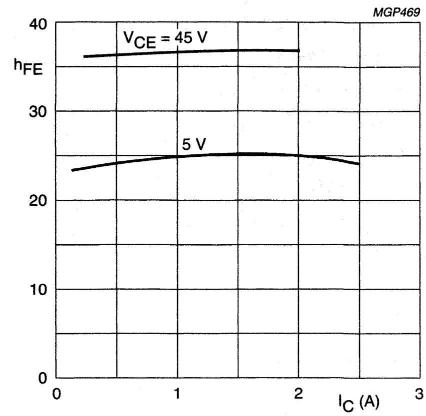


Fig.5 Typical values; T_j = 25 °C.

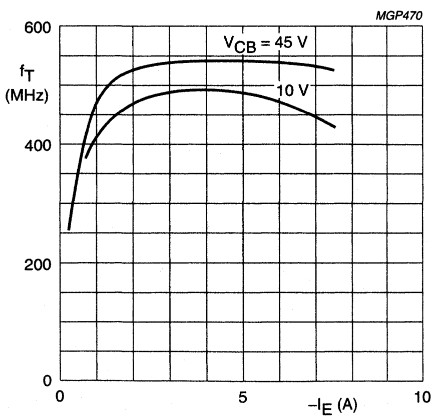


Fig.6 Typical values; f = 100 MHz; T_j = 25 °C.

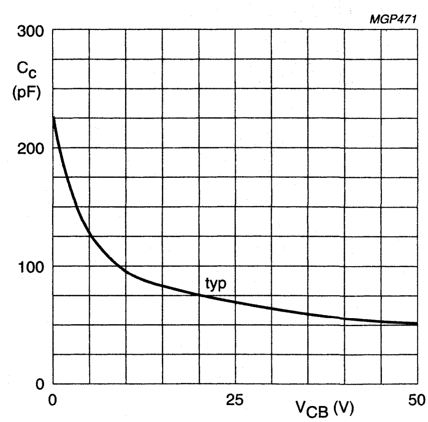


Fig.7 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in s.s.b. class-A operation (linear power amplifier)
V_{CE} = 45 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_p dB	I_C A	d_3(1) dB	d_5(1) dB	T_h °C
> 16 (P.E.P.)	> 19,5	1,2	−40	< −40	70
typ. 17 (P.E.P.)	typ. 20,5	1,2	−40	< −40	70

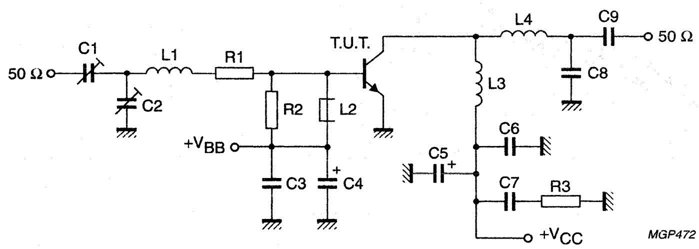


Fig.8 Test circuit; s.s.b. class-A.

List of components in Fig.8:

C1	=	C2 = 10 to 780 pF film dielectric trimmer
C3	=	22 nF ceramic capacitor (63 V)
C4	=	4,7 μF/16 V electrolytic capacitor
C5	=	1 μF/75 V solid tantalum capacitor
C6	=	C7 = 47 nF polyester capacitor (100 V)
C8	=	68 pF ceramic capacitor (500 V)
C9	=	3,9 nF ceramic capacitor
L1	=	3 turns closely wound enamelled Cu wire (1,0 mm); int. dia 9,0 mm; leads 2 × 5 mm
L2	=	Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3	=	1,05 μH; 15 turns enamelled Cu wire (1,0 mm); int. dia. 10 mm; length 17,4 mm; leads 2 × 5 mm
L4	=	162 nH; 6 turns enamelled Cu wire (1,0 mm); int. dia. 7,0 mm; length 11,6 mm; leads 2 × 5 mm
R1	=	1,6 Ω; parallel connection of 3 × 4,7 Ω carbon resistors (± 5%; 0,125 W)
R2	=	47 Ω carbon resistor (± 5%; 0,25 W)
R3	=	4,7 Ω carbon resistor (± 5%; 0,25 W)

Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

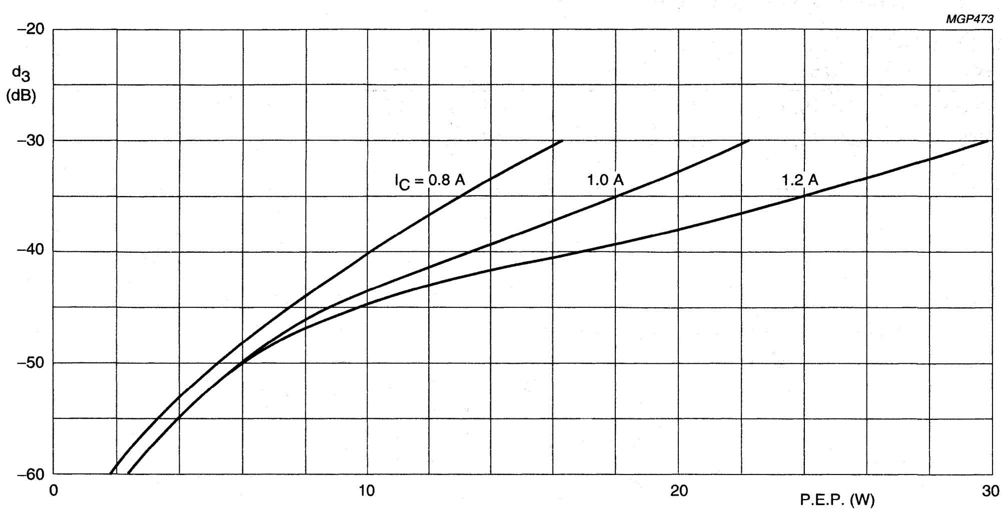


Fig.9 Intermodulation distortion (see note on previous page) as a function of output power. Typical values; V_{CE} = 45 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz; T_h = 70 °C.

R.F. performance in s.s.b. class-AB operation (linear power amplifier)
V_{CE} = 50 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_p dB	η_{dt}(%) AT 65 W P.E.P.	I_C (A) AT 65 W P.E.P.	d_3 (1) dB	d_5 (1) dB	$I_{C(ZS)}$ mA	T_h °C
10 to 65 (P.E.P.)	typ. 18	typ. 45	typ. 1,45	typ. −30	< −30	50	25

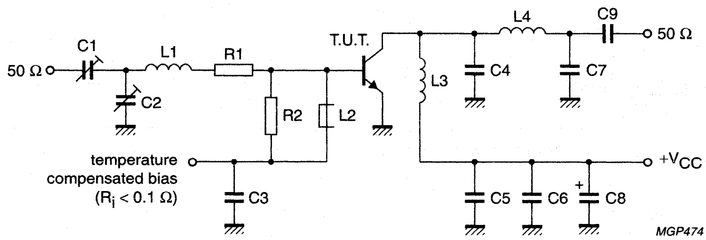


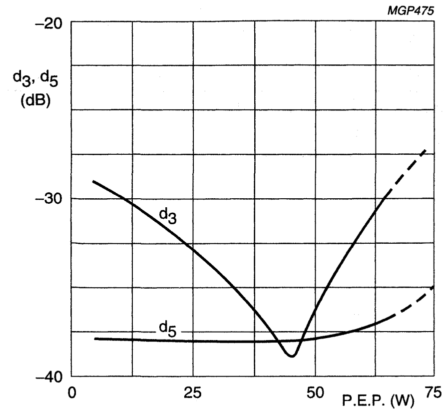
Fig.10 Test circuit; s.s.b. class-AB.

List of components:

C1 = C2 = 10 to 780 pF film dielectric trimmer
C3 = C5 = C6 = 220 nF polyester capacitor
C4 = 120 pF ceramic capacitor (500 V)
C7 = 150 pF ceramic capacitor (500 V)
C8 = 47µF/63 V electrolytic capacitor
C9 = 3,9 nF ceramic capacitor
L1 = 4 turns closely wound enamelled Cu wire (1,6 mm); int. dia 7,0 mm; leads 2 × 5 mm
L2 = Ferroxcube wide-band h.f. choke, grade 3B (cat.no. 4312 020 36640)
L3 = 9 turns enamelled Cu wire (1,0 mm); int. dia. 10 mm; length 14,5 mm; leads 2 × 5 mm
L4 = 6 turns enamelled Cu wire (1,0 mm); int. dia. 6,5 mm; length 11,0 mm; leads 2 × 5 mm
R1 = 2,4 Ω; parallel connection of 2 × 4,7 Ω carbon resistors
R2 = 39 Ω carbon resistor

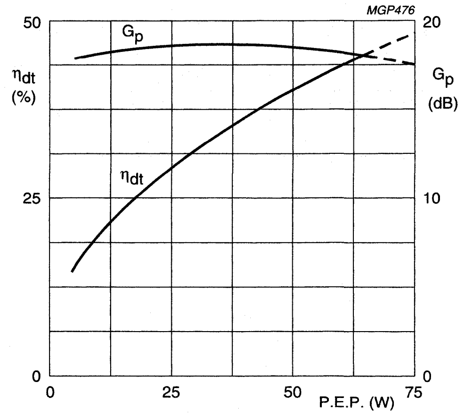
Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.



V_{CE} = 50 V; $I_{C(ZS)}$ = 50 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

Fig.11 Intermodulation distortion as a function of output power(1).



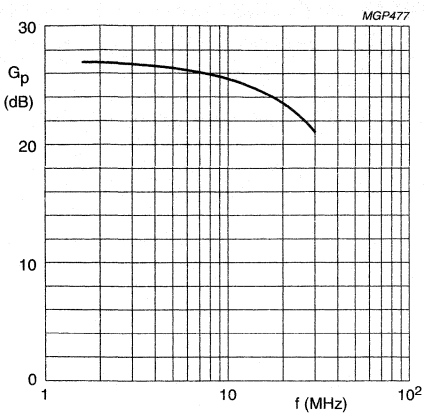
V_{CE} = 50 V; $I_{C(ZS)}$ = 50 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

Fig.12 Double-tone efficiency and power gain as a function of output power.

Ruggedness in s.s.b. operation

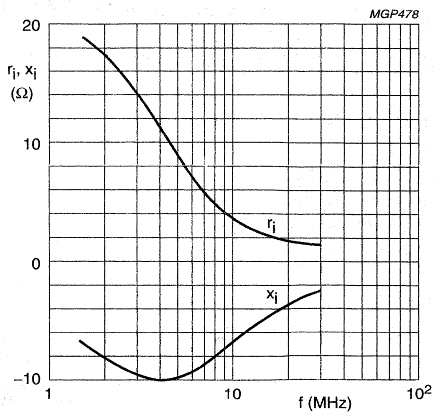
The BLW50F is capable of withstanding full load mismatch (VSWR = 50 through all phases) up to 45 W (P.E.P.) under the following conditions:

V_{CE} = 50 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz; T_h = 70 °C; $R_{th\ mb\text{-}h}$ = 0,3 K/W.



V_{CE} = 50 V; $I_{C(ZS)}$ = 50 mA; P_L = 60 W;
T_h = 25 °C; Z_L = 16 Ω.

Fig.13 Power gain as a function of frequency.



V_{CE} = 50 V; $I_{C(ZS)}$ = 50 mA; P_L = 60 W;
T_h = 25 °C; Z_L = 16 Ω.

Fig.14 Input impedance (series components) as a function of frequency.

Figs 13 and 14 are typical curves and hold for an unneutralized amplifier in s.s.b. class-AB operation.

HF/VHF power transistor BLW76

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-AB or class-B operated high power transmitters in the h.f. and v.h.f. bands. The transistor presents excellent performance as a linear amplifier in the h.f. band. It is resistance stabilized and is guaranteed to withstand severe load mismatch conditions. Transistors are delivered in matched h_{FE} groups.

The transistor has a ½" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C

MODE OF OPERATION	V_{CE} V	$I_{C(ZS)}$ A	f MHz	P_L W	G_p dB	η %	d_3 dB
s.s.b. (class-AB)	**28**	**0,05**	**1,6 – 28**	**8 – 80 (P.E.P.)**	> **13**	> **35**(1)	< **–30**
c.w. (class-B)	28	–	108	80	typ. 7,9	typ. 70	–

Note

1. At 80 W P.E.P.

PIN CONFIGURATION

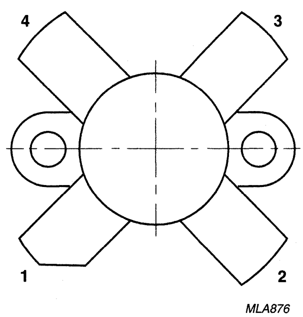


Fig.1 Simplified outline. SOT121B.

PINNING - SOT121B.

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	70	V
Collector-emitter voltage (open base)	V_{CEO}	max.	35	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	8	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	20	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	140	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

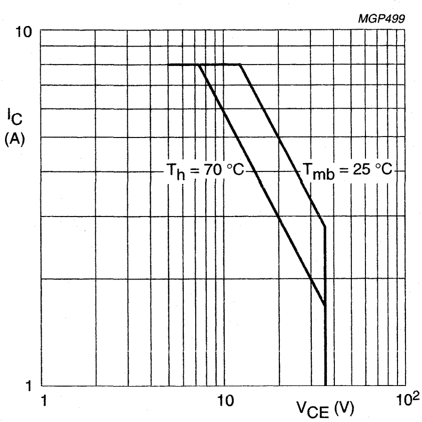
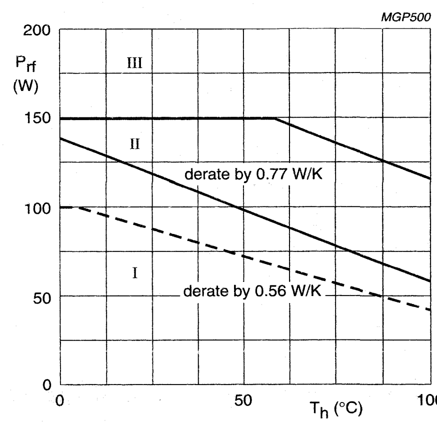


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \leq 28$ V; f > 1 MHz.

THERMAL RESISTANCE

(dissipation = 60 W; T_{mb} = 82 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	1,92	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	1,33	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,2	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 50 mA	$V_{(BR)\,CES}$	>	70	V
Collector-emitter breakdown voltage				
open base; I_C = 50 mA	$V_{(BR)\,CEO}$	>	35	V
Emitter-base breakdown voltage				
open collector; I_E = 10 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 35 V	I_{CES}	<	10	mA
D.C. current gain(1)				
I_C = 4 A; V_{CE} = 5 V	h_{FE}		15 to 80	
D.C. current grain ratio of matched devices(1)				
I_C = 4 A; V_{CE} = 5 V	h_{FE1}/h_{FE2}	<	1,2	
Collector-emitter saturation voltage(1)				
I_C = 12,5 A; I_B = 2,5 A	V_{CEsat}	typ.	2,5	V
Transition frequency at f = 100 MHz(2)				
$-I_E$ = 4 A; V_{CB} = 28 V	f_T	typ.	315	MHz
$-I_E$ = 12,5 A; V_{CB} = 28 V	f_T	typ.	305	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 28 V	C_c	typ.	125	pF
Feedback capacitance at f = 1 MHz				
I_C = 50 mA; V_{CE} = 28 V	C_{re}	typ.	85	pF
Collector-flange capacitance	C_{cf}	typ.	3	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0{,}01$.

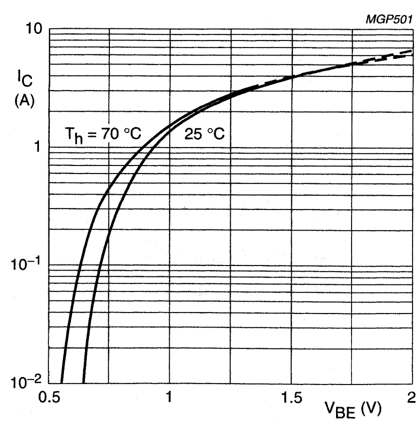


Fig.4 Typical values; V_{CE} = 20 V.

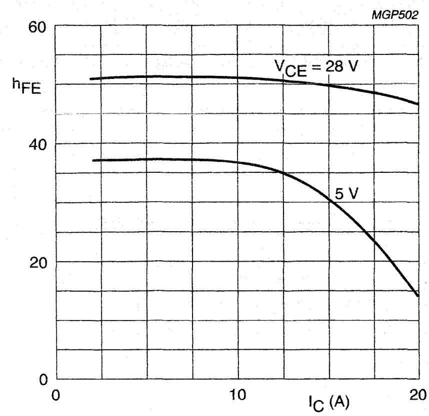


Fig.5 Typical values; T_j = 25 °C.

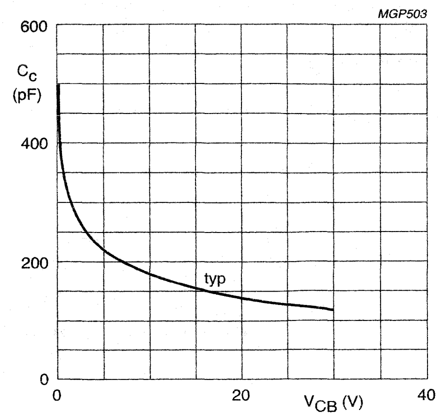


Fig.6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

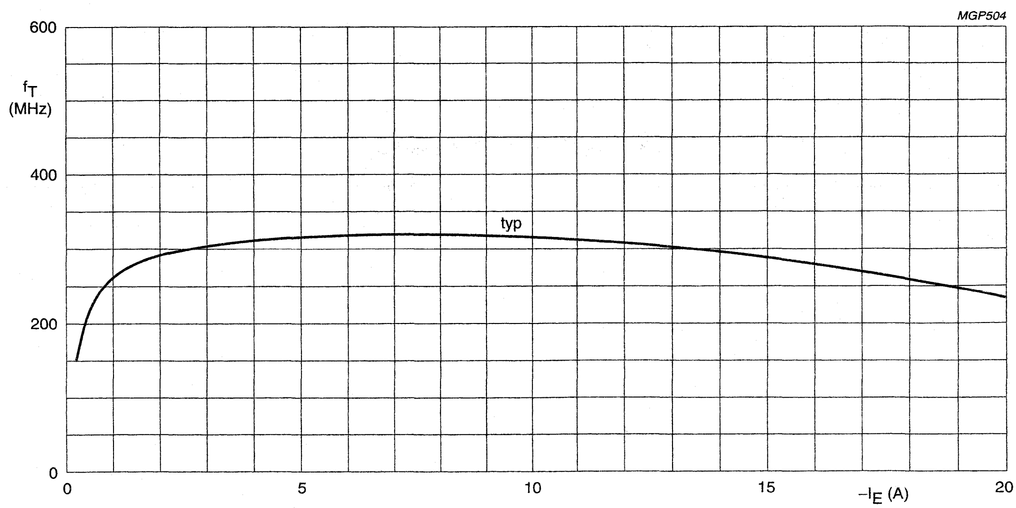


Fig.7 V_{CB} = 28 V; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in s.s.b. class-AB operation (linear power amplifier)
V_{CE} = 28 V; T_h = 25 °C; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_p dB	η_{dt} (%) at 80 W P.E.P.	I_C (A) at 80 W P.E.P.	d_3 dB	d_5 dB	$I_{C(ZS)}$ A
8 to 80 (P.E.P.)	> 13	> 35	< 4,1	< −30	< −30	0,05

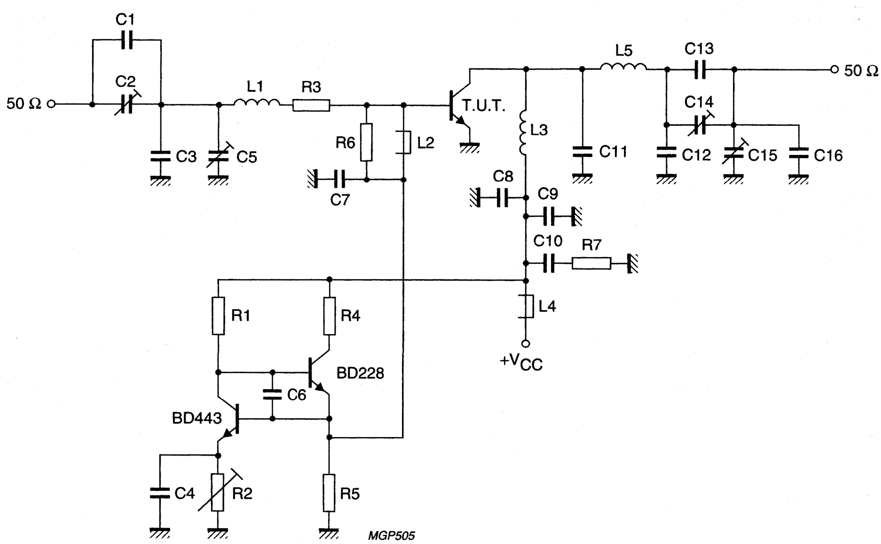
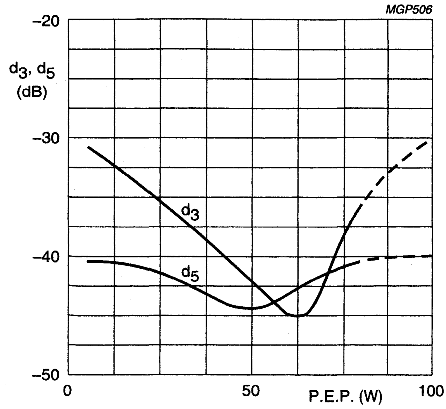


Fig.8 Test circuit; s.s.b. class-AB.

List of components:

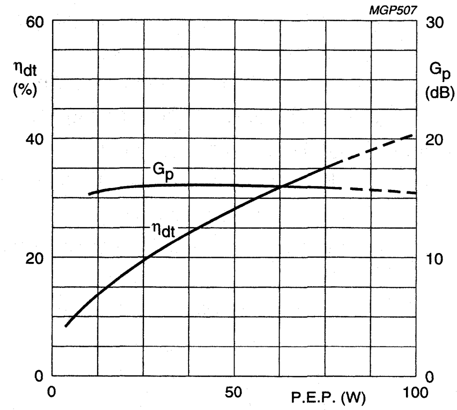
C1	=	27 pF ceramic capacitor (500 V)
C2	=	100 pF air dielectric trimmer (single insulated rotor type)
C3	=	100 pF polystyrene capacitor
C4	=	C6 = C9 = 100 nF polyester capacitor
C5	=	280 pF air dielectric trimmer (single non-insulated rotor type)
C7	=	C8 = 3,9 nF ceramic capacitor
C10	=	2,2 μF moulded metallized polyester capacitor
C11	=	180 pF polystyrene capacitor
C12	=	2 × 68 pF ceramic capacitors in parallel (500 V)
C13	=	120 pF polystyrene capacitor
C14	=	C15 = 280 pF air dielectric trimmer (single insulated rotor type)
C16	=	56 pF ceramic capacitor (500 V)
L1	=	108 nH; 4 turns Cu wire (1,6 mm); int. dia. 8,7 mm; length 11,2 mm; leads 2 × 7 mm
L2	=	L4 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3	=	88 nH; 3 turns Cu wire (1,6 mm); int. dia. 8,0 mm; length 8,0 mm; leads 2 × 7 mm
L5	=	120 nH; 4 turns Cu wire (1,6 mm); int. dia. 9,3 mm; length 11,2 mm; leads 2 × 7 mm
R1	=	1,5 kΩ (± 5%) carbon resistor (0,5 W)
R2	=	10 Ω wirewound potentiometer (3 W)
R3	=	0,9 Ω; parallel connection of 2 × 1,8 Ω carbon resistors (± 5%; 0,5 W each)
R4	=	60 Ω; parallel connection of 2 × 120 Ω wirewound resistors (5,5 W each)
R5	=	56 Ω (± 5%) carbon resistor (0,5 W)
R6	=	33 Ω (± 5%) carbon resistor (0,5 W)
R7	=	4,7 Ω (± 5%) carbon resistor (0,5 W)



V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

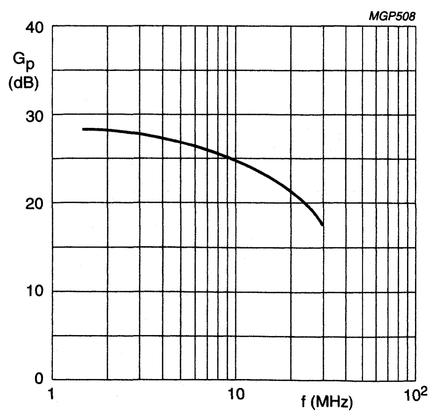
Fig.9 Intermodulation distortion as a function of output power.[1.)]

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.



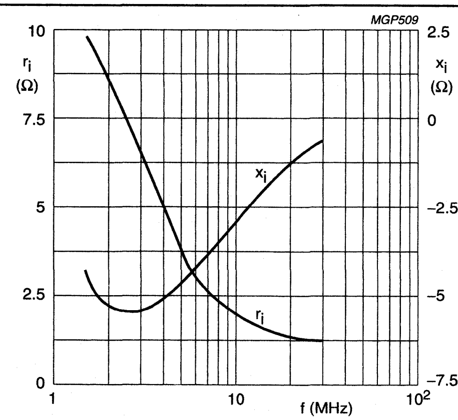
V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

Fig.10 Double-tone efficiency and power gain as a function of output power.



V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; P_L = 80 W;
T_h 25 °C; Z_L = 3,9 Ω.

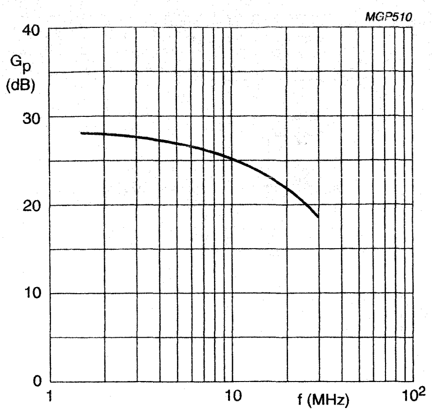
Fig.11 Power gain as a function of frequency.



V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; P_L = 80 W;
T_h 25 °C; Z_L = 3,9 Ω.

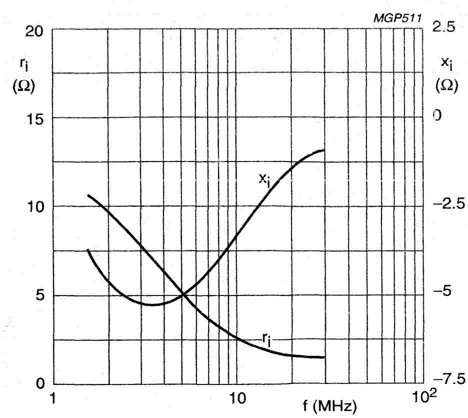
Fig.12 Input impedance (series components) as a function of frequency.

Figs 11 and 12 are typical curves and hold for an unneutralized amplifier in s.s.b. class-AB operation.



V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; P_L = 80 W; T_h = 25 °C;
Z_L = 3,9 Ω; neutralizing capacitor: 68 pF.

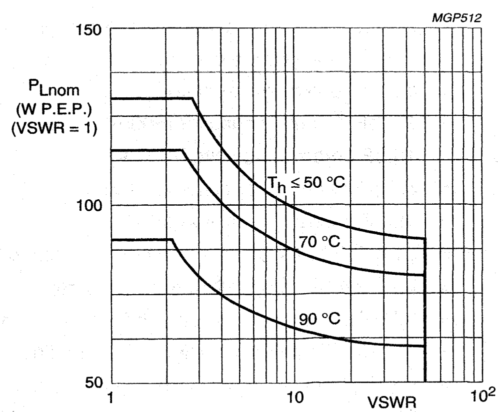
Fig.13 Power gain as a function of frequency.



V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; P_L = 80 W; T_h = 25 °C;
Z_L = 3,9 Ω; neutralizing capacitor: 68 pF.

Fig.14 Input impedance (series components) as a function of frequency.

Figs 13 and 14 are typical curves and hold for a push-pull amplifier with cross-neutralization in s.s.b. class-AB operation.



The graph shows the permissible output power under nominal conditions (VSWR = 1) as a function of the expected VSWR during short-time mismatch conditions with heatsink temperatures as parameter.

Fig.15 R.F. SOAR; s.s.b. class-AB operation; f_1 = 28,000 MHz; f_2 = 28,001 MHz; V_{CE} = 28 V; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit); T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_p (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
108	28	80	typ. 13	typ. 7,9	typ. 4,1	typ. 70	0,85 + j1,0	174 − j40

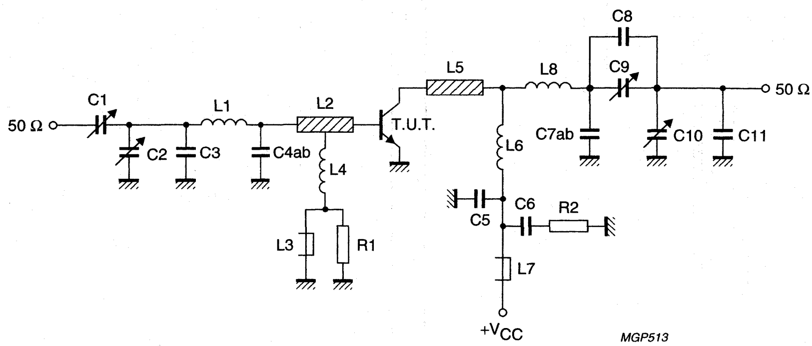


Fig.16 Test circuit; c.w. class-B.

List of components:

C1	=	C9 = C10 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C2	=	5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
C3	=	22 pF ceramic capacitor (500 V)
C4ab	=	2 × 82 pF ceramic capacitors in parallel (500 V)
C5	=	270 pF polystyrene capacitor
C6	=	100 nF polyester capacitor
C7a	=	8,2 pF ceramic capacitor (500 V)
C7b	=	10 pF ceramic capacitor (500 V)
C 8	=	5,6 pF ceramic capacitor (500 V)
C11	=	10 pF ceramic capacitor (500 V)
L1	=	21 nH; 2 turns Cu wire (1,0 mm); int. dia. 4,0 mm; length 3,5 mm; leads 2 × 5 mm
L2	=	L5 = 2,4 nH; strip (12 mm × 6 mm); tap for L4 at 6 mm from transistor
L3	=	L7 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4	=	100 nH; 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 × 5 mm
L6	=	49 nH; 2 turns Cu wire (1,6 mm); int. dia. 9,0 mm; length 4,7 mm; leads 2 × 5 mm
L8	=	56 nH; 2 turns Cu wire (1,6 mm); int. dia. 10,0 mm; length 4,5 mm; leads 2 × 5 mm

L2 and L5 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric.

R1	=	R2 = 10 Ω (± 10%) carbon resistor

Component layout and printed-circuit board for 108 MHz test circuit are shown in Fig.17.

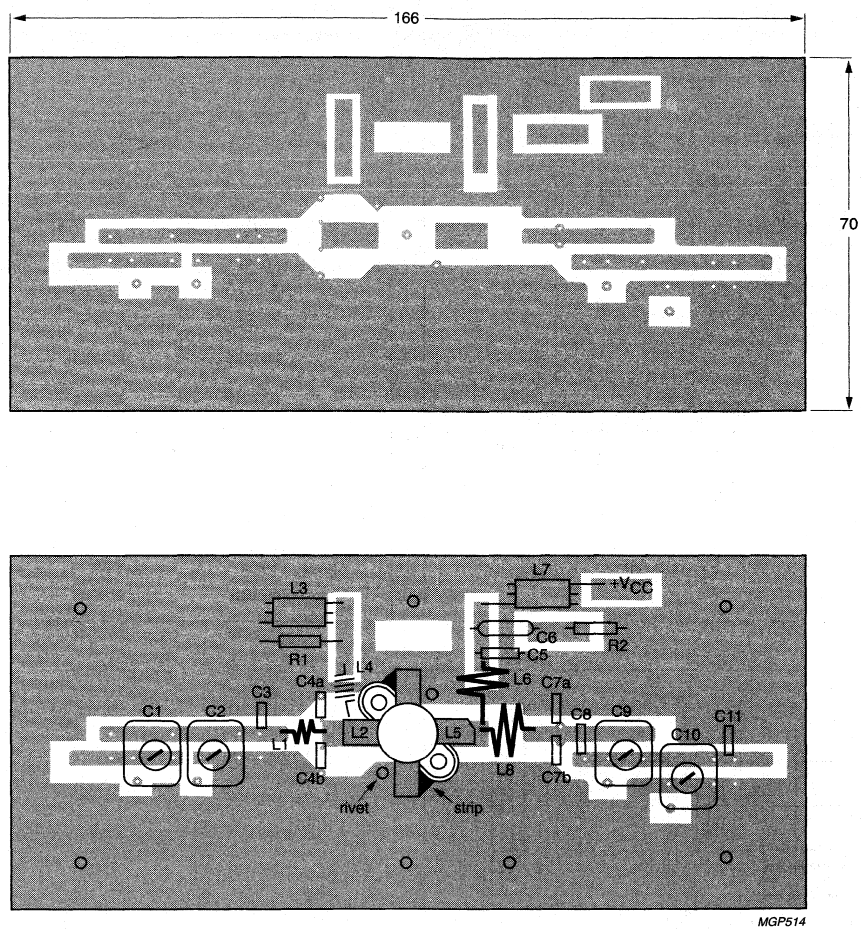


Fig.17 Component layout and printed-circuit board for 108 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

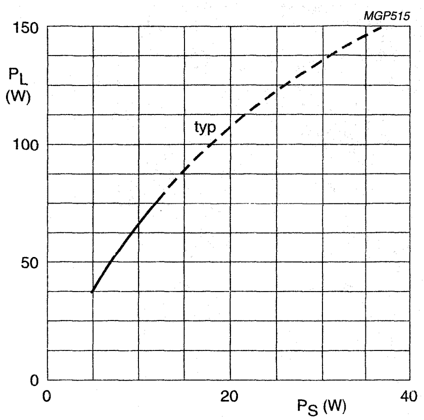


Fig.18 V_{CE} = 28 V; f = 108 MHz; T_h = 25 °C.

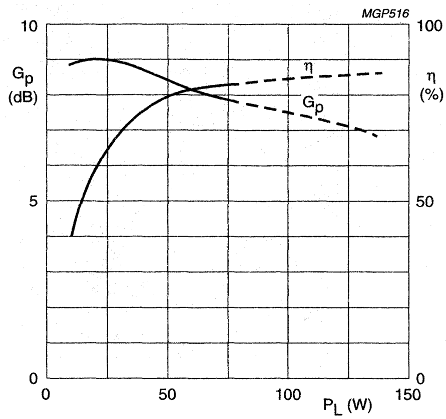
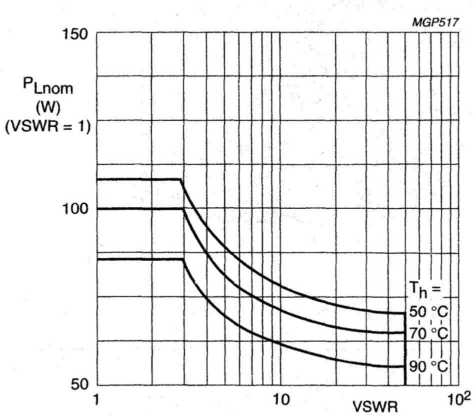


Fig.19 V_{CE} = 28 V; f = 108 MHz; T_h = 25 °C; typical values.



The graph shows the permissible output power under nominal conditions (VSWR = 1) as a function of the expected VSWR during short-time mismatch conditions with heatsink temperatures as parameter.

Fig.20 R.F. SOAR; c.w. class-B operation;
f = 108 MHz; V_{CE} = 28 V; $R_{th\ mb-h}$ = 0,2 K/W.

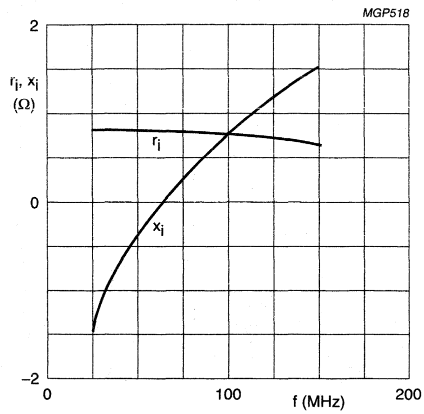


Fig.21 V_{CE} = 28 V; P_L = 80 W; T_h = 25 °C; typical values.

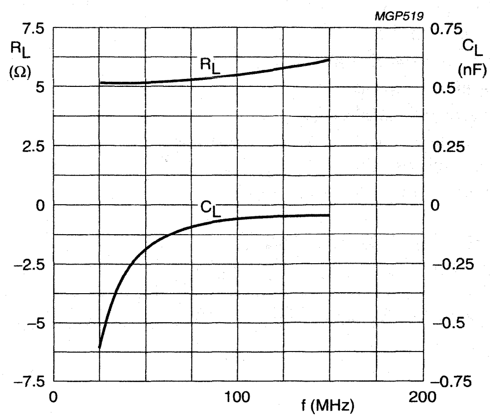


Fig.22 V_{CE} = 28 V; P_L = 80 W; T_h = 25 °C; typical values.

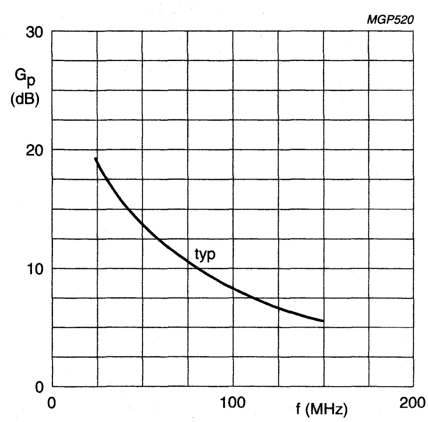


Fig.23 V_{CE} = 28 V; P_L = 80 W; T_h = 25 °C.

HF/VHF power transistor | BLW77

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-AB or class-B operated high power transmitters in the h.f. and v.h.f. bands. The transistor presents excellent performance as a linear amplifier in the h.f. band. It is resistance stabilized and is guaranteed to withstand severe load mismatch conditions. Transistors are delivered in matched h_{FE} groups.

The transistor has a ½" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C

MODE OF OPERATION	V_{CE} V	$I_{C(ZS)}$ A	f MHz	P_L W	G_p dB	η %	d_3 dB
s.s.b. (class-AB)	**28**	**0,1**	**1,6 – 28**	**15 – 130** (P.E.P.)	**> 12**	**> 37,5**(1)	**< –30**
c.w. (class-B)	28	–	87,5	130	typ. 7,5	typ. 75	–

Note

1. At 130 W P.E.P.

PIN CONFIGURATION

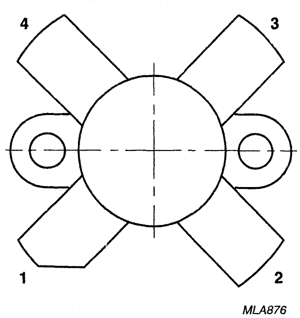


Fig.1 Simplified outline. SOT121B.

PINNING - SOT121B.

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

HF/VHF power transistor BLW77

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	70	V
Collector-emitter voltage (open base)	V_{CEO}	max.	35	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	12	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	30	A
R.F. power dissipation (f > 1 MHz;); T_{mb} = 25 °C	P_{rf}	max.	245	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

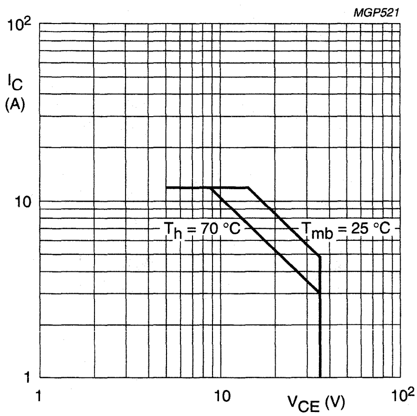
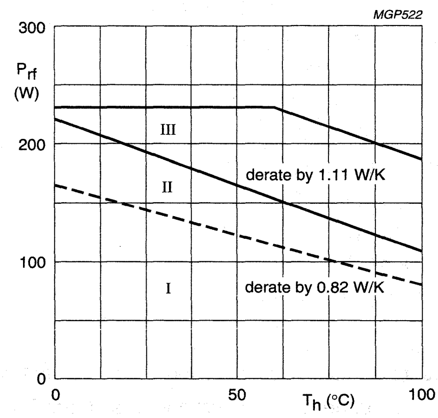


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \leq 28$ V; f ≥ 1 MHz.

THERMAL RESISTANCE

(dissipation = 100 W; T_{mb} = 90 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	1,03	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	0,71	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,2	K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 50$ mA	$V_{(BR)\,CES}$	>	70	V
Collector-emitter breakdown voltage				
open base; $I_C = 100$ mA	$V_{(BR)\,CEO}$	>	35	V
Emitter-base breakdown voltage				
open collector; $I_E = 20$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 35$ V	I_{CES}	<	20	mA
D.C. current gain(1)				
$I_C = 7$ A; $V_{CE} = 5$ V	h_{FE}		15 to 80	
D.C. current gain ratio of matched devices(1)				
$I_C = 7$ A; $V_{CE} = 5$ V	h_{FE1}/h_{FE2}	<	1,2	
Collector-emitter saturation voltage(1)				
$I_C = 20$ A; $I_B = 4$ A	V_{CEsat}	typ.	2	V
Transition frequency at f = 100 MHz(2)				
$-I_E = 7$ A; $V_{CB} = 28$ V	f_T	typ.	320	MHz
$-I_E = 20$ A; $V_{CB} = 28$ V	f_T	typ.	300	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 28$ V	C_c	typ.	255	pF
Feedback capacitance at f = 1 MHz				
$I_C = 100$ mA; $V_{CE} = 28$ V	C_{re}	typ.	175	pF
Collector-flange capacitance	C_{cf}	typ.	3	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50$ µs; $\delta \leq 0{,}01$.

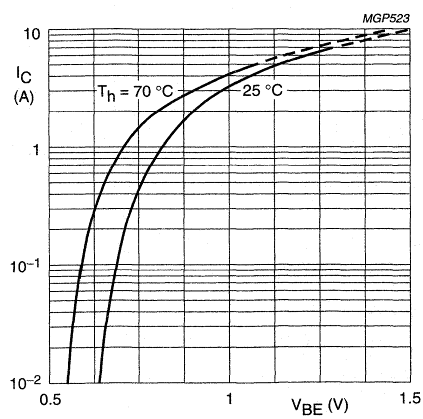


Fig.4 Typical values; $V_{CE} = 20$ V.

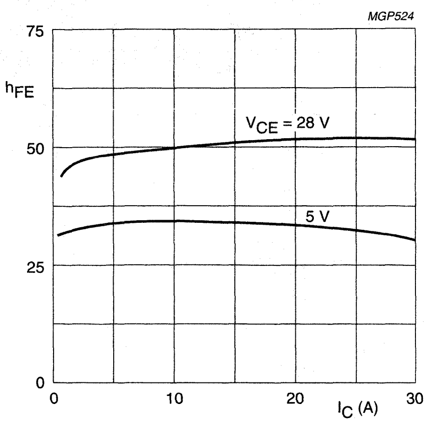


Fig.5 Typical values; T_j = 25 °C.

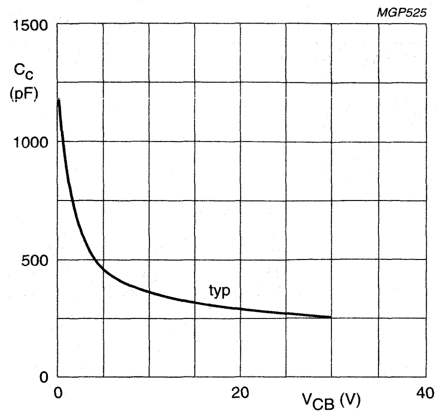


Fig.6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

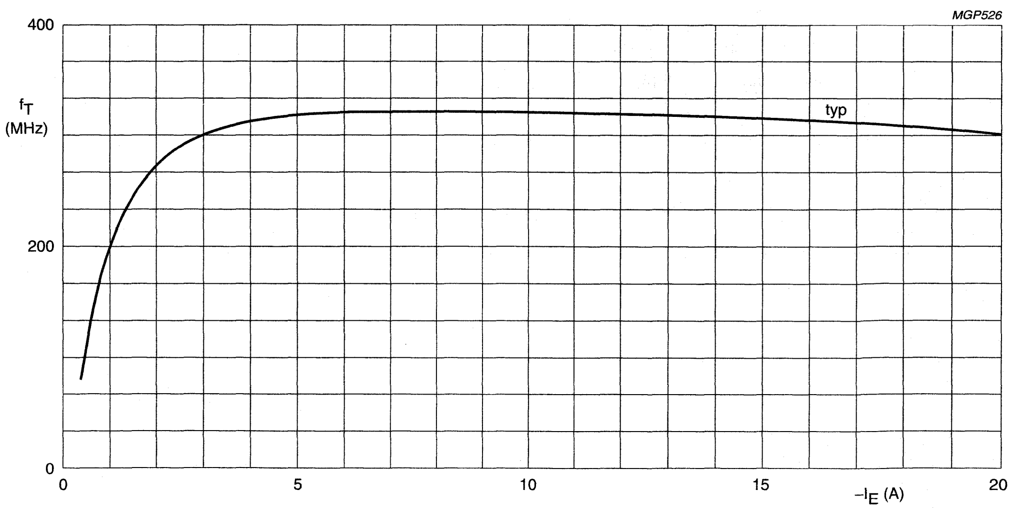


Fig.7 V_{CB} = 28 V; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in s.s.b. class-AB operation (linear power amplifier)

V_{CE} = 28 V; T_h = 25 °C; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER	G_p	η_{dt} (%)	I_C (A)	d_3	d_5	$I_{C(ZS)}$
W	dB	at 130 W P.E.P.		dB	dB	A
15 to 130 (P.E.P.)	> **12**	> **37,5**	< **6,2**	< **−30**	< **−30**	**0,1**

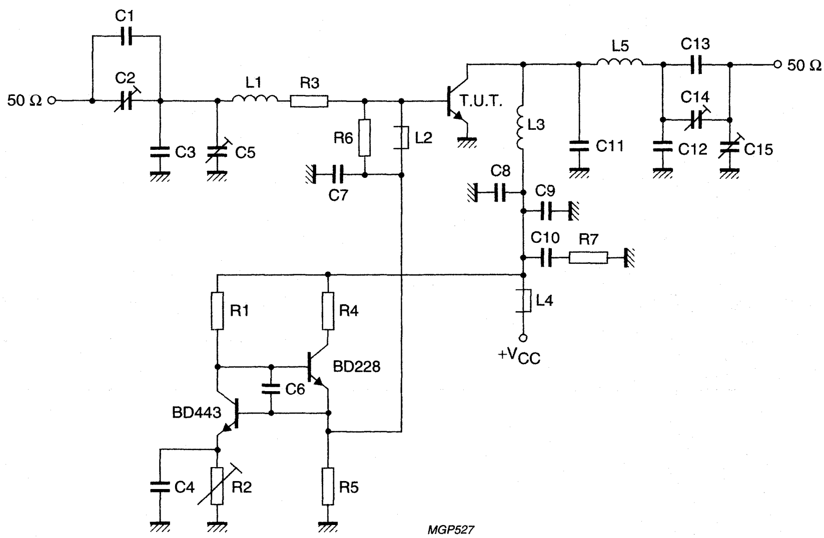
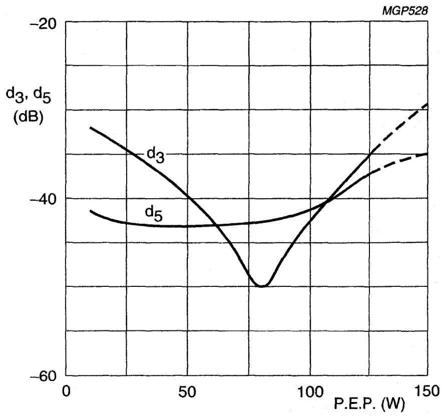


Fig.8 Test circuit; s.s.b. class-AB.

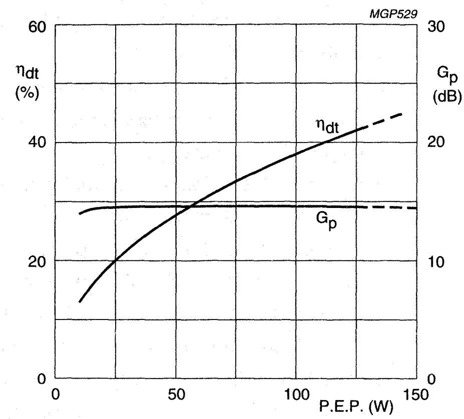
List of components:

C1	=	27 pF ceramic capacitor (500 V)
C2	=	100 pF air dielectric trimmer (single insulated rotor type)
C3	=	180 pF polystyrene capacitor
C4	=	C6 = C9 = 100 nF polyester capacitor
C5	=	100 pF air dielectric trimmer (single non-insulated rotor type)
C7	=	C8 = 3,9 nF ceramic capacitor
C10	=	2,2 μF moulded metallized polyester capacitor
C11	=	2 × 180 pF polysterene capacitors in parallel
C12	=	3 × 56 pF and 33 pF ceramic capacitors in parallel (500 V)
C13	=	4 × 56 pF and 68 pF ceramic capacitors in parallel (500 V)
C14	=	360 pF air dielectric trimmer (single insulated rotor type)
C15	=	360 pF air dielectric trimmer (single non-insulated rotor type)
L1	=	88 nH; 3 turns Cu wire (1,0 mm); int. dia. 9,0 mm; length 6,1 mm; leads 2 × 7 mm
L2	=	L4 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3	=	L5 = 80 nH; 2,5 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 10,0 mm; leads 2 × 7 mm
R1	=	470 Ω wirewound resistor (5,5 W)
R2	=	4,7 Ω wirewound potentiometer (3 W)
R3	=	0,55 Ω; parallel connection of 4 × 2,2 Ω carbon resistors (± 5%; 0,5 W each)
R4	=	45 Ω; parallel connection of 4 × 180 Ω wirewound resistors (5,5 W each)
R5	=	56 Ω (± 5%) carbon resistor (0,5 W)
R6	=	27 Ω (± 5%) carbon resistor (0,5 W)
R7	=	4,7 Ω (± 5%) carbon resistor (0,5 W)



V_{CE} = 28 V; $I_{C(ZS)}$ = 100 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

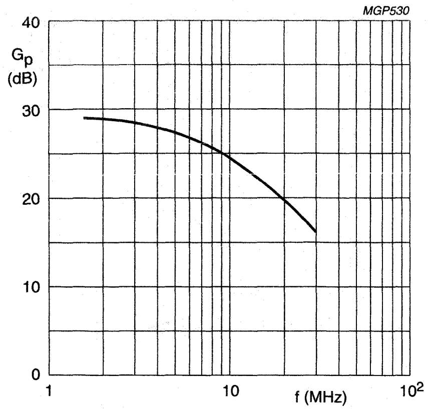
Fig.9 Intermodulation distortion as a function of output power.(1.)



V_{CE} = 28 V; $I_{C(ZS)}$ = 100 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

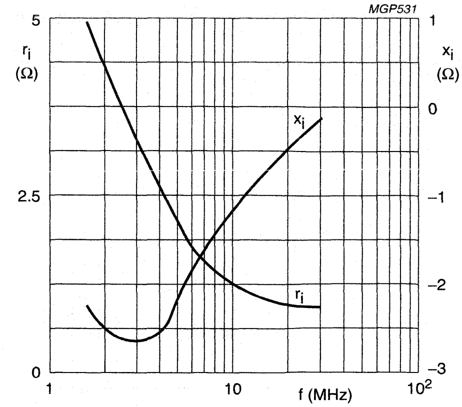
Fig.10 Double-tone efficiency and power gain as a function of output power.

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.



V_{CE} = 28 V; $I_{C(ZS)}$ = 100 mA; P_L = 130 W;
T_h = 25 °C; Z_L = 2,5 Ω.

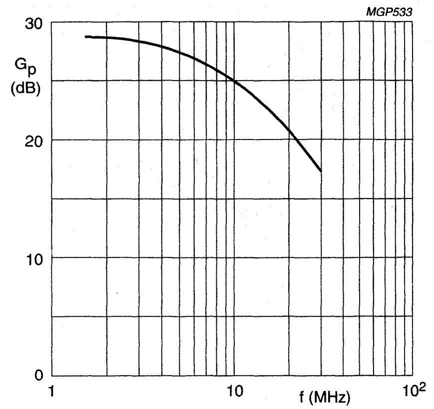
Fig.11 Power gain as a function of frequency.



V_{CE} = 28 V; $I_{C(ZS)}$ = 100 mA; P_L = 130 W;
T_h = 25 °C; Z_L = 2,5 Ω.

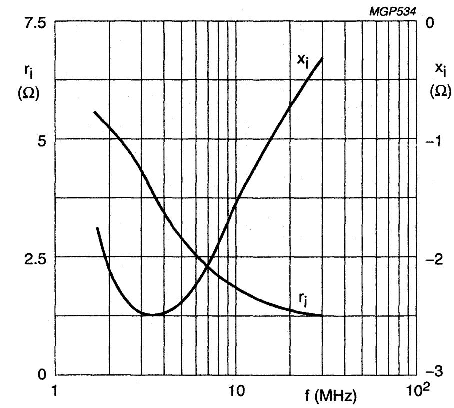
Fig.12 Input impedance (series components) as a function of frequency.

Figs 11 and 12 are typical curves and hold for an unneutralized amplifier in s.s.b. class-AB operation.



V_{CE} = 28 V; $I_{C(ZS)}$ = 100 mA; P_L = 130 W; T_h = 25 °C;
Z_L = 2,5 Ω; neutralizing capacitor: 150 pF.

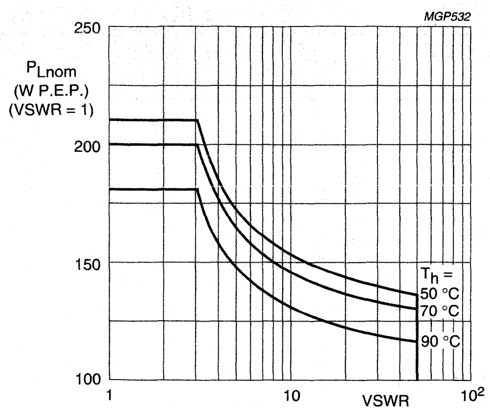
Fig.13 Power gain as a function of frequency.



V_{CE} = 28 V; $I_{C(ZS)}$ = 100 mA; P_L = 130 W; T_h = 25 °C;
Z_L = 2,5 Ω; neutralizing capacitor: 150 pF.

Fig.14 Input impedance (series components) as a function of frequency.

13 and 14 are typical curves and hold for a push-pull amplifier with cross-neutralization in s.s.b class-AB operation.



The graph shows the permissible output power under nominal conditions (VSWR = 1) as a function of the expected VSWR during short-time mismatch conditions with heatsink temperatures as parameter.

Fig.15 R.F. SOAR; s.s.b. class-AB operation; f_1 = 28,000 MHz; f_2 = 28,001 MHz; V_{CE} = 28 V; $R_{th\ mb-h}$ = 0,2 K/W.

HF/VHF power transistor BLW77

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit); T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_p (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
87,5	**28**	**130**	typ. **23,2**	typ. **7,5**	typ. **6,2**	typ. **75**	**0,62 + j0,73**	**273 − j42**

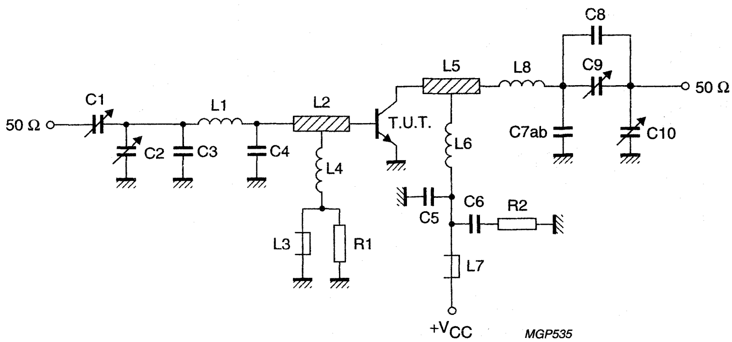


Fig.16 Test circuit; c.w. class-B.

List of components:

C1	=	4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C2	=	C9 = C10 = 7 to 100 pF film dielectric trimmer (cat. no. 2222 809 07015)
C3	=	C8 = 22 pF ceramic capacitor (500 V)
C4	=	4 × 82 pF ceramic capacitors in parallel (500 V)
C5	=	390 pF polystyrene capacitor
C6	=	220 nF polyester capacitor
C7a	=	2 × 10 pF ceramic capacitors in parallel (500 V)
C7b	=	2 × 8,2 pF ceramic capacitors in parallel (500 V)
L1	=	25 nH; 2 turns Cu wire (1,6 mm); int. dia. 5,0 mm; length 4,6 mm; leads 2 × 5 mm
L2	=	L5 = 2,4 nH; strip (12 mm × 6 mm); tap for L4 and L6 at 5 mm from transistor
L3	=	L7 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4	=	100 nH; 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 × 5 mm
L6	=	46 nH; 2 turns Cu wire (2,0 mm); int. dia. 9,0 mm; length 6,0 mm; leads 2 × 5 mm
L8	=	44 nH; 2 turns Cu wire (2,0 mm); int. dia. 9,0 mm; length 6,7 mm; leads 2 × 5 mm

L2 and L5 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric.

R1	=	10 Ω (± 10%) carbon resistor
R2	=	10 Ω (± 10%) carbon resistor

Component layout and printed-circuit board for 87,5 MHz test circuit are shown in Fig.17.

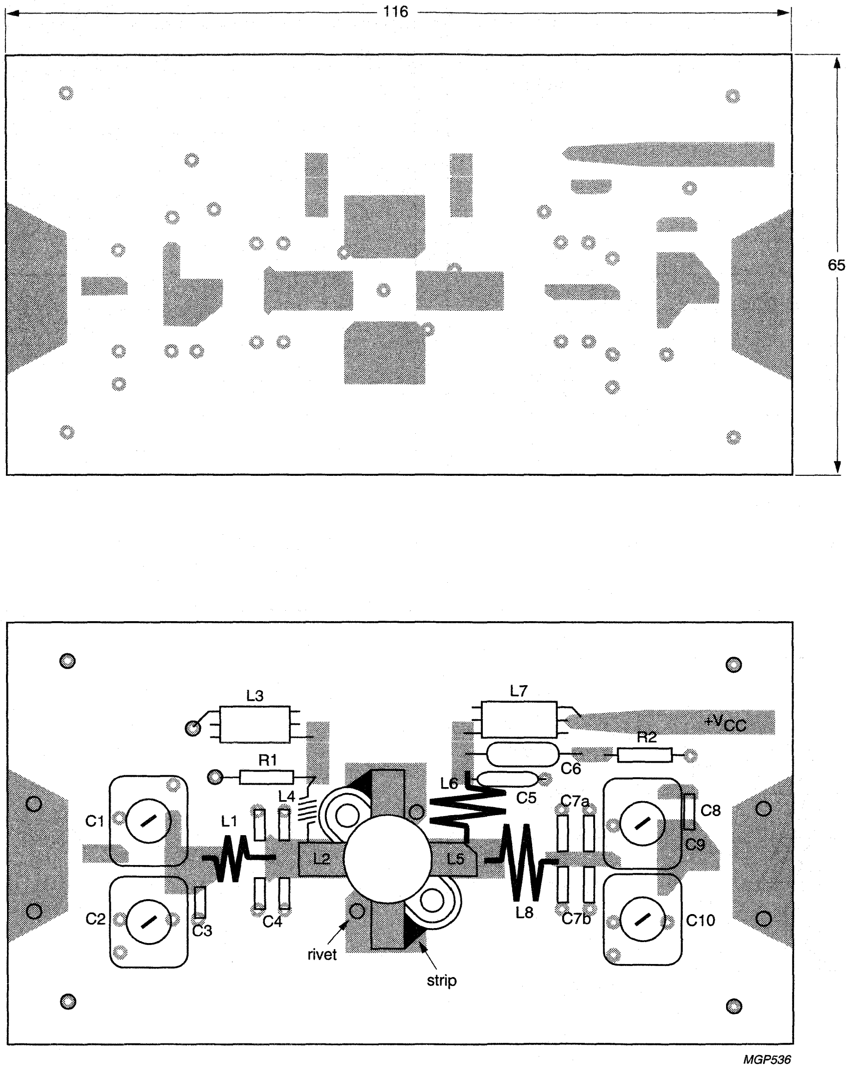


Fig.17 Component layout and printed-circuit board for 87,5 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

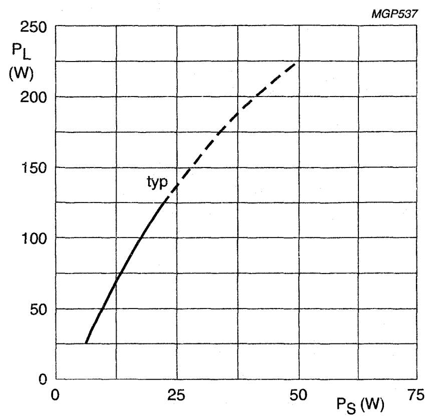


Fig.18 V_{CE} = 28 V; f = 87,5 MHz; T_h = 25 °C.

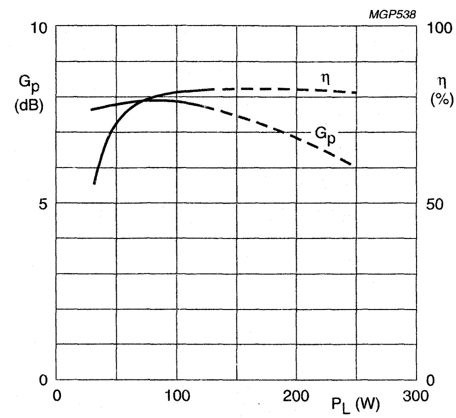
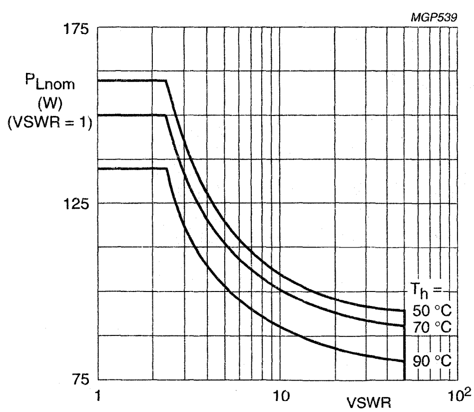


Fig.19 V_{CE} = 28 V; f = 87,5 MHz; T_h = 25 °C; typical values.



The graph shows the permissible output power under nominal conditions (VSWR = 1) as a function of the expected VSWR during short-time mismatch conditions with heatsink temperatures as parameter.

Fig.20 R.F. SOAR; c.w. class-B operation; f = 87,5 MHz; V_{CE} = 28 V; $R_{th\ mb\text{-}h}$ = 0,2 K/W.

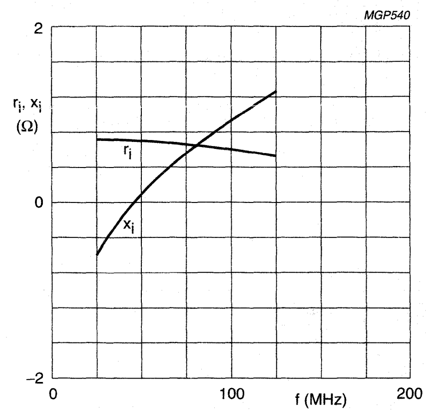


Fig.21 V_{CE} = 28 V; P_L =130 W; T_h = 25 °C; typical values.

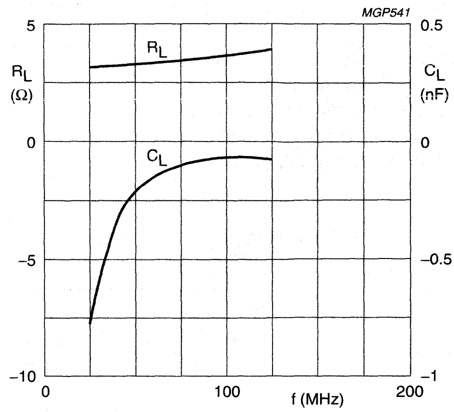


Fig.22 V_{CE} = 28 V; P_L =130 W; T_h = 25 °C; typical values.

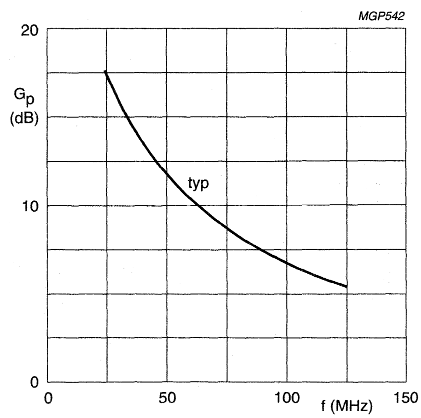


Fig.23 V_{CE} = 28 V; P_L =130 W; T_h = 25 °C.

HF/VHF power transistor — BLW83

DESCRIPTION

N-P-N silicon planar epitaxial transistor for use in transmitting amplifiers operating in the h.f. and v.h.f. bands, with a nominal supply voltage of 28 V. The transistor is specified for s.s.b. applications as linear amplifier in class-A and AB. The device is resistance stabilized and is guaranteed to withstand severe load mismatch conditions.

Matched h_{FE} groups are available on request.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η_{dt} %	I_C A	d_3 dB	T_h °C
s.s.b. (class-A)	**26**	**1,6 – 28**	**0 – 10 (P.E.P.)**	**> 20**	–	**1,35**	**< –40**	**70**
s.s.b. (class-AB)	28	1,6 – 28	3 – 30 (P.E.P.)	typ. 21	typ. 40	typ. 1,34	typ. –30	25

PIN CONFIGURATION

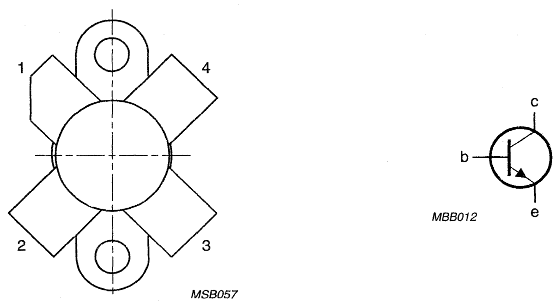


Fig.1 Simplified outline and symbol.

PINNING - SOT123

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage ($V_{BE} = 0$)				
peak value	V_{CESM}	max.	65	V
Collector-emitter voltage (open base)	V_{CEO}	max.	36	V
Emitter-base voltage (open-collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	3	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	9	A
R.F. power dissipation (f > 1 MHz); $T_{mb} = 25$ °C	P_{rf}	max.	76	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

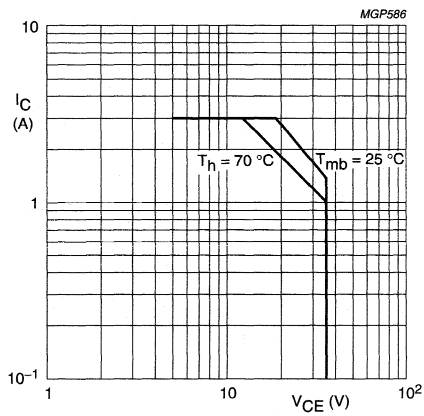


Fig.2 D.C. SOAR.

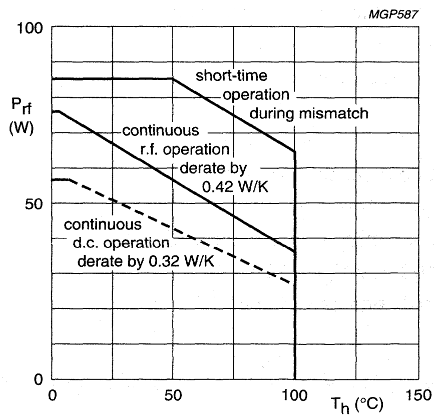


Fig.3 R.F. power dissipation; $V_{CE} \leq 28$ V; f ≥ 1 MHz.

THERMAL RESISTANCE

(dissipation = 35 W; $T_{mb} = 80$ °C, i.e. $T_h = 70$ °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	3,15	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	2,35	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 10 mA	$V_{(BR)CES}$	>	65	V
Collector-emitter breakdown voltage				
open base; I_C = 50 mA	$V_{(BR)CEO}$	>	36	V
Emitter-base breakdown voltage				
open collector; I_E = 10 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 36 V	I_{CES}	<	4	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	8	mJ
R_{BE} = 10 Ω	E_{SBR}	>	8	mJ
D.C. current gain (1)		typ.	50	
I_C = 1,25 A; V_{CE} = 5 V	h_{FE}	10 to 100		
D.C. current gain ratio of matched devices(1)				
I_C = 1,25 A; V_{CE} = 5 V	h_{FE1}/h_{FE2}	<	1,2	
Collector-emitter saturation voltage(1)				
I_C = 3,75 A; I_B = 0,75 A	V_{CEsat}	typ.	1,5	V
Transition frequency at f = 100 MHz(1)				
$-I_E$ = 1,25 A; V_{CB} = 28 V	f_T	typ.	530	MHz
$-I_E$ = 3,75 A; V_{CB} = 28 V	f_T	typ.	530	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 28 V	C_c	typ.	50	pF
Feedback capacitance at f = 1 MHz				
I_C = 100 mA; V_{CE} = 28 V	C_{re}	typ.	31	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200$ µs; $\delta \leq 0{,}02$.

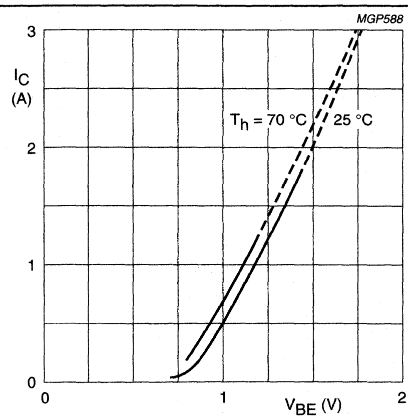


Fig.4 Typical values; V_{CE} = 28 V.

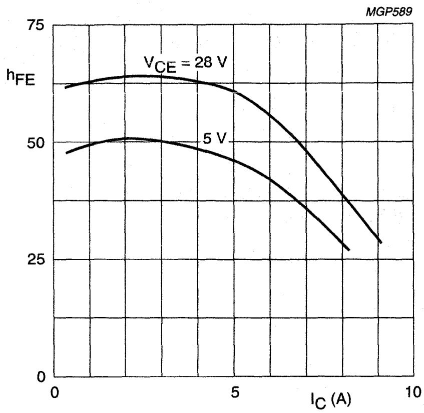


Fig.5 Typical values; T_j = 25 °C.

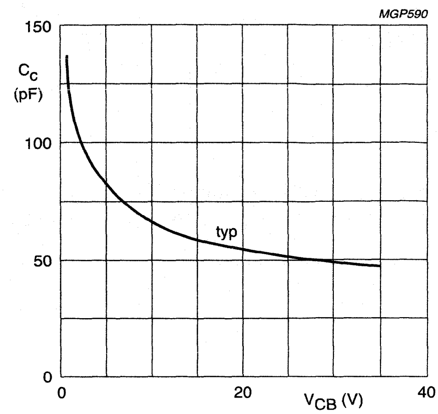


Fig.6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

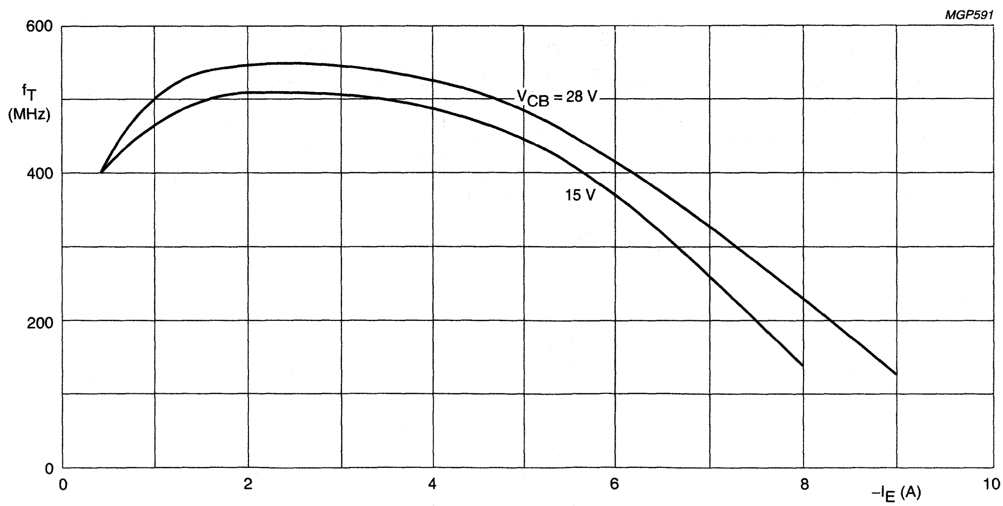


Fig.7 Typical values; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in s.s.b. class-A operation (linear power amplifier)
V_{CE} = 26 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_p dB	I_C A	d_3 dB(1)	d_5 dB(1)	T_h °C
> 10 (P.E.P.) typ. 11 (P.E.P.)	> 20	1,35	−40	< −40	70
typ. 12 (P.E.P.)	typ. 24	1,35	−40	< −40	25

Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

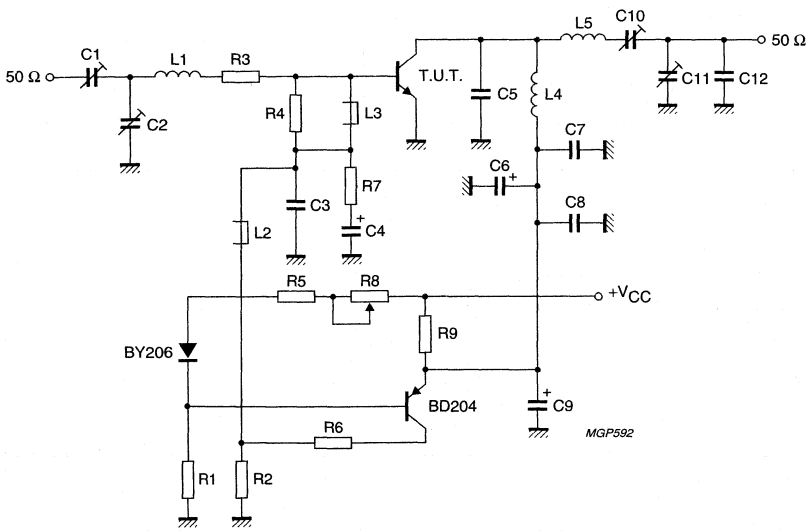


Fig.8 Test circuit; s.s.b. class-A.

List of components in Fig.8:

C1	=	C2 = 10 to 780 pF film dielectric trimmer
C3	=	22 nF ceramic capacitor (63 V)
C4	=	47 μF/10 V electrolytic capacitor
C5	=	56 pF ceramic capacitor (500 V)
C6	=	47 μF/35 V electrolytic capacitor
C7	=	C8 = 220 nF polyester capacitor
C9	=	10 μF/35 V electrolytic capacitor
C10	=	C11 = 7 to 100 pF film dielectric trimmer
C12	=	82 pF ceramic capacitor (500 V)
L1	=	3 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 9,0 mm; leads to 2 × 5 mm
L2	=	L3 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4	=	11 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 11,0 mm
L5	=	14 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 11,0 mm
R1	=	600 Ω; parallel connection of 2 × 1,2 kΩ carbon resistors (±5%; 0,5 W each)
R2	=	15 Ω carbon resistor (±5%; 0,25 W)
R3	=	1,2 Ω; parallel connection of 4 × 4,7 Ω carbon resistors (±5%; 0,125 W each)
R4	=	33 Ω carbon resistor (±5%; 0,25 W)
R5	=	18 Ω carbon resistor (±5%; 0,25 W)
R6	=	120 Ω wirewound resistor (±5%; 5,5 W)
R7	=	1 Ω carbon resistor (±5%; 0,125 W)
R8	=	47 Ω wirewound potentiometer (3 W)
R9	=	1,57 Ω; parallel connection of 3 × 4,7 Ω wirewound resistors (5%; 5,5 W each)

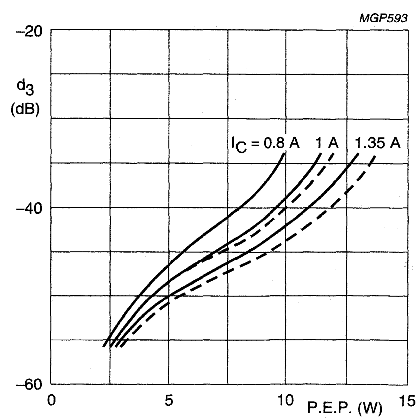


Fig.9 Intermodulation distortion as a function of output power.
Typical values; V_{CE} = 26 V; —— T_h = 70 °C; - - - T_h = 25 °C.

R.F. performance in s.s.b. class-AB operation (linear power amplifier)
V_{CE} = 28 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_p dB	η_{dt} (%) at 30 W P.E.P.	I_C (A) at 30 W P.E.P.	d_3 dB(1)	d_5 dB(1)	$I_{C(ZS)}$ mA	T_h °C
3 to 30 (P.E.P.)	typ. 21	typ. 40	typ. 1,34	typ. −30	< −30	25	25
3 to 25 (P.E.P.)	typ. 21	–	–	typ. −30	< −30	25	70

Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

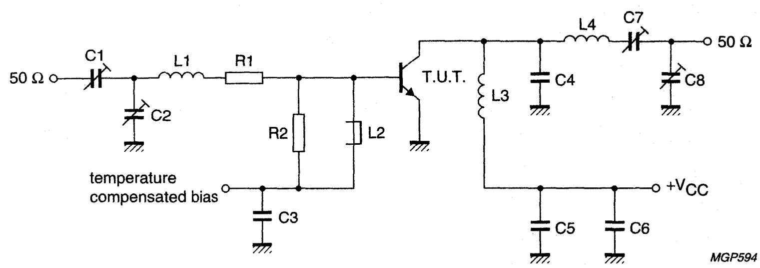
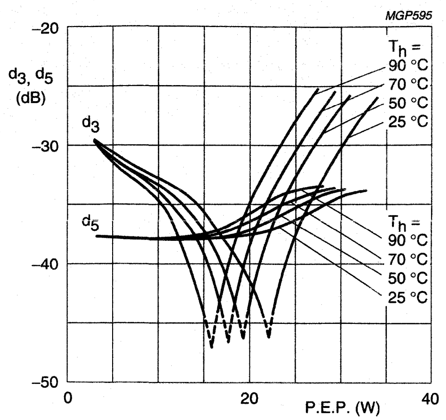


Fig.10 Test circuit; s.s.b. class-AB.

List of components:

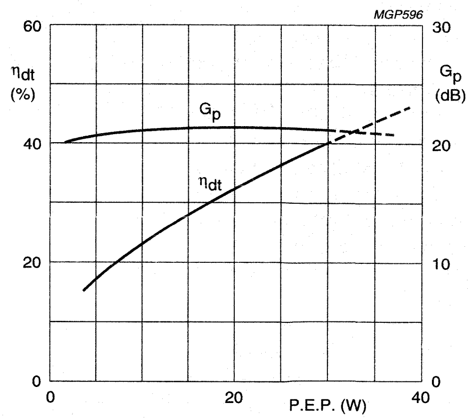
C1 = C2 = 10 to 780 pF film dielectric trimmer
C3 = C5 = C6 = 220 nF polyester capacitor
C4 = 56 pF ceramic capacitor (500 V)
C7 = C8 = 15 to 575 pF film dielectric trimmer
L1 = 4 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 7,0 mm; leads 2 × 5 mm
L2 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3 = 4 turns enamelled Cu wire (1,6 mm); int. dia. 10 mm; length 9,4 mm; leads 2 × 5 mm
L4 = 7 turns enamelled Cu wire (1,6 mm); int. dia. 12 mm; length 17,2 mm; leads 2 × 5 mm
R1 = 1,2 Ω; parallel connection of 4 × 4,7 Ω carbon resistors
R2 = 39 Ω carbon resistor

HF/VHF power transistor
BLW83



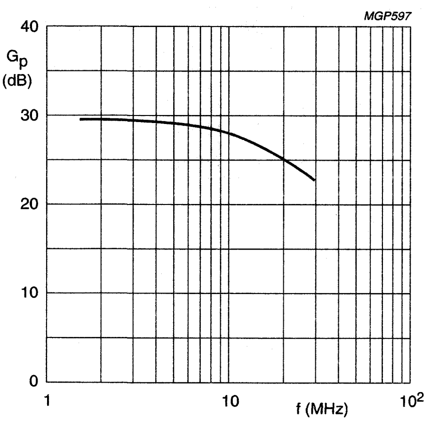
V_{CE} = 28 V; $I_{C(ZS)}$ = 25 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; typical values

Fig.11 Intermodulation distortion as a function of output power.(1)



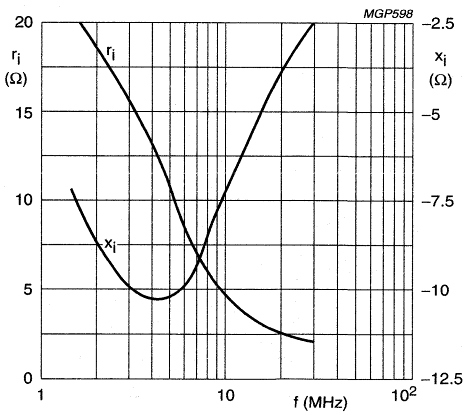
V_{CE} = 28 V; $I_{C(ZS)}$ = 25 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values

Fig.12 Double-tone efficiency and power gain as a function of output power.



V_{CE} = 28 V; $I_{C(ZS)}$ = 25 mA; P_L = 30 W; T_h = 25 °C; Z_L = 9,5 Ω

Fig.13 Power gain as a function of frequency.



V_{CE} = 28 V; $I_{C(ZS)}$ = 25 mA; P_L = 30 W; T_h = 25 °C; Z_L = 9,5 Ω

Fig.14 Input impedance (series components) as a function of frequency.

Figs 13 and 14 are typical curves and hold for an unneutralized amplifier in s.s.b. class-AB operation.

Ruggedness in s.s.b. operation

The BLW83 is capable of withstanding a load mismatch (VSWR = 50) under the following conditions:
f_1 = 28,000 MHz; f_2 = 28,001 MHz; V_{CE} = 28 V; T_h = 70 °C and P_{Lnom} = 35 W (P.E.P.).

HF/VHF power transistor BLW85

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, B and C operated mobile h.f. and v.h.f. transmitters with a nominal supply voltage of 12,5 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions with a supply over-voltage to 16,5 V. Matched h_{FE} groups are available on request.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	$\bar{z}_i$ Ω	$\bar{Z}_L$ Ω	d_3 dB
c.w. (class-B)	**12,5**	**175**	**45**	**> 4,5**	**> 75**	**1,4 + j1,5**	**2,7–j1,3**	–
s.s.b. (class-AB)	12,5	1,6–28	3–30 (P.E.P.)	typ. 19,5	typ. 35	–	–	typ. –33

PIN CONFIGURATION

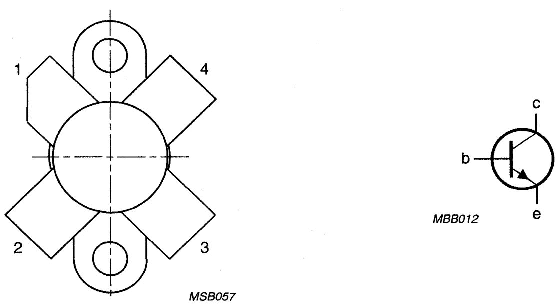


Fig.1 Simplified outline and symbol.

PINNING - SOT123

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage ($V_{BE} = 0$)				
peak value	V_{CESM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	16	V
Emitter-base voltage (open-collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	9	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	22	A
R.F. power dissipation up to (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	105	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

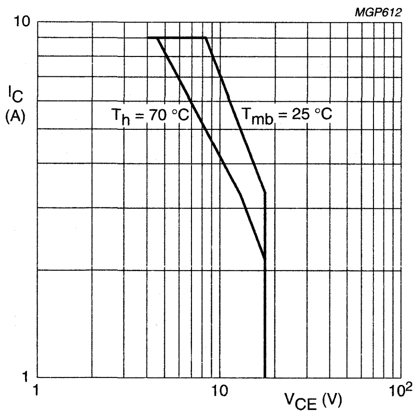


Fig.2 D.C. SOAR.

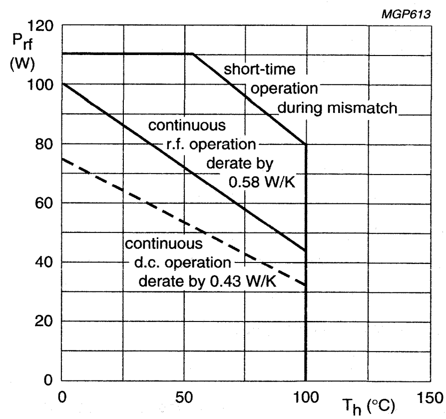


Fig.3 R.F. power dissipation; $V_{CE} \leq 16{,}5$ V; f ≥ 1 MHz.

THERMAL RESISTANCE

(dissipation = 30 W; T_{mb} = 79 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	2,5	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	1,8	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3	K/W

CHARACTERISTICS

T_j = 25 °C

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 50 mA	$V_{(BR)\,CES}$	>	36	V
Collector-emitter breakdown voltage				
open base; I_C = 100 mA	$V_{(BR)\,CEO}$	>	16	V
Emitter-base breakdown voltage				
open collector; I_E = 25 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 18 V	I_{CES}	<	25	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	8	mJ
R_{BE} = 10 Ω	E_{SBR}	>	8	mJ
D.C. current gain(1)		typ.	50	
I_C = 4 A; V_{CE} = 5 V	h_{FE}		10 to 80	
D.C. current gain ratio of matched devices(1)				
I_C = 4 A; V_{CE} = 5 V	h_{FE1}/h_{FE2}	<	1,2	
Collector-emitter saturation voltage(1)				
I_C = 12,5 A; I_B = 2,5 A	V_{CEsat}	typ.	1,5	V
Transition frequency at f = 100 MHz(1)				
$-I_E$ = 4 A; V_{CB} = 12,5 V	f_T	typ.	650	MHz
$-I_E$ = 12,5 A; V_{CB} = 12,5 V	f_T	typ.	600	MHz
Collector capacitance at f = 1 MHz				
I_E = I_e = 0; V_{CB} = 15 V	C_c	typ.	120	pF
Feedback capacitance at f = 1 MHz				
I_C = 200 mA; V_{CE} = 15 V	C_{re}	typ.	82	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \le 200$ µs; $\delta \le 0{,}02$.

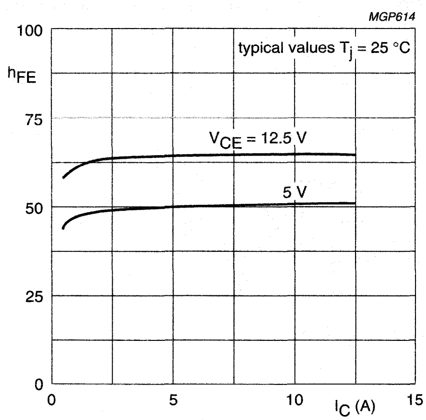


Fig.4

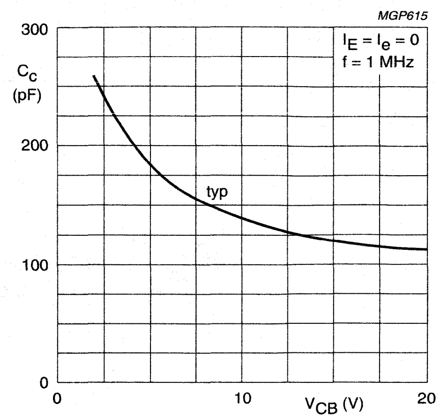


Fig.5 T_j = 25 °C.

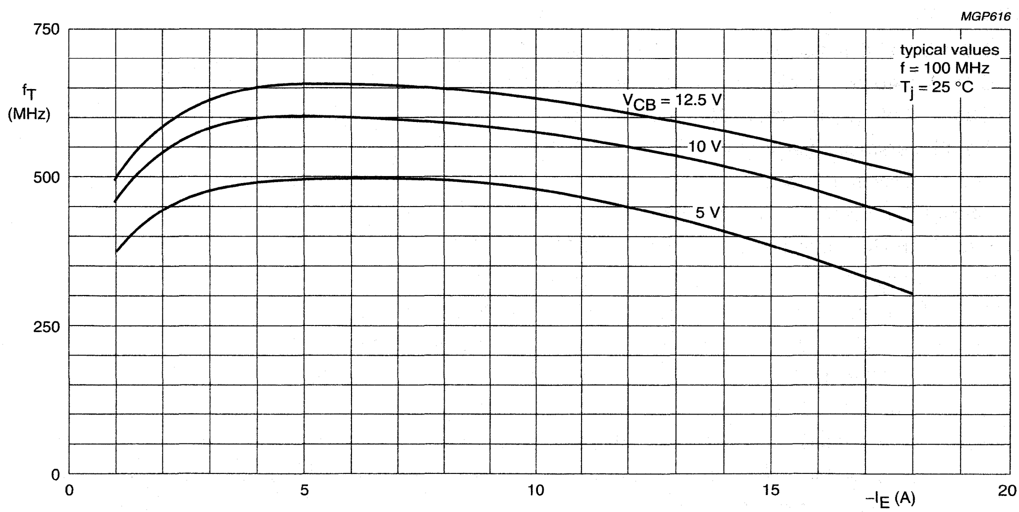


Fig.6

APPLICATION INFORMATION

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit); T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_p (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Z}_L$ (Ω)
175	**12,5**	**45**	**< 16**	**> 4,5**	**< 4,8**	**> 75**	**1,4 + j1,5**	**2,7 − j1,3**
175	13,5	45	–	typ. 6,0	–	typ. 75	–	–

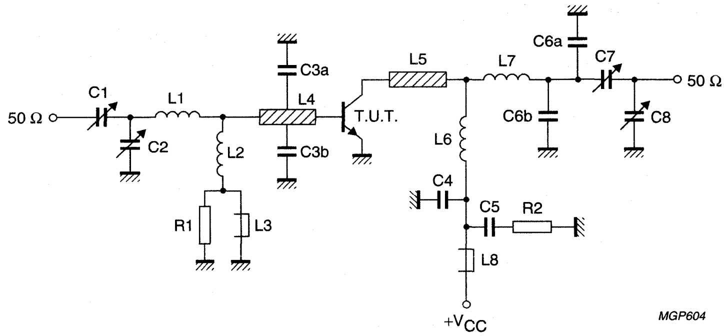


Fig.7 Test circuit; c.w. class-B.

List of components:

C1 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C2 = C8 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C3a = C3b = 47 pF ceramic capacitor (500 V)
C4 = 120 pF ceramic capacitor (500 V)
C5 = 100 nF polyester capacitor
C6a = C6b = 8,2 pF ceramic capacitor (500 V)
C7 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
L1 = 1 turn Cu wire (1,6 mm); int. dia. 9,0 mm; leads 2 × 5 mm
L2 = 100 nH; 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 × 5 mm
L3 = L8 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4 = L5 = strip (12 mm × 6 mm); taps for C3a and C3b at 5 mm from transistor
L6 = 2 turns enamelled Cu wire (1,6 mm); int. dia. 5,0 mm; length 6,0 mm; leads 2 × 5 mm
L7 = 2 turns enamelled Cu wire (1,6 mm); int. dia. 4,5 mm; length 6,0 mm; leads 2 × 5 mm

L4 and L5 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16".

R1 = 10 Ω (±10%) carbon resistor (0,25 W)
R2 = 4,7 Ω (±5%) carbon resistor (0,25 W)

Component layout and printed-circuit board for 175 MHz test circuit are shown in Fig.8.

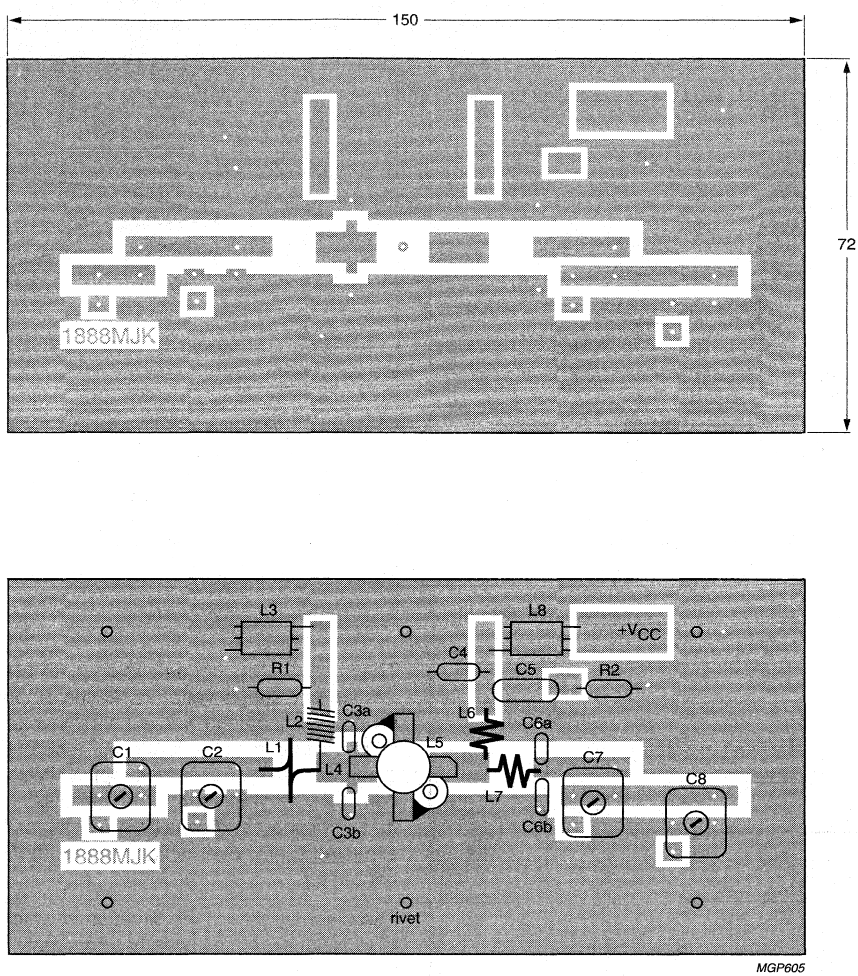


Fig.8 Component layout and printed-circuit board for 175 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

To minimize the dielectric losses, the ground plane under the interconnection of L7 and C7 has been removed.

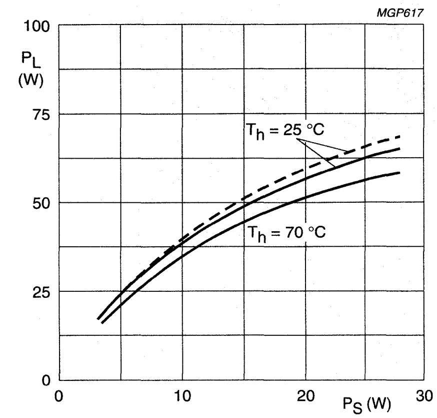


Fig.9 Typical values; f = 175 MHz;
— V_{CE} = 12,5 V; - - - V_{CE} = 13,5 V.

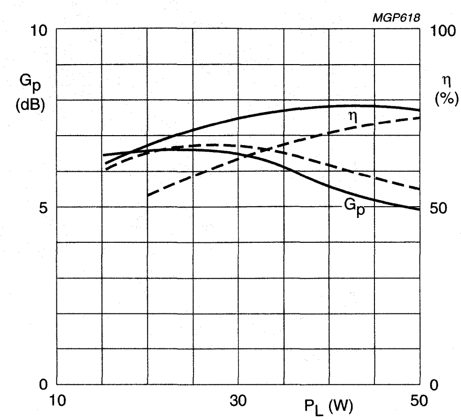


Fig.10 Typical values; f = 175 MHz ;T_h = 25 °C;
— V_{CE} = 12,5 V; - - - V_{CE} = 13,5 V.

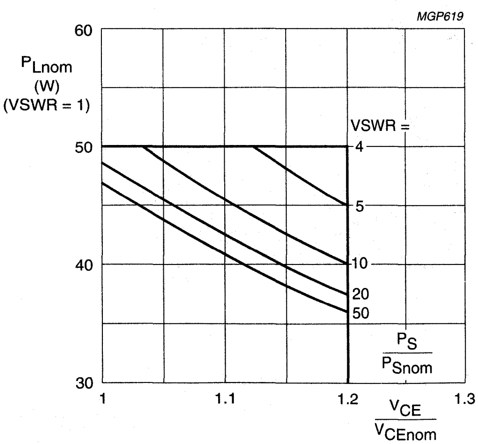
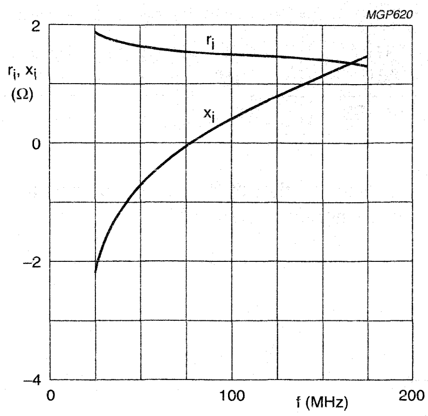


Fig.11 R.F. SOAR; (short-time operation during mismatch); f = 175 MHz; T_h = 70 °C;
$R_{th\ mb\text{-}h}$ = 0,3 K/W ;
V_{CEnom} = 12,5 V or 13,5 V; $P_S = P_{Snom}$ at V_{CEnom} and VSWR =1 measured in the circuit of Fig.7.

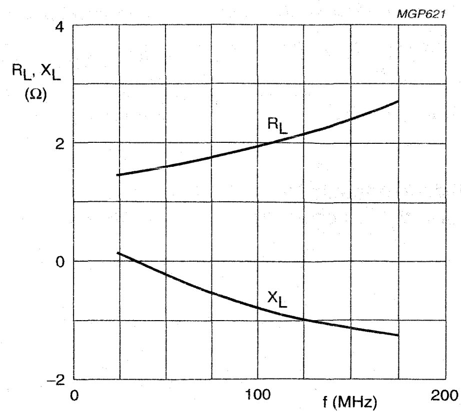
The transistor has been developed for use with unstabilized supply voltages. As the output power and drive power increase with the supply voltage, the nominal output power must be derated in accordance with the graph for safe operation at supply voltages other than the nominal. The graph shows the permissible output power under nominal conditions (VSWR = 1), as a function of the expected supply over-voltage ratio with VSWR as parameter.

The graph applies to the situation in which the drive (P_S/P_{Snom}) increases linearly with supply over-voltage ratio.



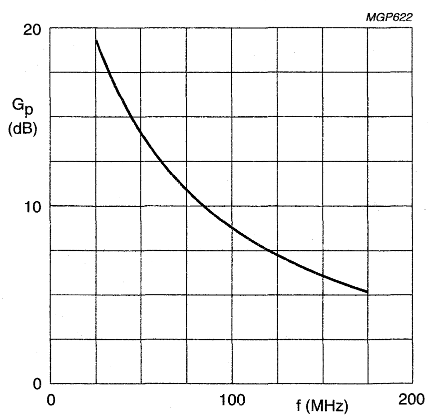
Typical values; V_{CE} = 12,5 V; P_L = 45 W;
class-B operation; T_h = 25 °C

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 12,5 V; P_L = 45 W;
class-B operation; T_h = 25 °C

Fig.13 Load impedance (series components).



Typical values; V_{CE} = 12,5 V; P_L = 45 W;
class-B operation; T_h = 25 °C

Fig.14

R.F. performance in s.s.b. class-AB operation
V_{CE} = 12,5 V; T_h up to 25 °C; $R_{th\ mb\text{-}h} \leq$ 0,3 K/W
f_1 = 28,000 MHz; f_2 = 28,001 Mhz

OUTPUT POWER W	G_p dB	η_{dt} %	d_3 dB(1)	d_5 dB(1)	$I_{C(ZS)}$ mA
3 to 30 (P.E.P.)	typ. 19,5	typ. 35	typ. −33	typ. −36	25

Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

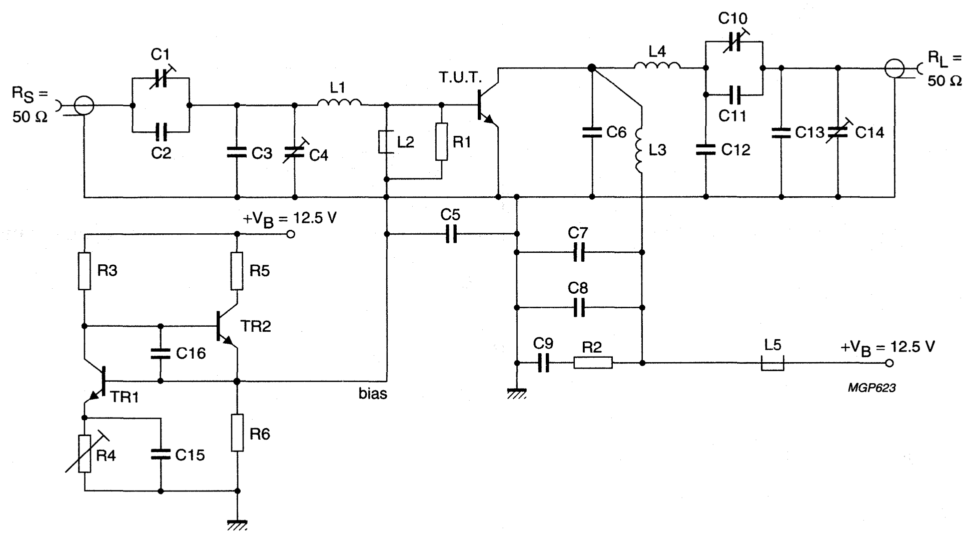
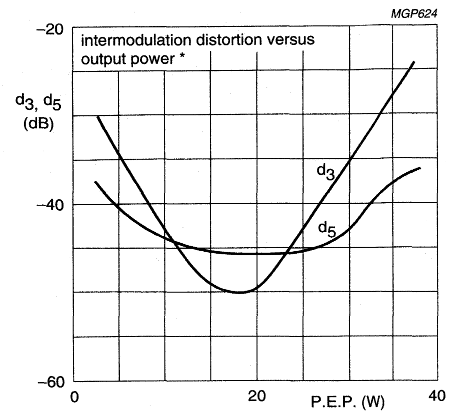


Fig.15 Test circuit; s.s.b. class-AB.

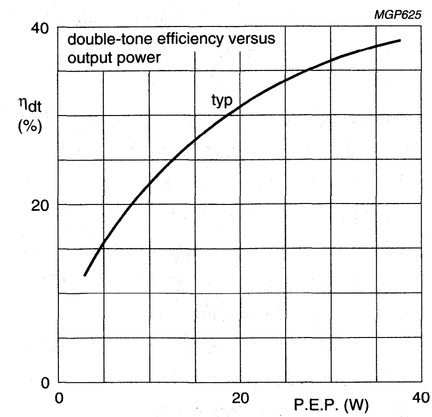
List of components:

TR1	=	TR2 = BD137
C1	=	100 pF air dielectric trimmer (single insulated rotor type)
C2	=	27 pF ceramic capacitor (500 V)
C3	=	180 pF polystyrene capacitor
C4	=	100 pF air dielectric trimmer (single non-insulated rotor type)
C5	=	C7 = 3,9 nF polyester capacitor
C6	=	2 × 270 pF polystyrene capacitors in parallel
C8	=	C15 = C16 = 100 nF polyester capacitor
C9	=	2,2 μF moulded metallized polyester capacitor
C10	=	2 × 385 pF (sections in parallel) film dielectric trimmer
C11	=	68 pF ceramic capacitor (500 V)
C12	=	2 × 82 pF ceramic capacitors in parallel (500 V)
C13	=	47 pF ceramic capacitor (500 V)
C14	=	385 pF film dielectric trimmer
L1	=	88 nH; 3 turns Cu wire (1,0 mm); int. dia. 9 mm; length 6,1 mm; leads 2 × 5 mm
L2	=	L5 = Ferroxcube choke coil (cat. no. 4312 020 36640)
L3	=	68 nH; 3 turns enamelled Cu wire (1,6 mm); int. dia. 8 mm; length 8,3 mm; leads 2 × 5 mm
L4	=	96 nH; 3 turns enamelled Cu wire (1,6 mm); int. dia. 10 mm; length 7,6 mm; leads 2 × 5 mm
R1	=	27 Ω (±5%) carbon resistor (0,5 W)
R2	=	4,7 Ω (±5%) carbon resistor (0,25 W)
R3	=	1,5 kΩ (±5%) carbon resistor (0,5 W)
R4	=	10 Ω wirewound potentiometer (3 W)
R5	=	47 Ω wirewound resistor (5,5 W)
R6	=	150 Ω (±5%) carbon resistor (0,25 W)



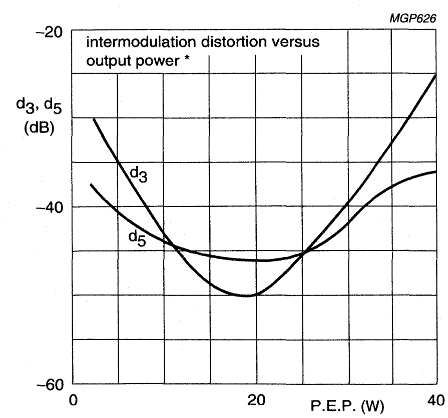
V_{CE} = 12,5 V; f_1 = 28,000 Mhz; f_2 = 28,001 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ ≤ 0,3 °K/W; $I_{C(ZS)}$ = 25 mA; typical values.

Fig.16



V_{CE} = 12,5 V; f_1 = 28,000 Mhz; f_2 = 28,001 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ ≤ 0,3 °K/W; $I_{C(ZS)}$ = 25 mA; typical values.

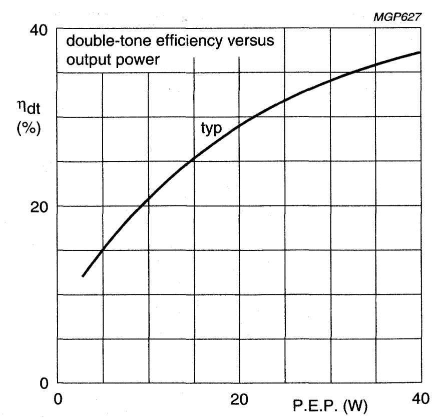
Fig.17



V_{CE} = 13,5 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ ≤ 0,3 K/W ; $I_{C(ZS)}$ = 25 mA; typical values.

* Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

Fig.18



V_{CE} = 13,5 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ ≤ 0,3 K/W ; $I_{C(ZS)}$ = 25 mA; typical values.

Fig.19

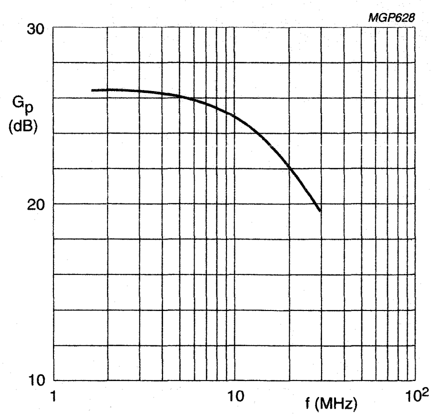


Fig.20 Power gain as a function of frequency.

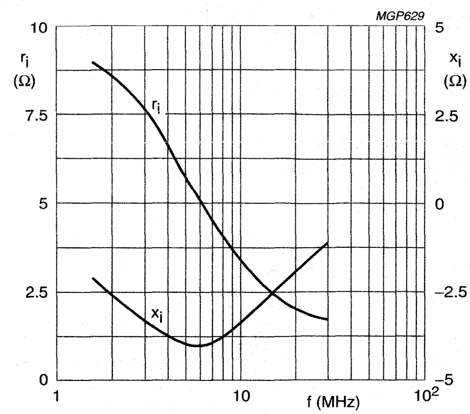


Fig.21 Input impedance (series components) as a function of frequency.

Fig. 20 and 21 are typical curves and hold for an unneutralized amplifier in s.s.b. class-AB operation.

Conditions:

V_{CE} = 12, 5 V	V_{CE} = 13, 5 V
P_L = 30 W (P.E.P.)	P_L = 35 W (P.E.P.)
T_h = 25 °C	T_h = 25 °C
$R_{th\ mb-h} \leq$ 0,3 K/W	$R_{th\ mb-h} \leq$ 0,3 K/W
$I_{C(ZS)}$ = 25 mA	$I_{C(ZS)}$ = 25 mA
Z_L = 1,8 Ω	Z_L = 1,8 Ω

HF/VHF power transistor BLW86

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, AB and B operated h.f. and v.h.f. transmitters with a nominal supply voltage of 28 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions. Matched h_{FE} groups are available on request.

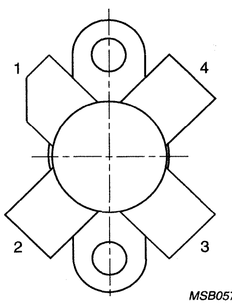
It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	$\bar{z}_i$ Ω	$\bar{Y}_L$ mS	d_3 dB
c.w. (class-B)	**28**	**175**	**45**	> **7,5**	> **70**	**0,7 + j1,3**	**110 − j62**	−
s.s.b. (class-AB)	28	1,6 − 28	5–47,5 (P.E.P.)	typ. 19	typ. 45	−	−	typ. −30
s.s.b. (class-A)	26	1,6 − 28	17 (P.E.P.)	typ. 22	−	−	−	typ. −42

PIN CONFIGURATION



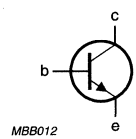


Fig.1 Simplified outline and symbol.

PINNING - SOT123

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	65	V
Collector-emitter voltage (open base)	V_{CEO}	max.	36	V
Emitter-base voltage (open-collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	4	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	12	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	105	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

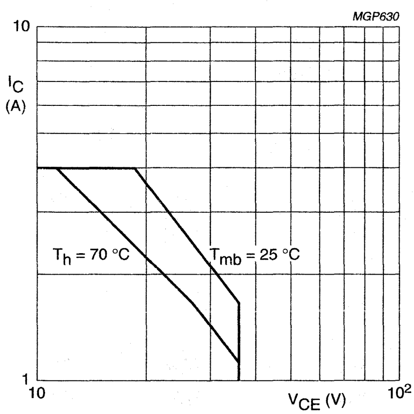
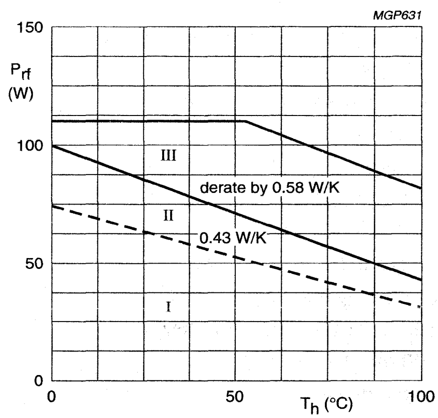


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \leq 28$ V; f > 1 MHz.

THERMAL RESISTANCE

(dissipation = 45 W; T_{mb} = 83,5 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	2,65	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	1,95	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 25 mA	$V_{(BR)CES}$	>	65	V
Collector-emitter breakdown voltage				
open base; I_C = 100 mA	$V_{(BR)CEO}$	>	36	V
Emitter-base breakdown voltage				
open collector; I_E = 10 mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{BE} = 0; V_{CE} = 36 V	I_{CES}	<	10	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	8	mJ
R_{BE} = 10 Ω	E_{SBR}	>	8	mJ
D.C. current gain(1)				
I_C = 2,5 A; V_{CE} = 5 V	h_{FE}	typ.	45	
			10 to 80	
D.C. current gain ratio of matched devices(1)				
I_C = 2,5 A; V_{CE} = 5 V	h_{FE1}/h_{FE2}	<	1,2	
Collector-emitter saturation voltage(1)				
I_C = 7,5 A; I_B = 1,5 A	V_{CEsat}	typ.	1,5	V
Transition frequency at f = 100 MHz(1)				
$-I_E$ = 2,5 A; V_{CB} = 28 V	f_T	typ.	570	MHz
$-I_E$ = 7,5 A; V_{CB} = 28 V	f_T	typ.	570	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 28 V	C_c	typ.	82	pF
Feedback capacitance at f = 1 MHz				
I_C = 100 mA; V_{CE} = 28 V	C_{re}	typ.	54	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0{,}02$.

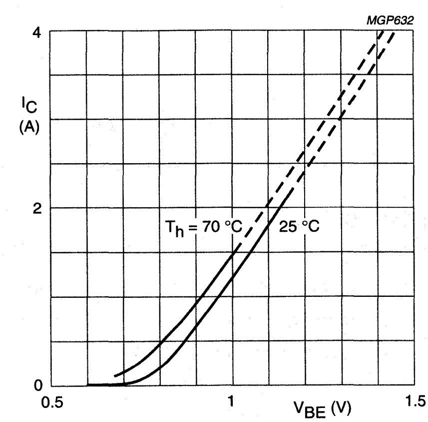


Fig.4 Typical values; V_{CE} = 28 V.

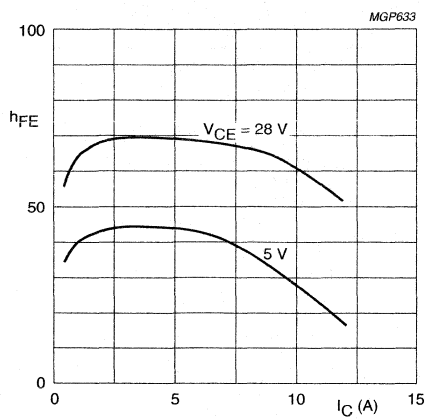


Fig.5 Typical values; T_j = 25 °C.

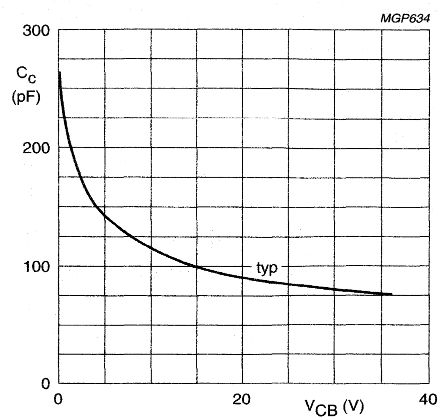


Fig.6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

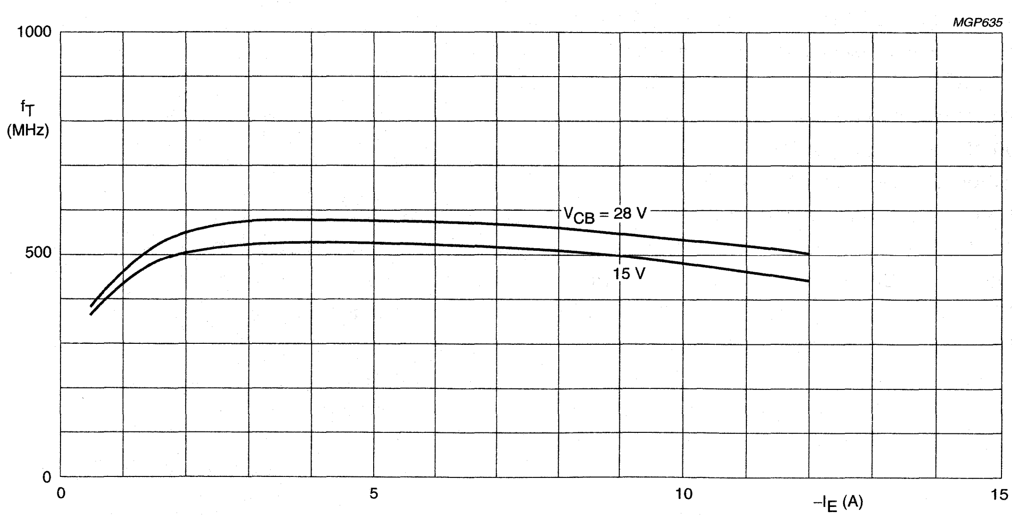


Fig.7 Typical values; f = 100 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit); T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_P (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
175	28	45	< 8	> 7,5	< 2,47	> 70	0,7 + j1,3	110 − j62

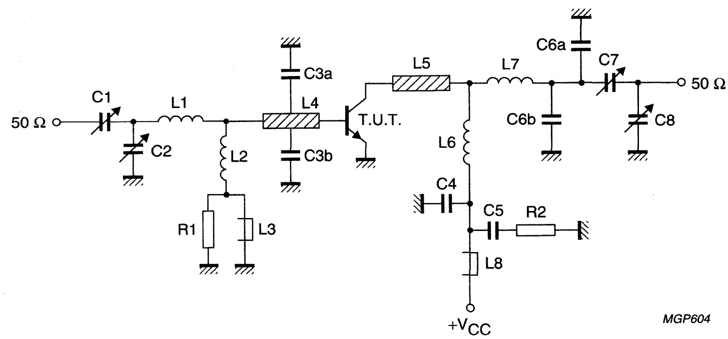


Fig.8 Test circuit; c.w. class-B.

List of components:

C1 = C7 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)

C2 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)

C3a = C3b = 47 pF ceramic capacitor (500 V)

C4 = 120 pF ceramic capacitor

C5 = 100 nF polyester capacitor

C6a = 2,2 pF ceramic capacitor (500 V)

C6b = 1,8 pF ceramic capacitor (500 V)

C8 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)

L1 = 14 nH; 1 turn Cu wire (1,6 mm); int. dia. 7,7 mm; leads 2 × 5 mm

L2 = 100 nH; 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 × 5 mm

L3 = L8 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)

L4 = L5 = strip (12 mm × 6 mm); taps for C3a and C3b at 5 mm from transistor

L6 = 80 nH; 3 turns Cu wire (1,6 mm); int. dia. 9,0 mm; length 8,0 mm; leads 2 × 5 mm

L7 = 62 nH; 3 turns Cu wire (1,6 mm); int. dia. 7,5 mm; length 8,1 mm; leads 2 × 5 mm

L4 and L5 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/6".

R1 = R2 = 10 Ω carbon resistor

Component layout and printed-circuit board for 175 MHz test circuit see Fig.9.

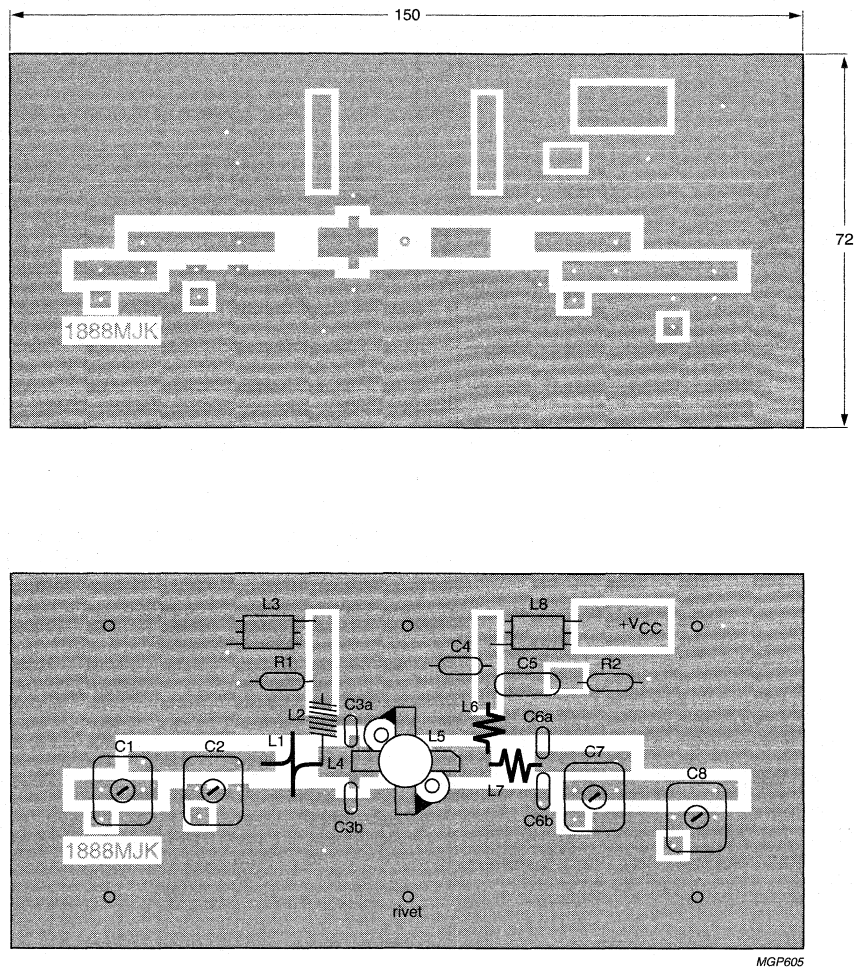


Fig.9 Component layout and printed-circuit board for 175 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

To minimize the dielectric losses, the ground plane under the interconnection of L7 and C7 has been removed.

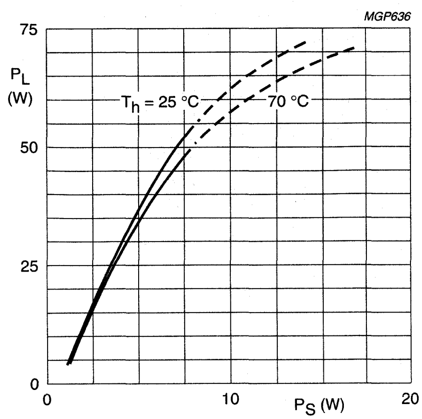


Fig.10 Typical values; V_{CE} = 28 V; f = 175 MHz.

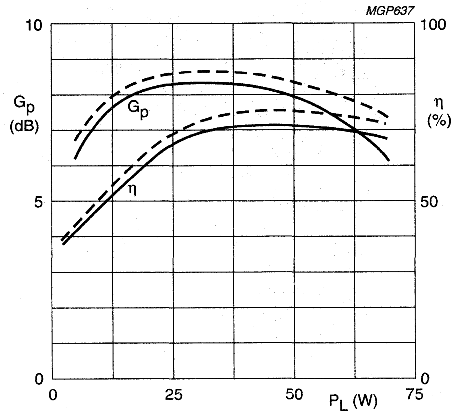
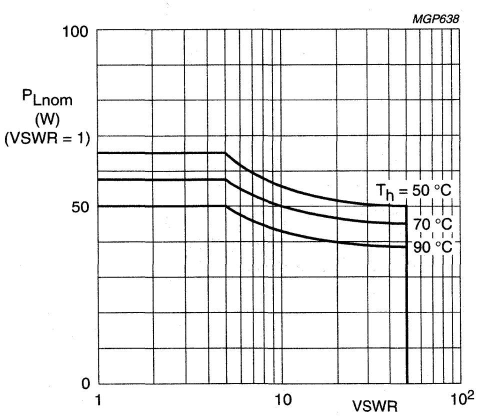
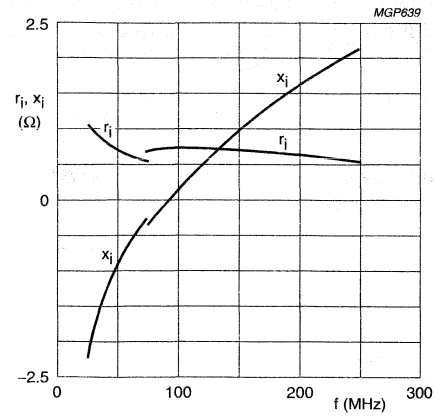


Fig.11 Typical values; V_{CE} = 28 V; f = 175 MHz;
– – – T_h = 25 °C; —— T_h = 70 °C.



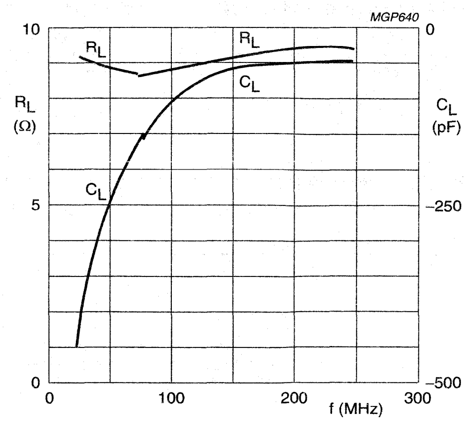
The graph shows the permissible output power under nominal conditions (VSWR = 1) as a function of the expected VSWR during short-time mismatch conditions with heatsink temperatures as parameter.

Fig.12 R.F. SOAR; c.w. class-B operation;
f = 175 MHz; V_{CE} = 28 V; $R_{th\ mb-h}$ = 0,3 K/W



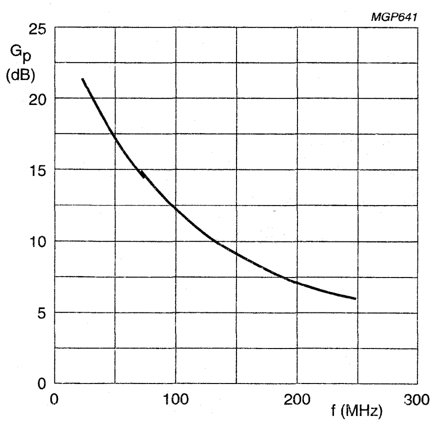
Typical values; V_{CE} = 28 V; P_L = 45 W; T_h = 25 °C.

Fig.13 Input impedance (series components).



Typical values; V_{CE} = 28 V; P_L = 45 W; T_h = 25 °C.

Fig.14 Load impedance (parallel components).



Typical values; V_{CE} = 28 V; P_L = 45 W; T_h = 25 °C.

Fig.15 Power gain versus frequency.

OPERATING NOTE

Below 75 MHz a base-emitter resistor of 10 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.

R.F. performance in s.s.b. class-AB operation (linear power amplifier)
V_{CE} = 28 V; f_1 = 28,000; f_2 = 28,001 MHz.

OUTPUT POWER W	G_P dB	η_{dt} (%) at 47,5 W	I_C (A) (P.E.P.)	d_3 dB(1)	d_5 dB(1)	$I_{C(ZS)}$ mA	T_h °C
5 to 47,5 (P.E.P.)	typ. 19	typ. 45	typ. 1,9	typ. −30	< −30	50	25
5 to 42,5 (P.E.P.)	typ. 19	−	−	typ. −30	< −30	50	70

Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

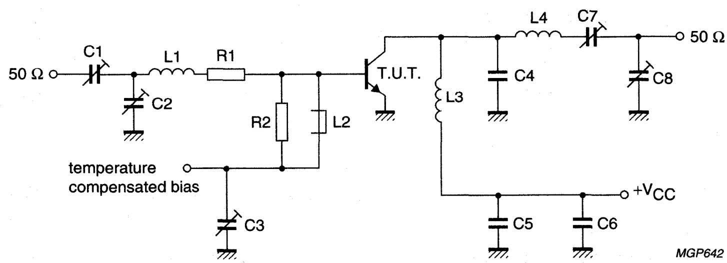
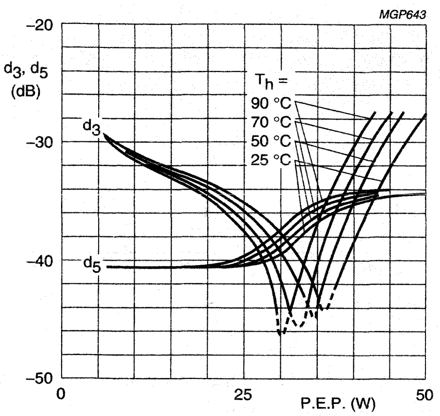


Fig.16 Test circuit; s.s.b. class-AB.

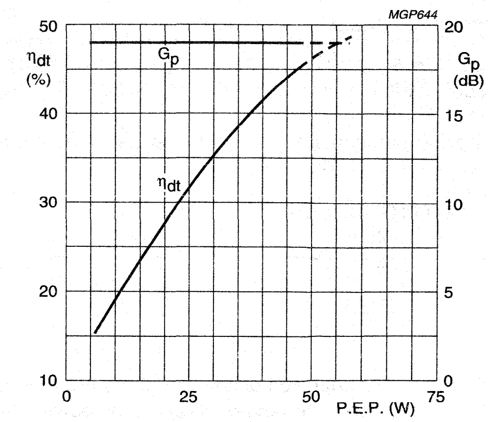
List of components:

C1 = C2 = 10 to 780 pF film dielectric trimmer
C3 = C5 = C6 = 220 nF polyester capacitor
C4 = 56 pF ceramic capacitor (500 V)
C7 = C8 = 15 to 575 pF film dielectric trimmer
L1 = 4 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 7,0 mm; leads 2 × 5 mm
L2 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3 = 4 turns enamelled Cu wire (1,6 mm); int. dia. 10 mm; length 9,4 mm; leads 2 × 5 mm
L4 = 7 turns enamelled Cu wire (1,6 mm); int. dia. 12 mm; length 17,2 mm; leads 2 × 5 mm
R1 =1,2 Ω; parallel connection of 4 × 4,7 Ω carbon resistors
R2 = 39 Ω carbon resistor



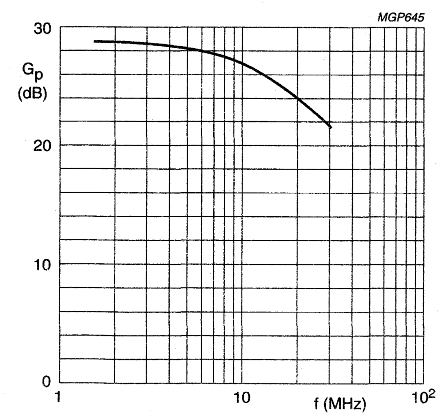
V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; typical values.

Fig.17 Intermodulation distortion as a function of output power.(1)



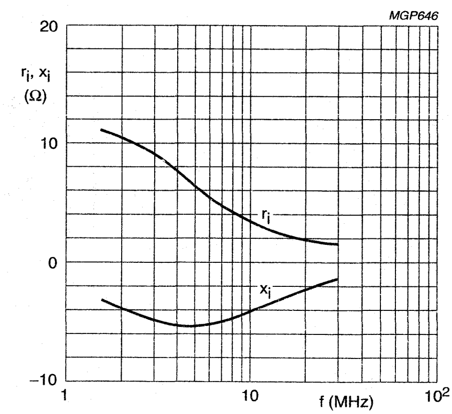
V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

Fig.18 Double-tone efficiency and power gain as a function of output power.



V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; P_L = 47,5 W;
T_h = 25 °C; Z_L = 6,4 Ω.

Fig.19 Power gain as a function of frequency.



V_{CE} = 28 V; $I_{C(ZS)}$ = 50 mA; P_L = 47,5 W;
T_h = 25 °C; Z_L = 6,4 Ω.

Fig.20 Input impedance (series components) as a function of frequency.

Figs 19 and 20 are typical curves and hold for an unneutralized amplifier in s.s.b. class-AB operation.

Ruggedness in s.s.b. operation

The BLW86 is capable of withstanding a load mismatch (VSWR = 50) under the following conditions: class-AB operation; f_1 = 28,000 MHz; f_2 = 28,001 MHz; V_{CE} = 28 V; T_h = 70 °C and P_{Lnom} = 50 W P.E.P.

R.F. performance in s.s.b. class-A operation (linear power amplifier)
V_{CE} = 26 V; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_P dB	I_C A	d_3 dB(1)	d_5 dB(1)	T_h °C
17 (P.E.P.)	typ. 22	1,7	typ. −40	< −40	70
17 (P.E.P.)	typ. 22	1,7	typ. −42	< −40	25

Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

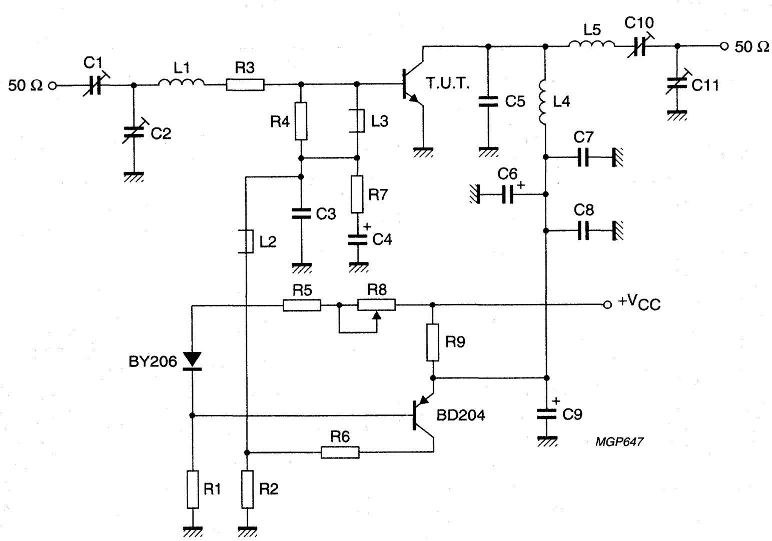


Fig.21 Test circuit; s.s.b. class-A.

List of components in Fig.21:

C1 = C2 = 10 to 780 pF film dielectric trimmer
C3 = 22 nF ceramic capacitor (63 V)
C4 = 47 μF/10 V electrolytic capacitor
C5 = 56 pF ceramic capacitor (500 V)
C6 = 47 μF/35 V electrolytic capacitor
C7 = C8 = 220 nF polyester capacitor
C9 = 10 μF/35 V electrolytic capacitor
C10 = 10 to 210 pF film dielectric trimmer
C11 = 15 to 575 pF film dielectric trimmer
L1 = 3 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 9,0 mm; leads 2 × 5 mm
L2 = L3 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4 = 11 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 11,0 mm
L5 = 14 turns closely wound enamelled Cu wire (1,6 mm); int. dia. 11,0 mm
R1 = 600 Ω; parallel connection of 2 × 1,2 kΩ carbon resistors (±5%; 0,5 W each)
R2 = 15 Ω carbon resistor (±5%; 0,25 W)
R3 = 1,2 Ω; parallel connection of 4 × 4,7 Ω carbon resistors (±5%; 0,125 W each)
R4 = 33 Ω carbon resistor (±5%; 0,25 W)
R5 = 18 Ω carbon resistor (±5%; 0,25 W)
R6 = 120 Ω wirewound resistor (±5%; 5,5 W)
R7 = 1 Ω carbon resistor (±5%; 0,125 W)
R8 = 47 Ω wirewound potentiometer (3 W)
R9 = 1,57 Ω; parallel connection of 3 × 4,7 Ω wirewound resistors (±5%; 5,5 W each)

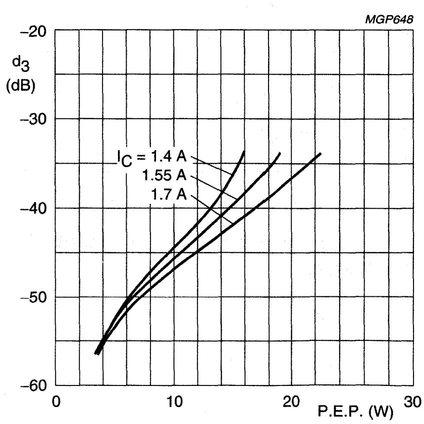


Fig.22 Intermodulation distortion as a function of output power. Typical values; V_{CE} = 26 V; T_h = 70 °C; f_1 = 28,000 MHz; f_2 = 28,001 MHz.

VHF power transistor BLW87

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, B and C operated mobile h.f. and v.h.f. transmitters with a nominal supply voltage of 13,5 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions with a supply over-voltage to 16,5 V.

It has a 3/8" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in an unneutralized common-emitter class-B circuit

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	$\bar{z}_i$ Ω	$\bar{Y}_L$ mS
c.w.	13,5	175	25	> 6	> 70	1,6 + j1,4	210 + j5,5

PIN CONFIGURATION

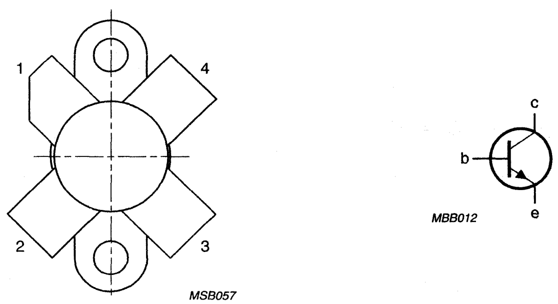


Fig.1 Simplified outline and symbol.

PINNING - SOT123

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	18	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	6	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	12	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	76	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

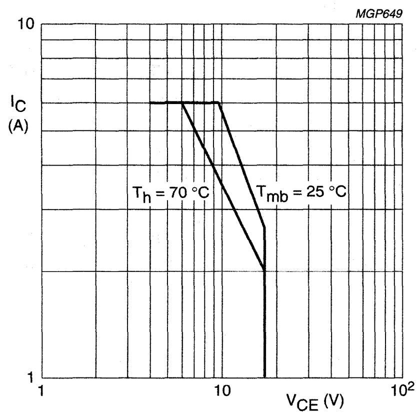


Fig.2 D.C. SOAR.

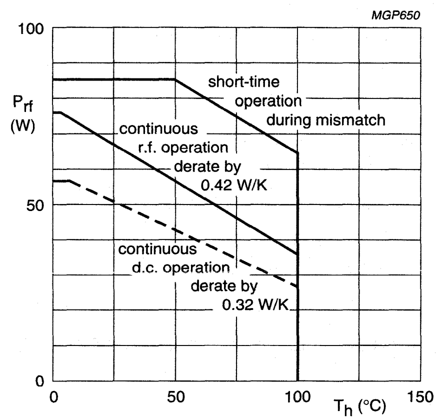


Fig.3 R.F. power dissipation; V_{CE} ≤ 16,5 V; f ≥ 1 MHz.

THERMAL RESISTANCE

(dissipation = 20 W; T_{mb} = 76 °C; i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	3,0	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	2,25	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,3	K/W

CHARACTERISTICS

$T_j = 25\ °C$

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 25$ mA	$V_{(BR)\ CES}$	>	36	V
Collector-emitter breakdown voltage				
open base; $I_C = 50$ mA	$V_{(BR)\ CEO}$	>	18	V
Emitter-base breakdown voltage				
open collector; $I_E = 10$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 18$ V	I_{CES}	<	10	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	8	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>	8	mJ
D.C. current gain(1)		typ.	50	
$I_C = 2,5$ A; $V_{CE} = 5$ V	h_{FE}		10 to 80	
Collector-emitter saturation voltage(1)				
$I_C = 7,5$ A; $I_B = 1,5$ A	V_{CEsat}	typ.	1,7	V
Transition frequency at f = 100 MHz(1)				
$-I_E = 2,5$ A; $V_{CB} = 13,5$ V	f_T	typ.	800	MHz
$-I_E = 7,5$ A; $V_{CB} = 13,5$ V	f_T	typ.	750	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 15$ V	C_c	typ.	65	pF
Feedback capacitance at f = 1 MHz				
$I_C = 100$ mA; $V_{CE} = 15$ V	C_{re}	typ.	41	pF
Collector-flange capacitance	C_{cf}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0,02$.

VHF power transistor

BLW87

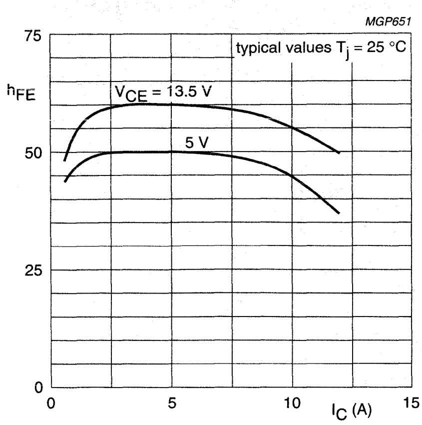


Fig.4

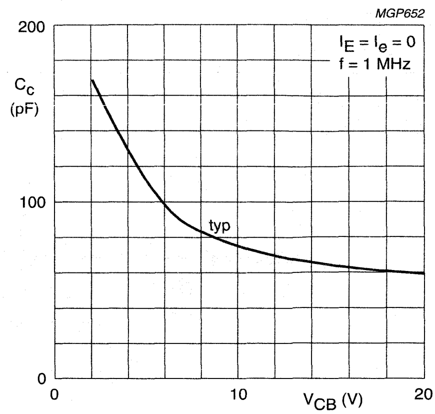


Fig.5 T_j = 25 °C.

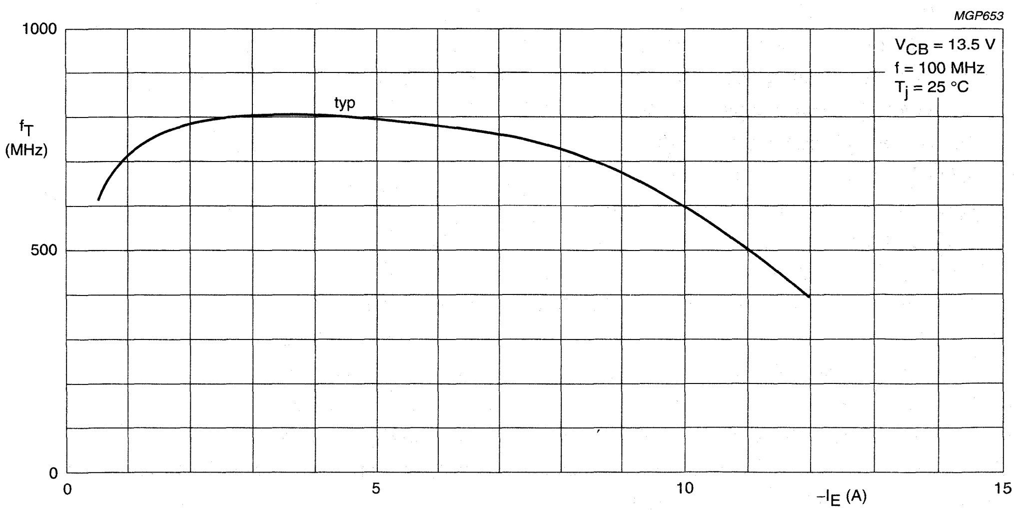


Fig.6

APPLICATION INFORMATION

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit); $T_h = 25$ °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_P (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
175	**13,5**	**25**	**< 6,25**	**> 6**	**< 2,64**	**> 70**	**1,6 + j1,4**	**210 + j5,5**
175	12,5	25	–	typ. 6,6	–	typ. 75	–	–

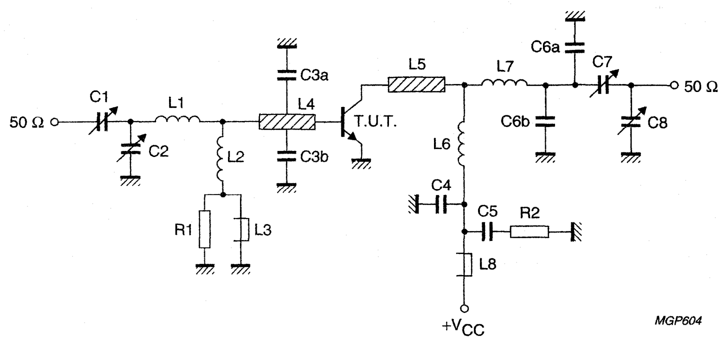


Fig.7 Test circuit; c.w. class-B.

List of components:

C1 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C2 = C8 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C3a = C3b = 47 pF ceramic capacitor (500 V)
C4 = 120 pF ceramic capacitor (500 V)
C5 = 100 nF polyester capacitor
C6a = C6b = 8,2 pF ceramic capacitor (500 V)
C7 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
L1 = 1 turn Cu wire (1,6 mm); int. dia. 9,0 mm; leads 2 × 5 mm
L2 = 100 nH; 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm; leads 2 × 5 mm
L3 = L8 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L4 = L5 = strip (12 mm × 6 mm); taps for C3a and C3b at 5 mm from transistor
L6 = 2 turns Cu wire (1,6 mm); int. dia. 5,0 mm; length 6,0 mm; leads 2 × 5 mm
L7 = 2 turns Cu wire (1,6 mm); int. dia. 4,5 mm; length 6,0 mm; leads 2 × 5 mm
L4 and L5 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16".
R1 = 10 Ω (± 10%) carbon resistor (0,25 W)
R2 = 4,7 Ω (± 5%) carbon resistor (0,25 W)

Component layout and printed-circuit board for 175 MHz test circuit are shown in Fig.8.

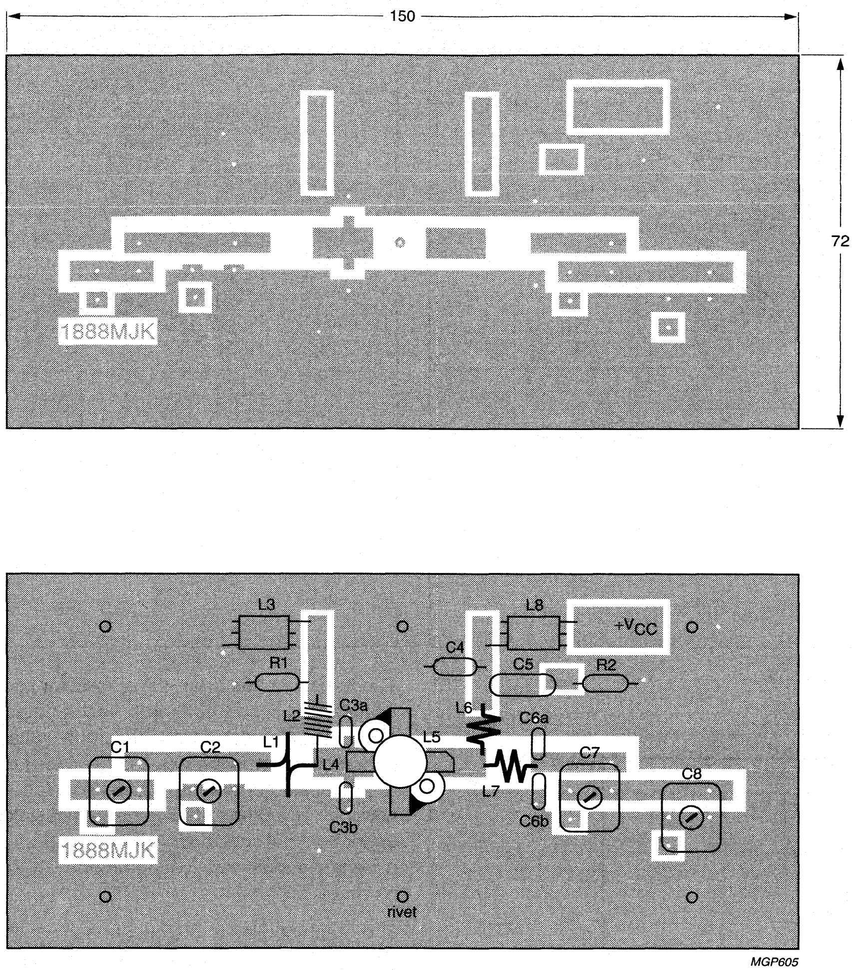


Fig.8 Component layout and printed-circuit board for 175 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

VHF power transistor BLW87

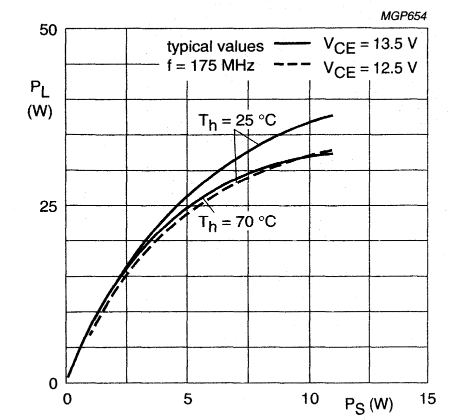


Fig.9

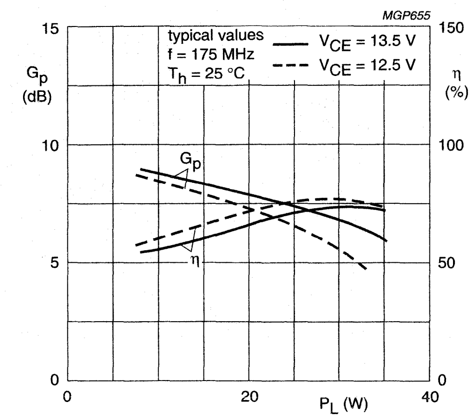


Fig.10

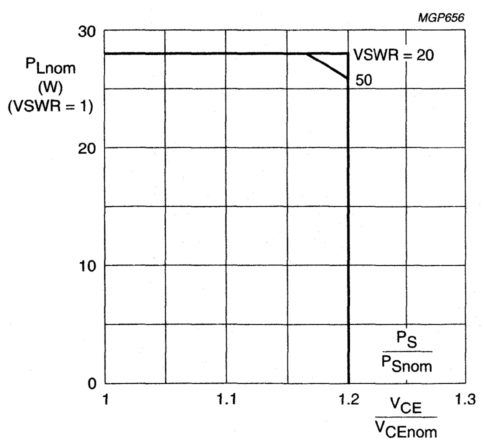


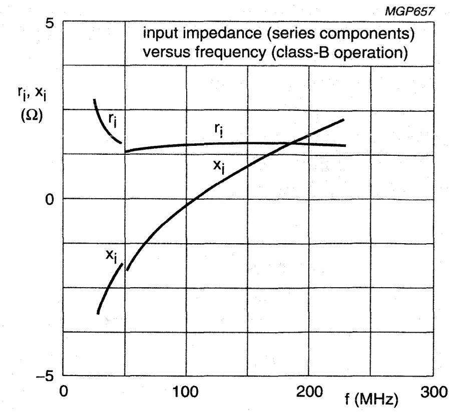
Fig.11 R.F. SOAR (short-time operation during mismatch); f = 175 MHz; T_h = 70 °C; $R_{th\ mb\text{-}h}$ = 0,3 K/W; V_{CEnom} = 13,5 V or 12,5 V; $P_S = P_{Snom}$ at V_{CEnom} and VSWR =1; measured in the circuit of Fig.7.

The transistor has been developed for use with unstabilized supply voltages. As the output power and drive power increase with the supply voltage, the nominal output power must be derated in accordance with the graph for safe operation at supply voltages other than the nominal. The graph shows the permissible output power under nominal conditions (VSWR = 1), as a function of the expected supply over-voltage ratio with VSWR as parameter.

The graph applies to the situation in which the drive (P_S/P_{Snom}) increases linearly with supply over-voltage ratio.

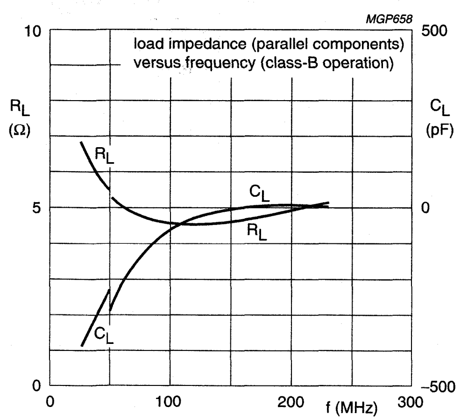
OPERATING NOTE

Below 50 MHz a base-emitter resistor of 10 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.



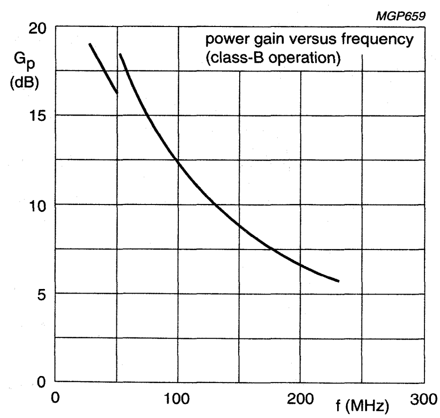
Typical values; V_{CE} = 13,5 V; P_L = 25 W; T_h = 25 °C.

Fig.12



Typical values; V_{CE} = 13,5 V; P_L = 25 W; T_h = 25 °C.

Fig.13



Typical values; V_{CE} = 13,5 V; P_L = 25 W; T_h = 25 °C.

Fig.14

HF/VHF power transistor — BLW96

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, AB and B operated high power industrial and military transmitting equipment in the h.f. and v.h.f. band. The transistor presents excellent performance as a linear amplifier in s.s.b. applications. It is resistance stabilized and is guaranteed to withstand severe load mismatch conditions. Transistors are supplied in matched h_{FE} groups.

The transistor has a ½" flange envelope with a ceramic cap. All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	d_3 dB	d_5 dB	$I_{C(ZS)}$ (I_C) A
s.s.b. (class-AB)	**50**	**1,6 – 28**	**25 – 200 (P.E.P.)**	> 13,5	> **40**(1)	< **−30**	< **−30**	**0,1**
c.w. (class-B)	50	108	200	typ. 6,5	typ. 67	–	–	(6)
s.s.b. (class-A)	40	28	50 (P.E.P.)	typ. 19	–	typ. −40	< −40	(4)

Note

1. η_{dt} at 200 W P.E.P.

PIN CONFIGURATION

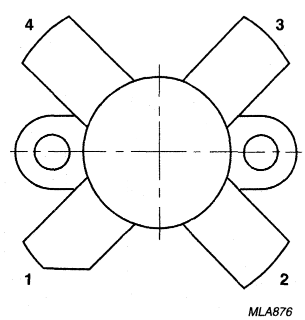


Fig.1 Simplified outline. SOT121B.

PINNING - SOT121B.

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	110	V
Collector-emitter voltage (open base)	V_{CEO}	max.	55	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	12	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	40	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 45 °C	P_{rf}	max.	340	W
Storage temperature	T_{stg}	–65 to + 150		°C
Operating junction temperature	T_j	max.	200	°C

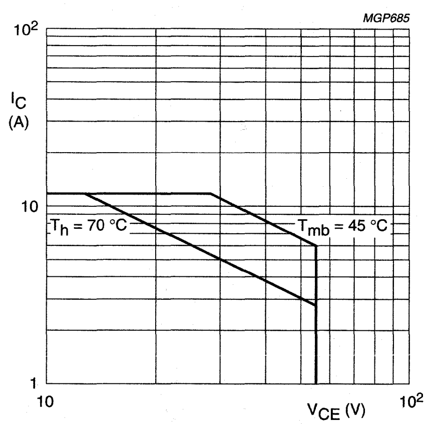
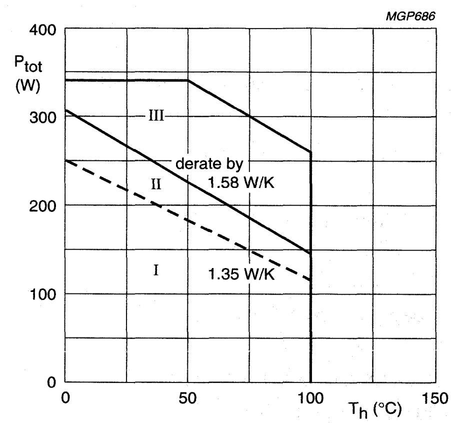


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation; f > 1 MHz
III Short-time operation during mismatch; f > 1 MHz

Fig.3 Power/temperature derating curves.

THERMAL RESISTANCE

(dissipation = 150 W; T_{mb} = 100 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	0,63	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	0,45	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,2	K/W

CHARACTERISTICS

$T_j = 25\ °C$

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 50$ mA	$V_{(BR)CES}$	>	110	V
Collector-emitter breakdown voltage				
open base; $I_C = 200$ mA	$V_{(BR)CEO}$	>	55	V
Emitter-base breakdown voltage				
open collector; $I_E = 20$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 55$ V	I_{CES}	<	10	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	20	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>	20	mJ
D.C. current gain(1)				
$I_C = 7$ A; $V_{CE} = 5$ V	h_{FE}	typ.	30	
		15 to	50	
D.C. current gain ratio of matched devices(1)				
$I_C = 7$ A; $V_{CE} = 5$ V	h_{FE1}/h_{FE2}	≤	1,2	
Collector-emitter saturation voltage(1)				
$I_C = 20$ A; $I_B = 4$ A	V_{CEsat}	typ.	1,9	V
Transition frequency at f = 100 MHz(2)				
$-I_E = 7$ A; $V_{CB} = 45$ V	f_T	typ.	235	MHz
$-I_E = 20$ A; $V_{CB} = 45$ V	f_T	typ.	245	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 50$ V	C_c	typ.	280	pF
Feedback capacitance at f = 1 MHz				
$I_C = 150$ mA; $V_{CE} = 50$ V	C_{re}	typ.	170	pF
Collecting-flange capacitance	C_{cf}	typ.	4,4	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300\ \mu s$; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50\ \mu s$; $\delta \leq 0{,}01$.

HF/VHF power transistor

BLW96

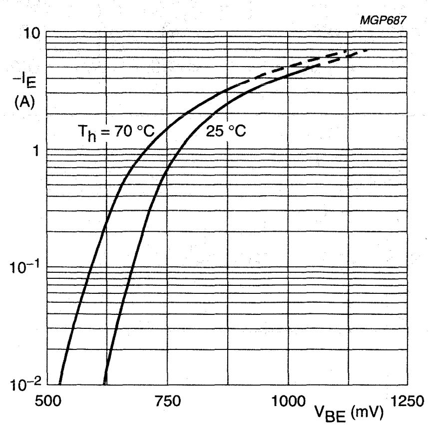


Fig.4 Typical values; V_{CE} = 40 V.

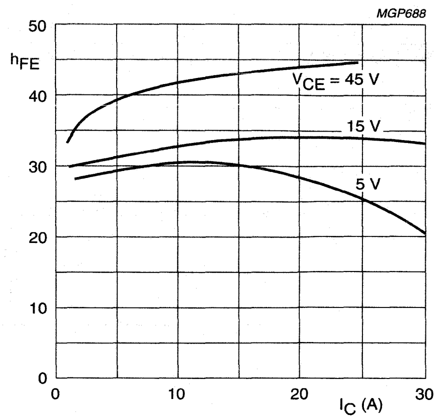


Fig.5 Typical values; T_j = 25 °C.

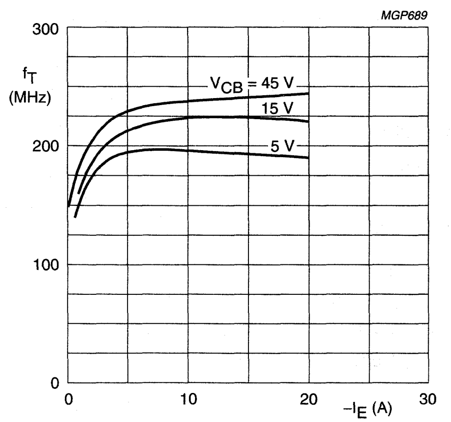


Fig.6 Typical values; f = 100 MHz; T_j = 25 °C.

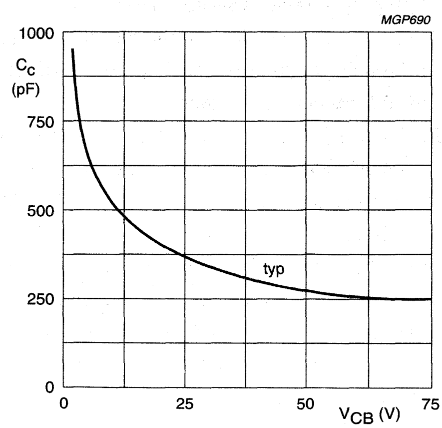


Fig.7 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in s.s.b. class-AB operation (linear power amplifier)
V_{CE} = 50 V; T_h = 25 °C; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_p dB	η_{dt} (%) at 200 W (P.E.P.)	I_C (A) at 200 W (P.E.P.)	d_3 (1) dB	d_5 (1) dB	$I_{C(ZS)}$ A
25 to 200 (P.E.P.)	> 13,5	> 40	< 5,0	< −30	< −30	0,1

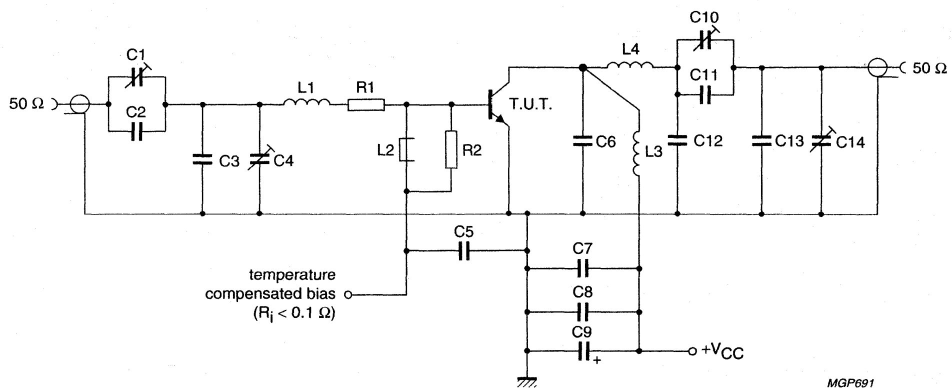


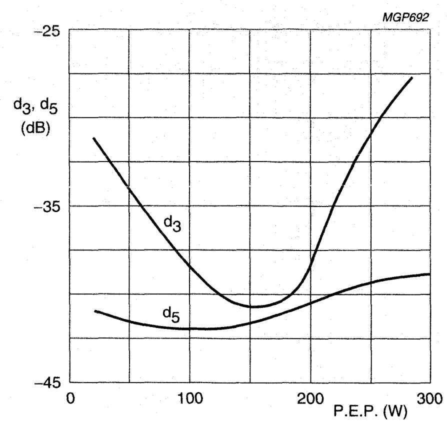
Fig.8 Test circuit; s.s.b. class-AB.

List of components:

- C1 = C4 = C10 = C14 = 100 pF film dielectric trimmer
- C2 = 27 pF ceramic capacitor (500 V)
- C3 = 270 pF polysterene capacitor (630 V)
- C5 = C7 = C8 = 220 nF multilayer ceramic chip capacitor
- C6 = 27 pF multilayer ceramic chip capacitor (500 V; ATC(2))
- C9 = 47 µF/63 V electrolytic capacitor
- C11 = 2 × 36 pF multilayer ceramic chip capacitors (500 V; ATC(2)) in parallel
- C12 = 2 × 43 pF multilayer ceramic chip capacitors (500 V; ATC(2)) in parallel
- C13 = 43 pF multilayer ceramic chip capacitor (500 V; ATC(2))
- L1 = 88 nH; 3 turns Cu wire (1,0 mm); int. dia. 9,0 mm; length 6,1 mm; leads 2 × 5 mm
- L2 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
- L3 = 150 nH; 5 turns Cu wire (2,0 mm); int. dia. 10,0 mm; length 18,7 mm; leads 2 × 5 mm
- L4 = 197 nH; 5 turns Cu wire (2,0 mm); int. dia. 12,0 mm; length 18,6 mm; leads 2 × 5 mm
- R1 = 0,66 Ω; parallel connection of 5 × 3,3 Ω metal film resistors (PR37; ± 5%; 1,6 W each)
- R2 = 27 Ω carbon resistor (± 5%; 0,5 W)

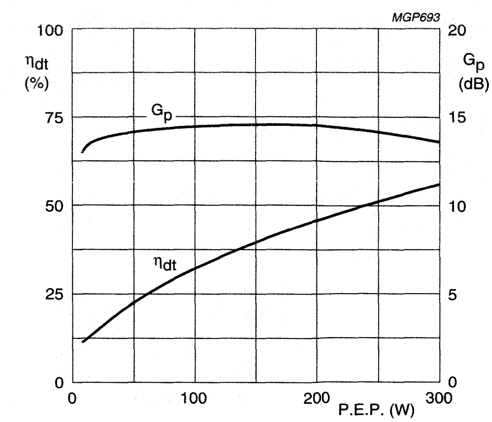
Notes

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.
2. ATC means American Technical Ceramics.



V_{CE} = 50 V; $I_{C(ZS)}$ = 0,1 A; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

Fig.9 Intermodulation distortion as a function of output power.(1)



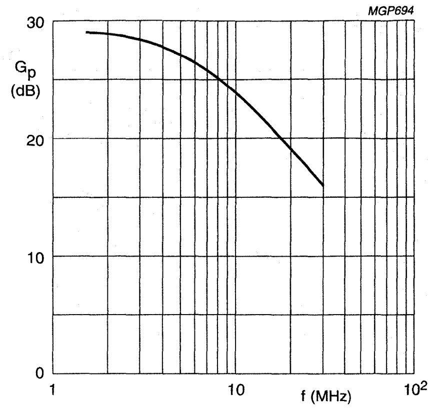
V_{CE} = 50 V; $I_{C(ZS)}$ = 0,1 A; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C; typical values.

Fig.10 Double-tone efficiency and power gain as a function of output power.

Ruggedness

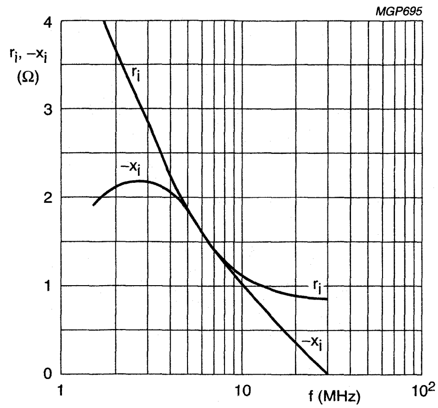
The BLW96 is capable of withstanding full load mismatch (VSWR = 50 through all phases) up to 150 W (P.E.P.) or a load mismatch (VSWR = 5 through all phases) up to 200 W (P.E.P.) under the following conditions:

V_{CE} = 45 V; f = 28 MHz; T_h = 70 °C; $R_{th\ mb\text{-}h}$ = 0,2 K/W.



V_{CE} = 50 V; $I_{C(ZS)}$ = 0,1 A; P_L = 200 W (P.E.P.);
T_h = 25 °C; Z_L = 5 Ω; neutralizing capacitor: 47 pF

Fig.11 Power gain as a function of frequency.



V_{CE} = 50 V; $I_{C(ZS)}$ = 0,1 A; P_L = 200 W (P.E.P.);
T_h = 25 °C; Z_L = 5 Ω; neutralizing capacitor: 47 pF

Fig.12 Input impedance (series components) as a function of frequency.

Figs 11 and 12 are typical curves and hold for one transistor of a push-pull amplifier with cross-neutralization in s.s.b. class-AB operation.

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit)
T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_p (dB)	I_C (A)	η (%)
108	50	200	typ. 45	typ. 6,5	typ. 6	typ. 67

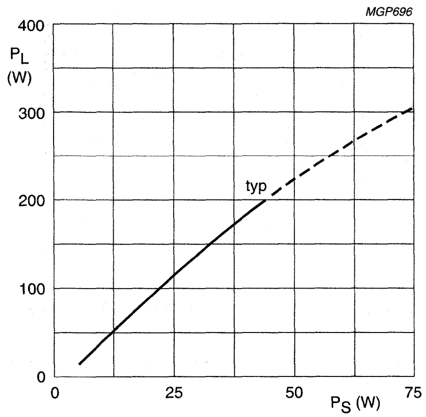


Fig.13 V_{CE} = 50 V; f = 108 MHz; T_h = 25 °C.

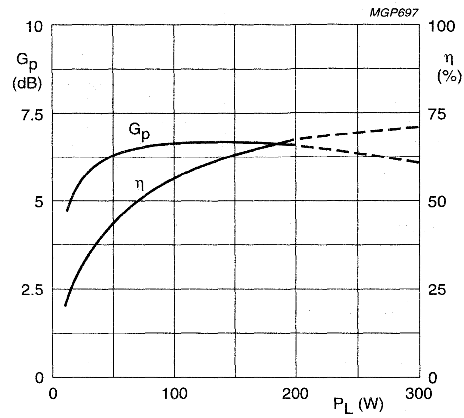
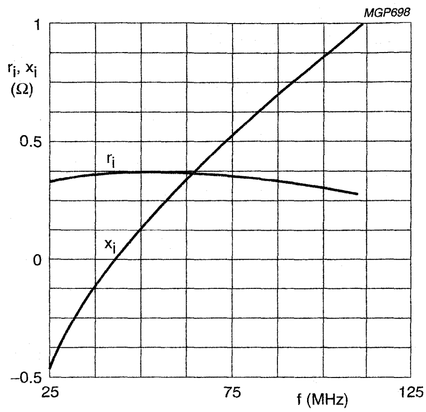
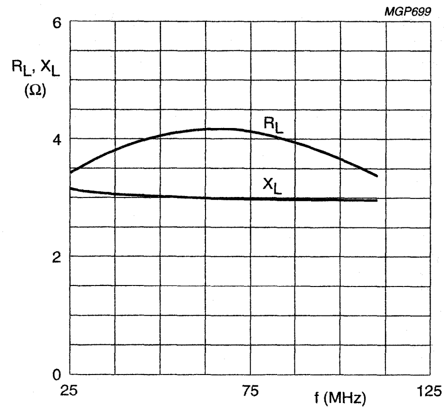


Fig.14 V_{CE} = 50 V; f = 108 MHz; T_h = 25 °C; typical values.



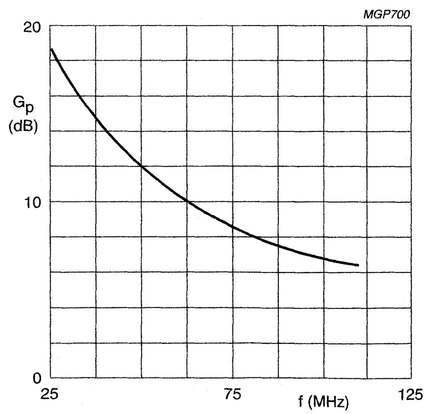
Typical values; V_{CE} = 50 V; P_L = 200 W; T_h = 25 °C; class-B operation

Fig.15 Input impedance (series components).



Typical values; V_{CE} = 50 V; P_L = 200 W; T_h = 25 °C; class-B operation

Fig.16 Load impedance (series components).



Typical values; V_{CE} = 50 V; P_L = 200 W; T_h = 25 °C; class-B operation

Fig.17

R.F. performance in s.s.b. class-A operation (linear power amplifier)
V_{CE} = 40 V; T_h = 25 °C; f_1 = 28,000 MHz; f_2 = 28,001 MHz

OUTPUT POWER W	G_p dB	I_C A	d_3(1) dB	d_5(1) dB
typ. 50 (P.E.P.)	typ. 19	4	typ. −40	< −40

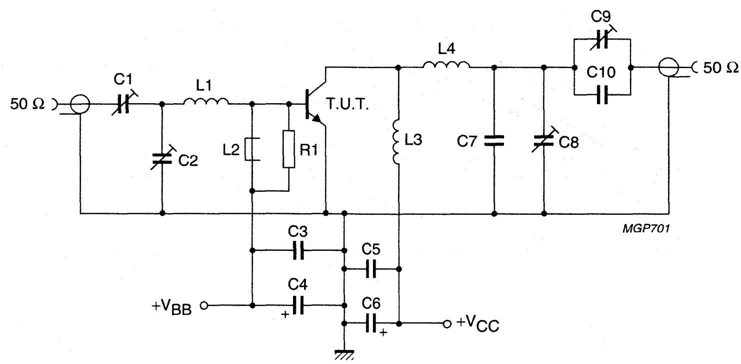


Fig.18 Test circuit; s.s.b. class-A.

List of components:

C1 = C2 = 10 to 780 pF film dielectric trimmer
C3 = 220 nF polyester capacitor (100 V)
C4 = 100 μF/4 V electrolytic capacitor
C5 = 2 × 330 nF polyester capacitors (100 V) in parallel
C6 = 47 μF/63 V electrolytic capacitor
C7 = C10 = 2 × 82 pF ceramic capacitors (500 V) in parallel
C8 = C9 = 10 to 150 pF air dielectric trimmer
L1 = 45 nH; 2 turns enamelled Cu wire (1,6 mm); int. dia. 8,0 mm; length 4,0 mm; leads 2 × 3 mm
L2 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3 = 110 nH; 4 turns enamelled Cu wire (2,0 mm); int. dia. 10,0 mm; length 8,0 mm; leads 2 × 2 mm
L4 = 210 nH; 5 turns enamelled Cu wire (2,0 mm); int. dia. 12,0 mm; length 10,0 mm; leads 2 × 2 mm
R1 = 27 Ω carbon resistor (± 5%; 0,5 W)

Note

1. Stated intermodulation distortion figures are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

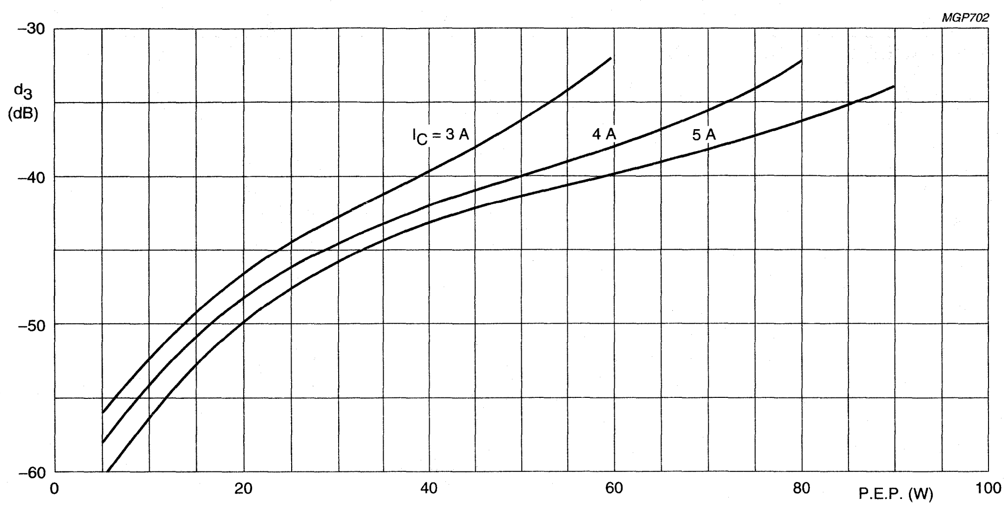


Fig.19 Third order intermodulation distortion as a function of output power.(1) Typical values; V_{CE} = 40 V; T_h = 25 °C; f_1 = 28,000 MHz; f_2 = 28,001 MHz.

HF power transistor BLW97

DESCRIPTION

N-P-N silicon planar epitaxial transistor designed for use in class-A, AB and B operated high-power industrial and military transmitting equipment in the h.f. band.

The transistor offers excellent performance as a linear amplifier in s.s.b. applications. It is resistance stabilized and is made to withstand severe load-mismatch conditions. All leads are isolated from the flange.

The transistors are supplied in matched h_{FE} groups.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C

MODE OF OPERATION	V_{CE} V	$I_{C(ZS)}$ A	f MHz	P_L W	G_p dB	η_{dt} %	d_3 dB	d_5 dB
s.s.b. (class-AB)	28	0,1	1,6 – 28	175 (PEP)	> 11,5	> 40	< –30	< –30

PIN CONFIGURATION

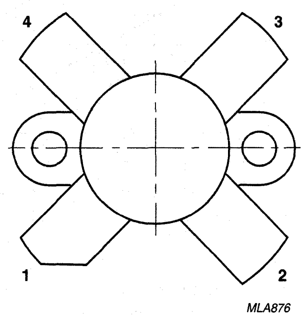


Fig.1 Simplified outline. SOT121B.

PINNING - SOT121B.

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (peak value)				
$V_{BE} = 0$	V_{CESM}	max.	65	V
open base	V_{CEO}	max.	33	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current				
average	$I_{C(AV)}$	max.	15	A
peak value; f > 1 MHz	I_{CM}	max.	50	A
Total d.c. power dissipation at $T_h = 25°C$	$P_{tot(d.c.)}$	max.	190	W
R.F. power dissipation				
f > 1 MHz; $T_h = 25°C$	$P_{tot(rf)}$	max.	230	W
Storage temperature	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	200	°C

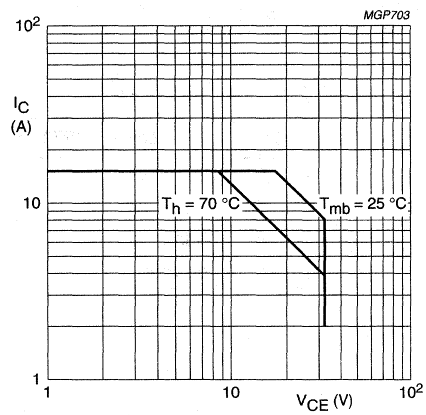
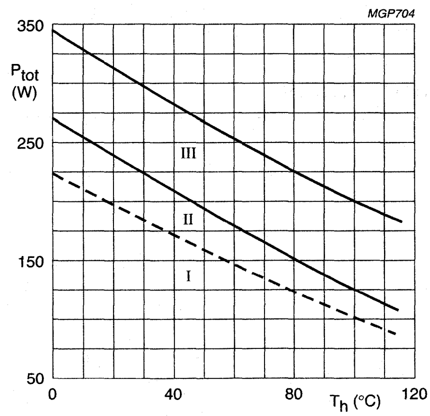


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation (f > 1 Mhz).
III Short-time operation during mismatch; (f > 1 MHz).

Fig.3 Power/temperature derating curves.

THERMAL RESISTANCE

(dissipation = 120 W; $T_h = 25$ °C i.e. $T_{mb} = 49$ °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	0,63	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	0,48	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 50 mA	$V_{(BR)CES}$	>	65	V
I_C = 100 mA; open base	$V_{(BR)CEO}$	>	33	V
Emitter-base breakdown voltage				
I_E = 20 mA; open collector	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
V_{CE} = 33 V; V_{BE} = 0	I_{CES}	<	20	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	20	mJ
R_{BE} = 10 Ω	E_{SBR}	>	20	mJ
D.C. current gain(1)		typ.	30	
I_C = 10 A; V_{CE} = 5 V	h_{FE}	15 to	50	
D.C. current gain ratio of matched devices(1)				
I_C = 10 A; V_{CE} = 5 V	h_{FE1}/h_{FE2}	<	1,2	
Collector-emitter saturation voltage(1)				
I_C = 25 A; I_B = 5 A	V_{CEsat}	typ.	2,4	V
Transition frequency at f = 100 MHz(2)				
$-I_E$ = 10 A; V_{CB} = 28 V	f_T	typ.	230	MHz
$-I_E$ = 20 A; V_{CB} = 28 V	f_T	typ.	235	MHz
Collector capacitance at f = 1 MHz				
$I_E = i_e$ = 0; V_{CB} = 28 V	C_c	typ.	380	pF
Feedback capacitance at f = 1 MHz				
I_C = 0; V_{CE} = 28 V	C_{re}	typ.	235	pF
Collector-flange capacitance	C_{cf}	typ.	4,5	pF

Notes

1. Measured under pulse conditions: t_p = 500 μs.
2. Measured under pulse conditions: t_p = 300 μs; δ = 0,02.

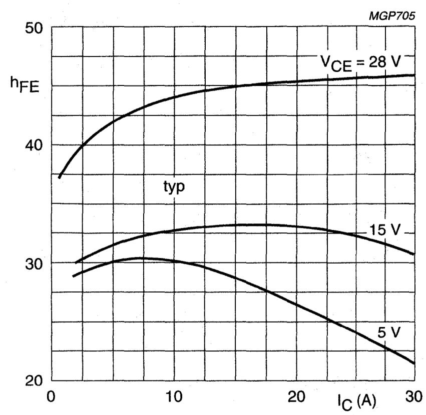


Fig.4 T_j = 25 °C.

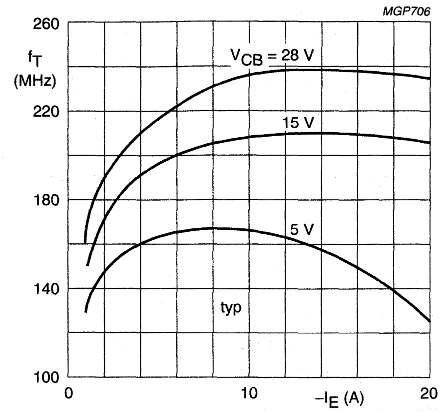


Fig.5 T_j = 25 °C; f = 100 MHz; t_p = 300 µs.

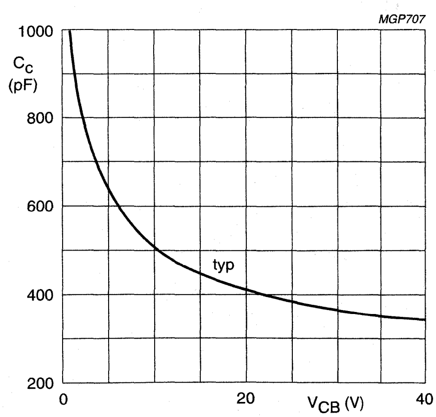


Fig.6 $I_E = i_e = 0$; f = 1 MHz; T_j = 25 °C.

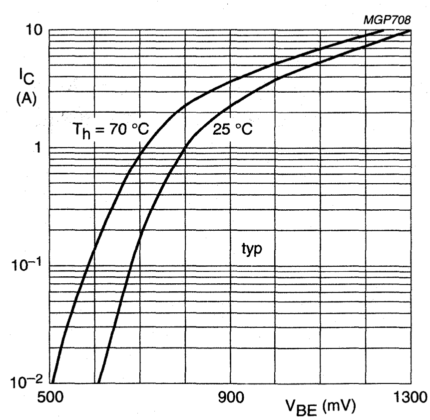


Fig.7 V_{CE} = 28 V.

APPLICATION INFORMATION

R.F. performance in s.s.b. class-AB operation (linear power amplifier).
V_{CE} = 28 V; T_h = 25 °C; f_1 = 28,000 MHz; f_2 = 28,001 MHz.

OUTPUT POWER W	G_p dB	η_{dt} %	I_C A	d_3 (1) dB	d_5 (1) dB	$I_{C(ZS)}$ A
175 (PEP)	> 11,5 typ. 13,0	> 40 typ. 50	< 7,8 typ. 6,3	< −30 typ. −34	< −30 typ. −38	0,1

Note

1. The stated intermodulation distortion levels are referred to the according level of either of the equal amplified tones. Relative to the according peak envelope powers these figures should be increased by 6 dB.

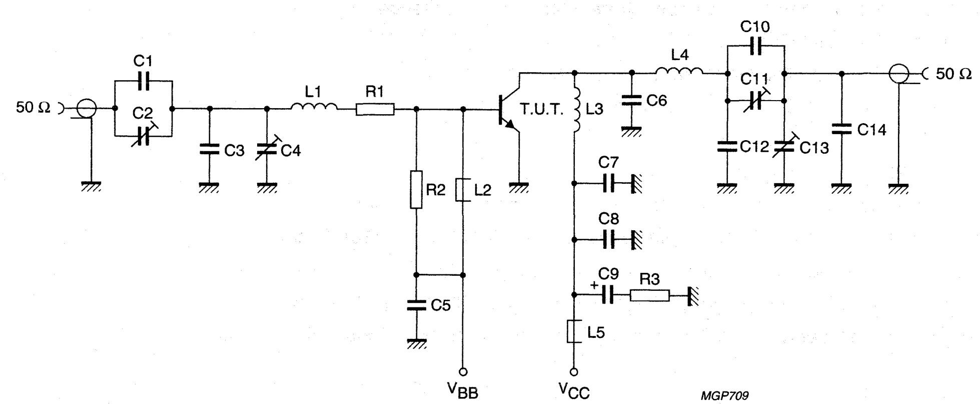


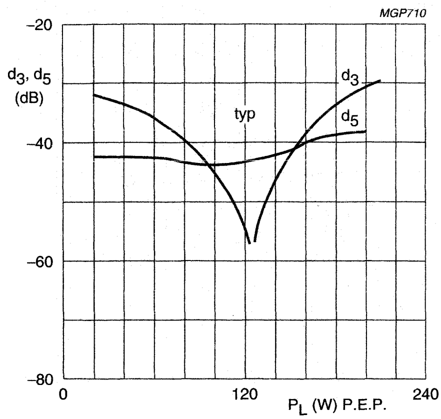
Fig.8 Class-AB (s.s.b.) test circuit.

List of components:

C1	=	47 pF (500 V) multilayer ceramic chip capacitor(1)
C2	=	100 pF film dielectric trimmer
C3	=	2 × 130 pF (300 V) multilayer ceramic chip capacitors in parallel(1)
C4	=	280 pF film dielectric trimmer
C5	=	10 nF (50 V) multilayer ceramic chip capacitor 2222 856 13103
C6	=	2 × 180 pF (300 V) multilayer ceramic chip capacitors in parallel(1)
C7	=	100 nF (50 V) multilayer ceramic chip capacitor 2222 856 48104
C8	=	10 nF (50 V) multilayer ceramic chip capacitor 2222 856 13103
C9	=	2,2 µF - 63 V solid aluminium electrolytic capacitor
C10	=	5 × 82 pF (500 V) multilayer ceramic chip capacitors in parallel(1)
C11	=	250 pF air dielectric trimmer
C12	=	5 × 33 pF ceramic feed-through capacitors mounted in parallel on a brass plate
C13	=	100 pF air dielectric trimmer
C14	=	3 × 91 pF (500 V) multilayer ceramic chip capacitors in parallel(1)
R1	=	0,7 Ω - 7 W (7 × 4,7 Ω - 1 W carbon resistors in parallel)
R2	=	27 Ω - 0,25 W carbon resistor
R3	=	4,7 Ω - 0,25 W carbon resistor
L1	=	73 nH; 4 turns Cu wire (1,5 mm); int. dia. 7 mm; length 9,4 mm; leads 2 × 5 mm
L2	=	Ferroxcube wide-band h.f. choke grade 3B (cat. no. 4312 020 36640); 6 leads in parallel
L3	=	70,4 nH; 4 turns Cu wire (2 mm); int. dia. 7 mm; length 14,8 mm; leads 2 × 5 mm
L4	=	83,5 nH; 4 turns Cu wire (2 mm); int. dia. 8 mm; length 15 mm; leads 2 × 5 mm
L5	=	Ferroxcube wide-band h.f. choke grade 3 B (cat. no. 4312 020 36640) with 6 leads in parallel

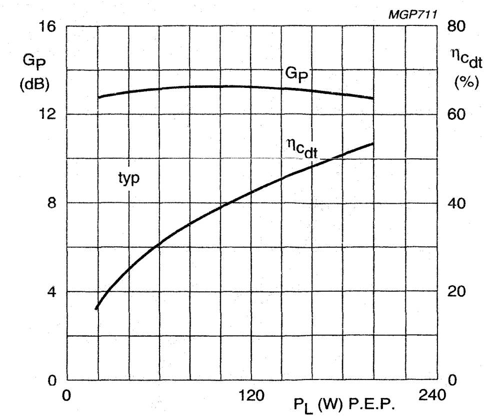
Note

1. American Technical Ceramics capacitor or capacitor of same quality.



V_{CE} = 28 V; $I_{C(ZS)}$ = 0,1 A; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C.

Fig.9 Intermodulation distortion (see note on preceding page).



V_{CE} = 28 V; $I_{C(ZS)}$ = 0,1 A; f_1 = 28,000 MHz;
f_2 = 28,001 MHz; T_h = 25 °C.

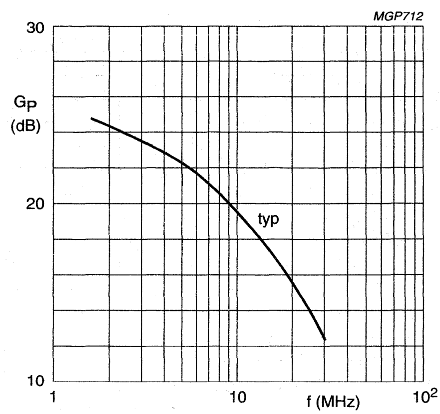
Fig.10 Power gain and double-tone efficiency.

RUGGEDNESS

The BLW97 is capable of withstanding full load mismatch (VSWR = 50 through all phases) up to 150 W (P.E.P.) or a load mismatch (VSWR = 5 through all phases) up to 175 W (P.E.P.) under the following conditions:

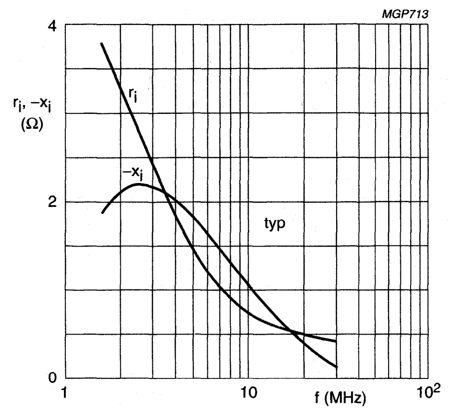
V_{CE} = 28 V; f = 28 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0,2 K/W.

Figures 11 and 12 t typical curves which are valid for one transistor of a push-pull amplifier in s.s.b. class-AB operation.



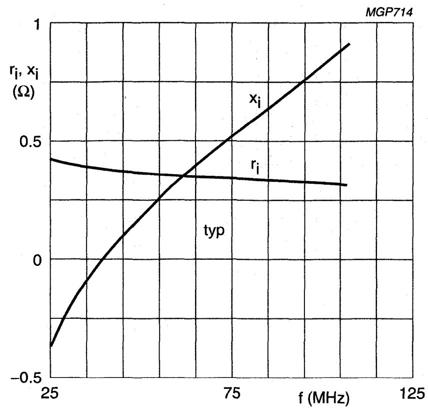
V_{CE} = 28 V; $I_{C(ZS)}$ = 0,1 A;
P_L = 175 W(PEP); T_h = 25 °C;
Z_L = 1,55 Ω

Fig.11 Power gain.



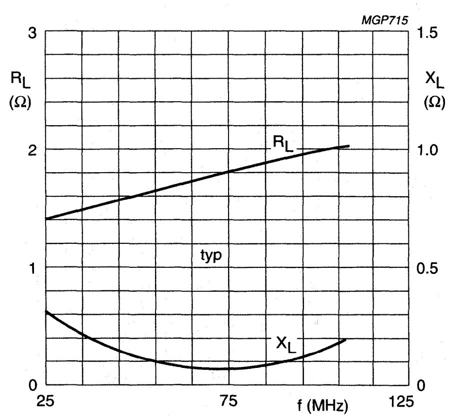
V_{CE} = 28 V; $I_{C(ZS)}$ = 0,1 A;
P_L = 175 W(PEP); T_h = 25 °C;
Z_L = 1,55 Ω

Fig.12 Input impedance (series components).



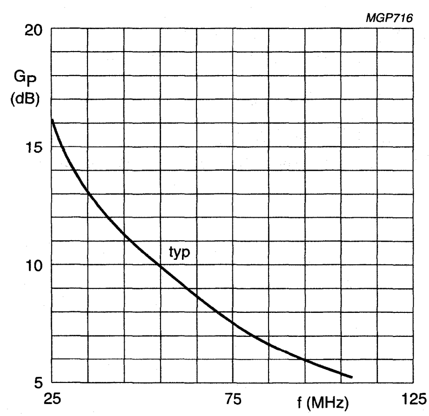
V_{CE} = 28 V; P_L = 175 W; T_h = 25 °C;
class-B operation.

Fig.13 Input impedance (series components).



V_{CE} = 28 V; P_L = 175 W; T_h = 25 °C;
class-B operation.

Fig.14 Load impedance (series components).



V_{CE} = 28 V; P_L = 175 W; T_h = 25 °C;
class-B operation.

Fig.15 Power gain.

UHF linear power transistor BLW98

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in linear u.h.f. amplifiers of TV transposers and transmitters in band IV-V, as well as for driver stages in tube systems.

FEATURES:

- diffused emitter ballasting resistors for an optimum temperature profile;
- gold sandwich metallization ensures excellent reliability.

The transistor has a ¼" capstan envelope with ceramic cap. All leads are isolated from the stud.

QUICK REFERENCE DATA

R.F. performance in linear amplifier

MODE OF OPERATION	f_{vision} MHz	V_{CE} V	I_C mA	T_h °C	d_{im} (1) dB	$P_{o\ sync}$ (1) W	G_p dB
class-A	860	25	850	70	−60	> 3,5	> 6,5
class-A	860	25	850	25	−60	typ. 4,4	typ. 7,0

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

PIN CONFIGURATION

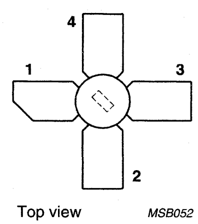


Fig.1 Simplified outline. SOT122A.

PINNING - SOT122A.

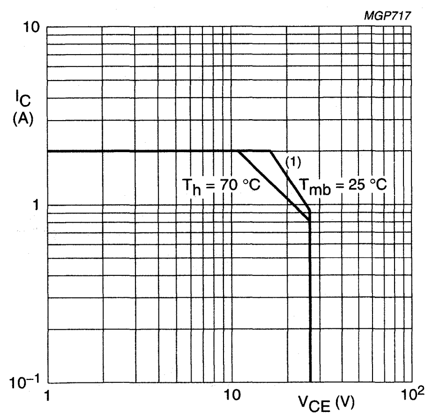
PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage				
(peak value); $V_{BE} = 0$	V_{CESM}	max.	50	V
open base	V_{CEO}	max.	27	V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5	V
Collector current				
d.c.	I_C	max.	2	A
(peak value); f > 1 MHz	I_{CM}	max.	4	A
Total power dissipation at $T_h = 70\ °C$	P_{tot}	max.	21,5	W
Storage temperature	T_{stg}		−65 to +150	°C
Operating junction temperature	T_j	max.	200	°C



(1) Second breakdown limit (independent of temperature).

Fig.2 D.C. SOAR.

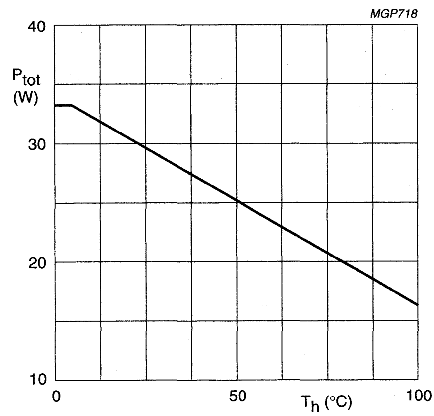


Fig.3 Power derating curve vs. temperature.

THERMAL RESISTANCE

(dissipation = 21,25 W; T_{mb} = 82,75 °C, T_h = 70 °C)

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	5,45	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,6	K/W

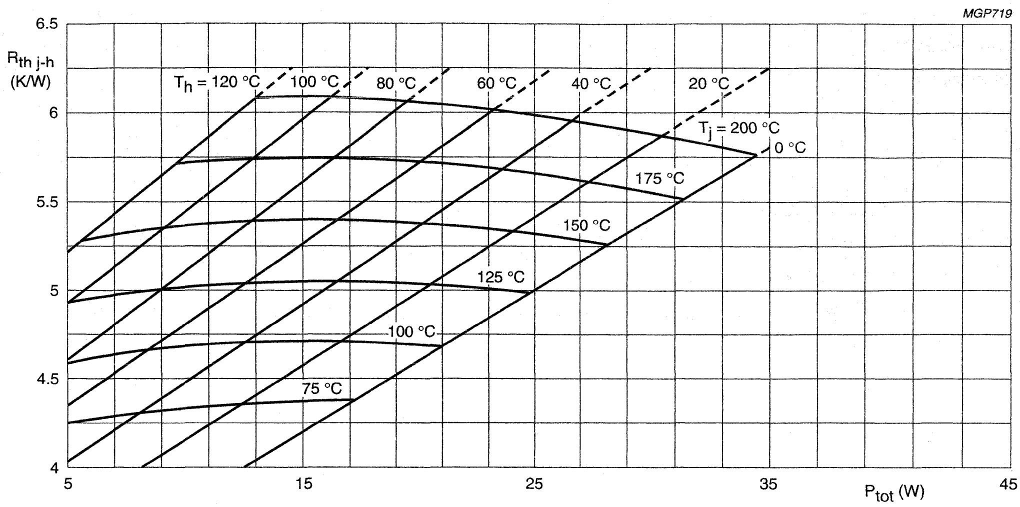


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb\text{-}h}$ = 0,6 K/W.)

Example

Nominal class-A operation (without r.f. signal): V_{CE} = 25 V; I_C = 850 mA; T_h = 70 °C.

Fig.4 shows:	$R_{th\ j\text{-}h}$	max.	6,05	K/W
	T_j	max.	200	°C
Typical device:	$R_{th\ j\text{-}h}$	typ.	5,35	K/W
	T_j	typ.	183	°C

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage				
V_{BE} = 0; I_C = 10 mA	$V_{(BR)CES}$	>	50	V
open base, I_C = 25 mA	$V_{(BR)CEO}$	>	27	V
Emitter-base breakdown voltage				
open collector, I_E = 5 mA	$V_{(BR)EBO}$	>	3,5	V
D.C. current gain[1]				
I_C = 850 mA; V_{CE} = 25 V	h_{FE}	>	15	
		typ.	40	
Collector-emitter saturation voltage[1]				
I_C = 500 mA; I_B = 100 mA	V_{CEsat}	typ.	0,25	V
Transition frequency at f = 500 MHz[2]				
$-I_E$ = 850 mA; V_{CB} = 25 V	f_T	typ.	2,5	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ.	24	pF
		<	30	pF
Feedback capacitance at f = 1 MHz				
I_C = 50 mA; V_{CE} = 25 V	C_{re}	typ.	15	pF
Collector-stud capacitance	C_{cs}	typ.	1,2	pF

Notes

1. Measured under pulse conditions: $t_p \leq 300\ \mu s$; $\delta \leq 0{,}02$.
2. Measured under pulse conditions: $t_p \leq 50\ \mu s$; $\delta \leq 0{,}01$.

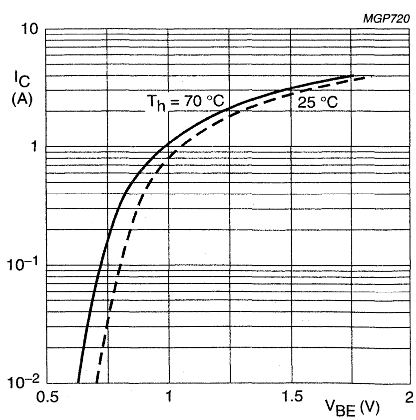


Fig.5 Typical values; V_{CE} = 25 V.

UHF linear power transistor

BLW98

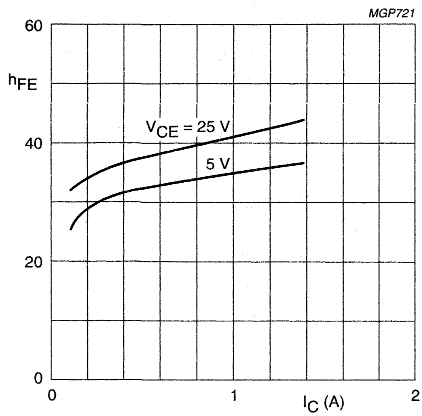


Fig.6 Typical values; T_j = 25 °C.

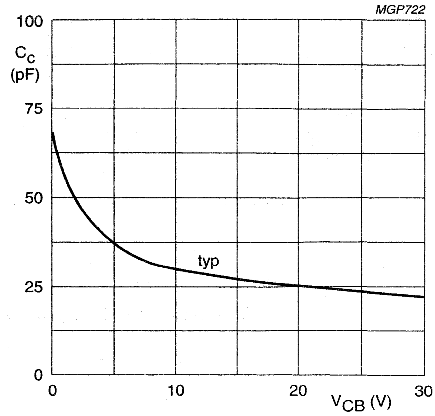


Fig.7 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

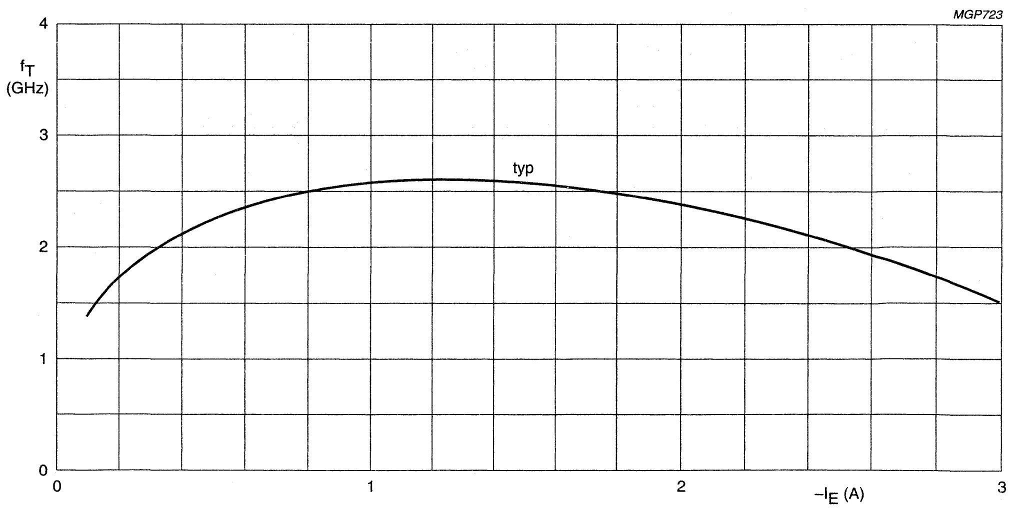


Fig.8 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C.

APPLICATION INFORMATION

R.F. performance in u.h.f. class-A operation (linear power amplifier)

f_{vision} (MHz)	V_{CE} (V)	I_C (mA)	T_h (°C)	d_{im}(dB)(1)	$P_{o\ sync}$ (W)(1)	G_P (dB)
860	25	850	70	−60	> 3,5	> 6,5
860	25	850	70	−60	typ. 3,8	typ. 7,0
860	25	850	25	−60	typ. 4,4	typ. 7,0

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

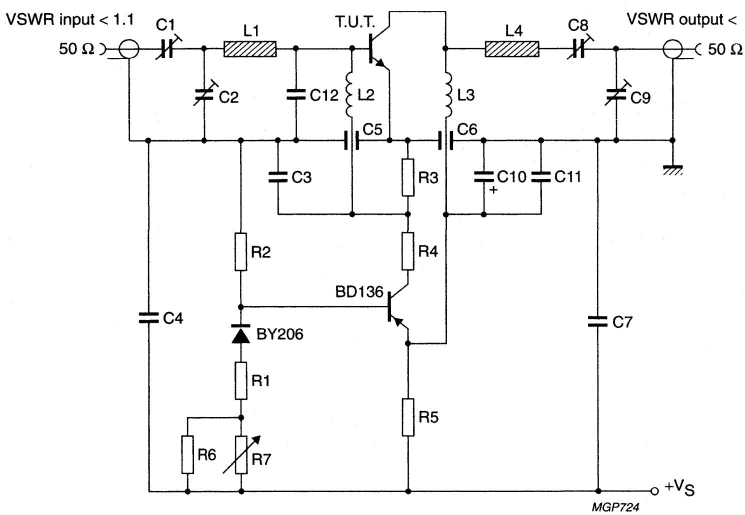
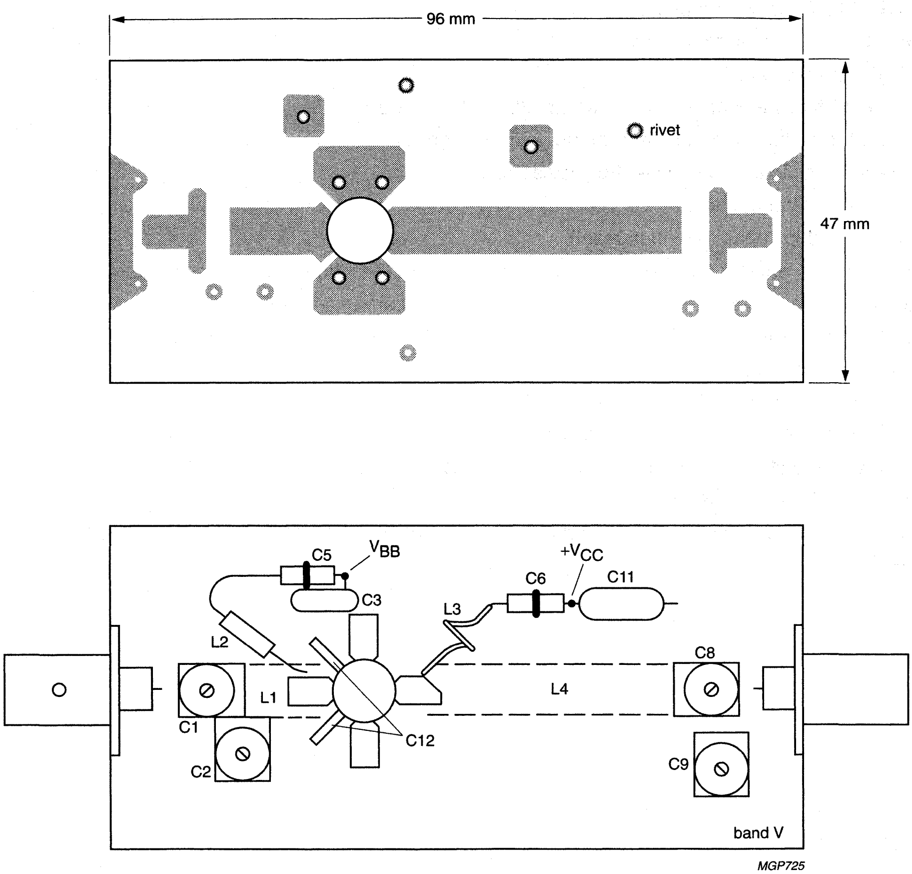


Fig.9 Class-A test circuit at f_{vision} = 860 MHz.

List of components:

C1 = C2 = 1,4 to 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C3 = C4 = 100 nF polyester capacitor
C5 = C6 = 1 nF feed-through capacitor
C7 = 5,6 pF ceramic capacitor
C8 = 2 to 18 pF film dielectric trimmer (cat. no. 2222 809 09003)
C9 = 2 to 9 pF film dielectric trimmer (cat. no. 2222 809 09002)
C10 = 10 μF/40 V solid aluminium electrolytic capacitor
C11 = 470 nF polyester capacitor
C12 = 2 × 3,3 pF chip capacitors (in parallel)
R1 = 150 Ω carbon resistor (0,25 W)
R2 = 1,8 kΩ carbon resistor (0,5 W)
R3 = 33 Ω carbon resistor (0,5 W)
R4 = 220 Ω carbon resistor (1 W)
R5 = 4 × 12 Ω carbon resistors in parallel (1 W each)
R6 = 1 kΩ carbon resistor (0,25 W)
R7 = 220 Ω carbon potentiometer (0,25 W)
L1 = stripline (13,6 mm × 6,9 mm)
L2 = microchoke 0,47 μH (cat. no. 4322 057 04770)
L3 = 1 turn Cu wire (1 mm); internal diameter 5,5 mm; leads 2 × 5 mm
L4 = stripline (40,8 mm × 6,9 mm)

L1 and L4 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ε_r = 2,74); thickness 1,5 mm.



Note

Hole in printed-circuit board: Ø 9,7 mm.

Fig.10 Component layout and printed circuit board for 860 MHz class-A test circuit.

The circuit and the components are on one side of the PTFE fibre-glass board, the other side is unetched copper to serve as a ground-plane. Earth connections are made by hollow rivets. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

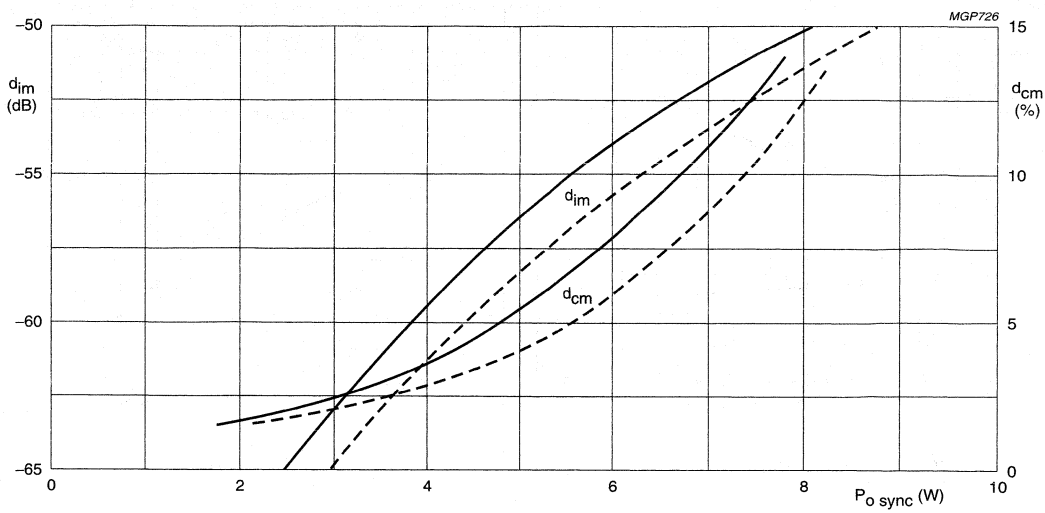
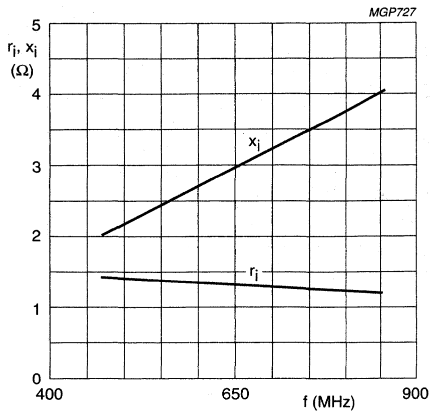


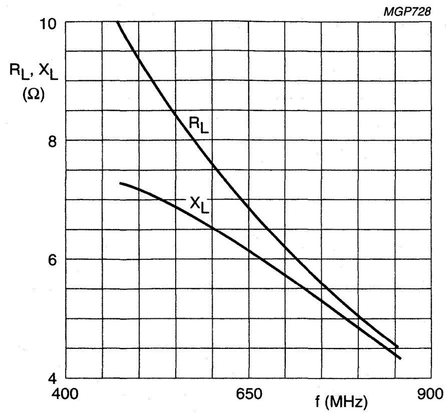
Fig.11 Intermodulation distortion (d_{im})(1.) and cross-modulation distortion (d_{cm})(2.) as a function of $P_{o\ sync}$. Typical values; V_{CE} = 25 V; I_C = 850 mA;- - -T_h = 25 °C;——T_h = 70 °C; f_{vision} = 860 MHz.

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
   Intermodulation distortion of input signal ≤ −75 dB.
2. Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level.
   Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB.



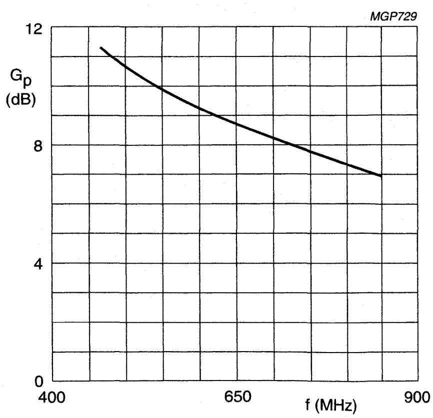
Typical values; V_{CE} = 25 V; I_C = 850 mA;
class-A operation; T_h = 70 °C.

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 25 V; I_C = 850 mA;
class-A operation; T_h = 70 °C.

Fig.13 Load impedance (series components).



Typical values; V_{CE} = 25 V; I_C = 850 mA;
class-A operation; T_h = 70 °C.

Fig.14

UHF linear power transistor | BLW898

FEATURES

- Internal input matching for wideband operation and high power gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATION

- Common emitter class-A operation in linear transposers/transmitters (television) in the 470 to 860 MHz frequency band.

DESCRIPTION

NPN silicon planar transistor in a SOT171A 6-lead rectangular flange package, with a ceramic cap. The transistor delivers a $P_{o\ sync}$ = 3 W in class-A operation at 860 MHz and a supply voltage of 25 V.

PINNING SOT171A

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

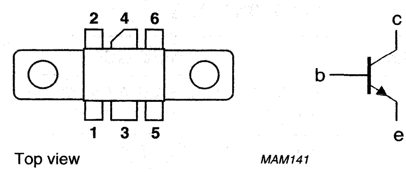


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)
CW class-A	860	25	1.1	≥3(1)	≥9(1)

Note

1. Three-tone test signal (−8, −16, and −10 dB); d_{im} = −63 dB.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

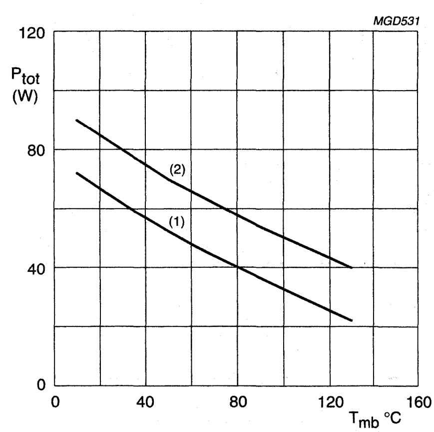
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	collector current (DC)		–	3.7	A
$I_{C(AV)}$	average collector current		–	3.7	A
P_{tot}	total power dissipation	up to T_{mb} = 70 °C	–	44	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	P_{tot} = 44 W; T_{mb} = 70 °C	3	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink		0.3	K/W



(1) Continuous operation

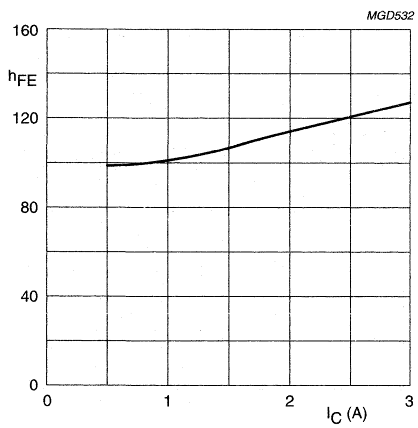
(2) Short-time operation during mismatch.

Fig.2 Power derating curve.

CHARACTERISTICS

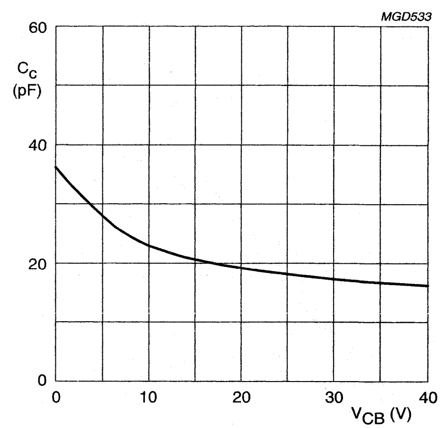
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 15 mA; I_E = 0	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 30 mA; I_B = 0	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 0.6 mA; I_C = 0	2.5	–	–	V
I_{CBO}	collector-base leakage current	V_{BE} = 0; V_{CB} = 28 V	–	–	1.5	mA
I_{CEO}	collector-emitter leakage current	V_{CE} = 20 V	–	–	3	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 1.1 A	30	–	140	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	18	–	pF
C_{re}	feedback capacitance	V_{CB} = 25 V; I_C = 0; f = 1 MHz	–	11	–	pF



V_{CE} = 25 V; t_p = 500 µs; δ = <1 %.

Fig.3 DC current gain as a function of collector current; typical values.



I_E = i_e = 0; f = 1 MHz.

Fig.4 Collector capacitance as a function of collector-base voltage; typical values.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter class-A test circuit.

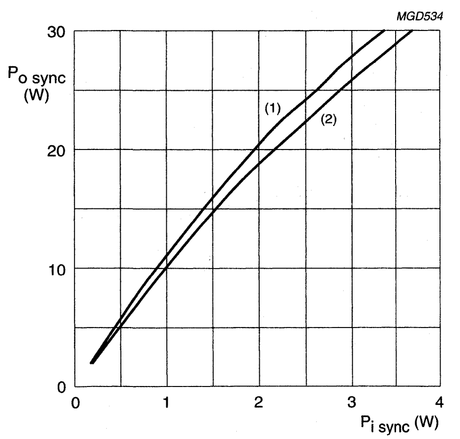
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB)
CW class-A	860	25	1.1	≥3[1]	≥9[1]	<–63[1]
CW class-A	860	25	1.1	≥3[2]	≥9[2]	<–60[2]

Notes

1. Three-tone test method (vision carrier –8 dB, sound carrier –10 dB, sideband signal –16 dB), 0 dB corresponds to peak sync level.
2. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), 0 dB corresponds to peak sync level.

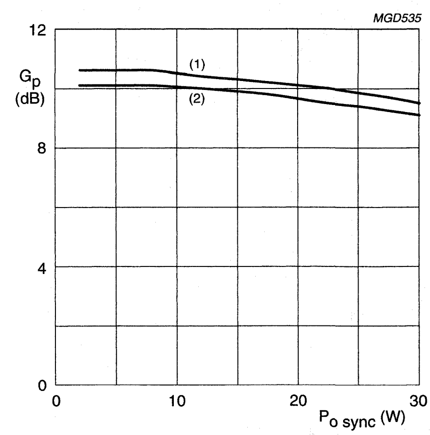
Ruggedness in class-A operation

The BLW898 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases, under the conditions: V_{CE} = 25 V; I_{CQ} = 1.1 A; T_h = 25 °C; f = 860 MHz; $P_{o\ sync}$ = 3 W.



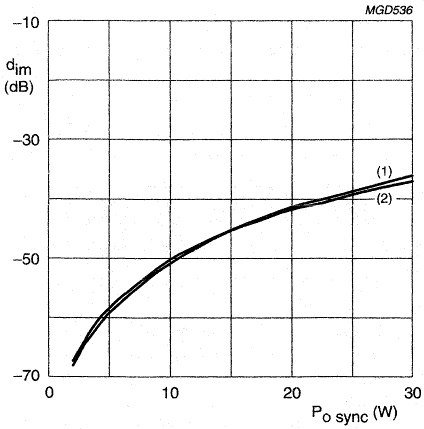
V_{CE} = 25 V; I_{CQ} = 1.1 A; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.5 Output power as a function of input power; typical values.



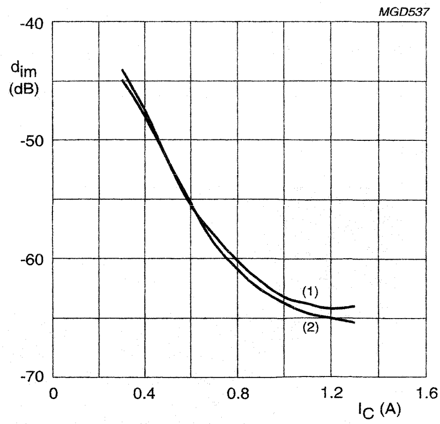
V_{CE} = 25 V; I_{CQ} = 1.1 A; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.6 Power gain as a function of output power; typical values.



$V_{CE} = 25$ V; $I_{CQ} = 1.1$ A; f = 860 MHz; (3-tone; −8/−16/−10 dB).
(1) $T_h = 25$ °C.
(2) $T_h = 70$ °C.

Fig.7 Intermodulation distortion as a function of output power; typical values.



$V_{CE} = 25$ V; $I_{CQ} = 1.1$ A; f = 860 MHz; $P_{o\ sync} = 3$ W;
(3-tone; −8/−16/−10 dB).
(1) $T_h = 70$ °C.
(2) $T_h = 25$ °C.

Fig.8 Intermodulation distortion as a function of collector current; typical values.

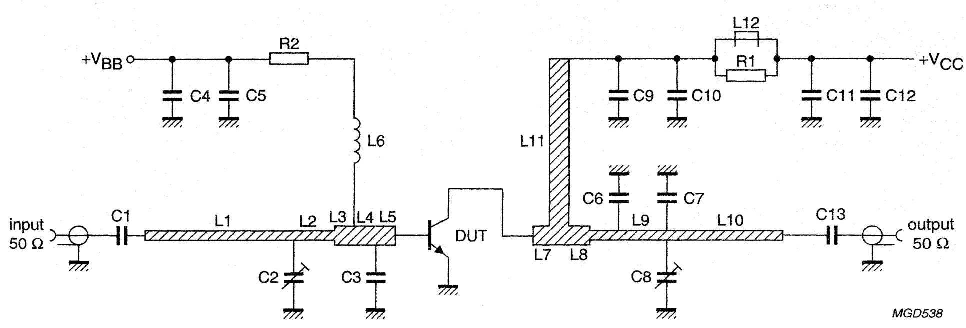
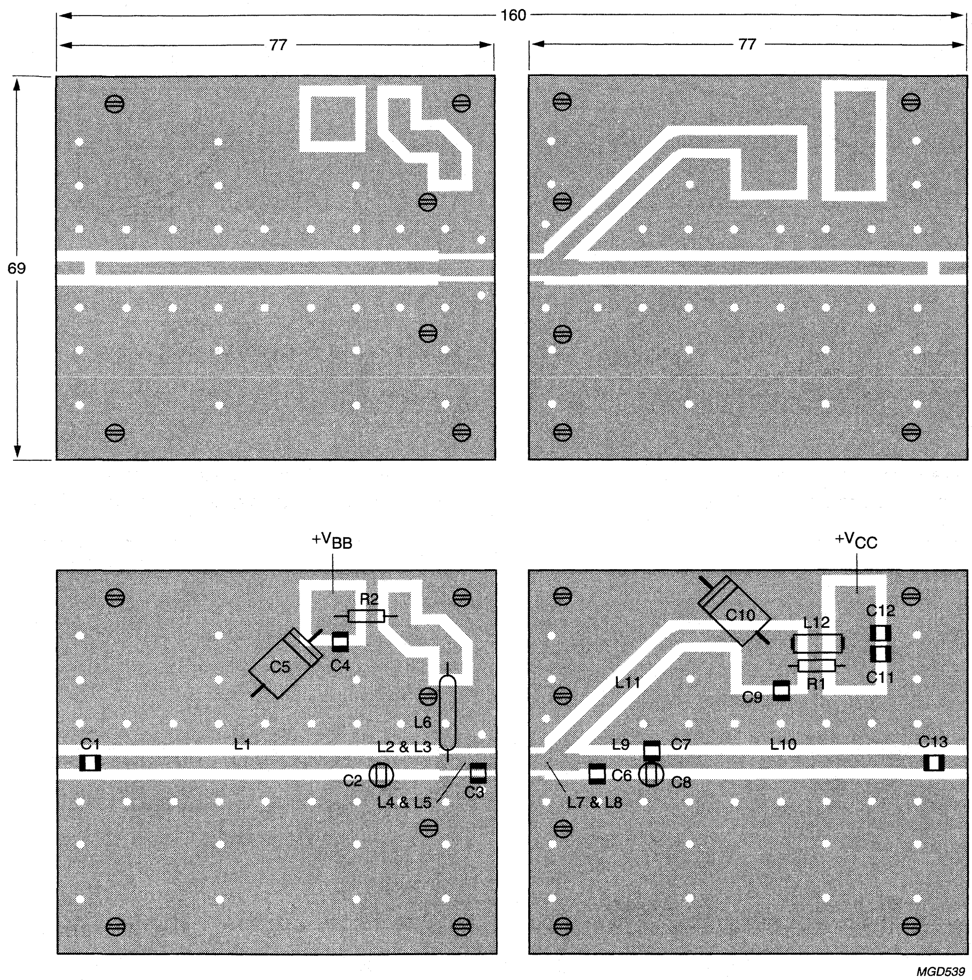


Fig.9 Class-A test circuit at 860 MHz.



Dimensions in mm.

Fig.10 Printed-circuit board and component lay-out for 860 MHz class-A test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1	multilayer ceramic chip capacitor; note 1	8.2 pF		
C2, C8	Tekelec Giga trim 37271	0.6 to 4.5 pF		
C3	multilayer ceramic chip capacitor; note 1	15 pF		
C4, C12	multilayer ceramic chip capacitor	10 nF; 63 V		2222 592 16627
C5	solid aluminium capacitor	10 μF; 63 V		2222 030 38109
C6	multilayer ceramic chip capacitor; note 2	10 pF		
C7	multilayer ceramic chip capacitor; note 2	2.4 pF		
C9	multilayer ceramic chip capacitor; note 2	500 pF		
C10	solid aluminium capacitor	47 μF; 63 V		2222 031 38479
C11	multilayer ceramic chip capacitor; note 2	330 pF		
C13	multilayer ceramic chip capacitor; note 1	5.1 pF		
L1	stripline; note 3	50 Ω	50 × 2.3 mm	
L2	stripline; note 3	50 Ω	10 × 2.3 mm	
L3	stripline; note 3	40 Ω	2 × 3.25 mm	
L4, L5	stripline; note 3	40 Ω	4 × 3.25 mm	
L6	RF choke	220 nH		
L7	stripline; note 3	40 Ω	9 × 3.25 mm	
L8	stripline; note 3	40 Ω	3.5 × 3.25 mm	
L9	stripline; note 3	50 Ω	9 × 2.3 mm	
L10	stripline; note 3	50 Ω	48.5 × 2.3 mm	
L11	stripline; note 3	40 Ω	41.5 × 3.25 mm	
L12	grade 4S2 ferroxcube wideband RF choke			4330 030 36301
R1	metal film resistor	50 Ω; 0.6 W		2322 156 14999
R2	metal film resistor	10 Ω; 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad PCB with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$); thickness 0.79 mm.

Table 1 Common emitter scattering parameter, I_{CQ} = 1.1 A; V_{CE} = 25 V.

f (MHZ)	S_{11}		S_{21}		S_{12}		S_{22}		G_{UM} (dB)
	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (ANG)	ANG. (DEG)	
470	0.962	176.1	1.002	68.3	0.017	32.6	0.802	−178.2	15.7
495	0.961	175.9	0.961	66.9	0.017	32.8	0.803	−178.2	15.2
520	0.959	175.7	0.923	65.7	0.017	33.6	0.804	−178.2	14.7
545	0.958	175.5	0.891	64.4	0.018	34.9	0.803	−178.3	14.3
570	0.957	175.3	0.861	63.2	0.018	35.8	0.804	−178.2	14.0
595	0.955	175.0	0.835	62.0	0.018	36.1	0.805	−178.2	13.5
620	0.953	174.8	0.815	61.0	0.019	36.8	0.804	−178.2	13.0
645	0.951	174.5	0.795	59.7	0.019	37.3	0.805	−178.1	12.7
670	0.950	174.2	0.775	58.6	0.019	37.4	0.807	−178.0	12.5
695	0.947	173.9	0.757	57.7	0.020	37.8	0.806	−178.0	12.0
720	0.943	173.7	0.744	56.6	0.021	38.5	0.805	−178.1	11.5
745	0.942	173.4	0.732	55.4	0.021	38.6	0.807	−177.9	11.3
770	0.941	173.1	0.724	54.4	0.021	39.8	0.808	−177.8	11.1
795	0.938	172.8	0.716	53.3	0.021	40.1	0.807	−177.8	10.8
820	0.935	172.5	0.707	51.8	0.022	39.1	0.808	−177.8	10.6
845	0.933	172.1	0.701	50.9	0.021	39.3	0.810	−177.6	10.4
860	0.932	171.9	0.700	50.2	0.022	39.4	0.809	−177.5	10.3

VHF power transistor BLY87C

DESCRIPTION

N-P-N silicon planar epitaxial transistor intended for use in class-A, B and C operated mobile, h.f. and v.h.f. transmitters with a nominal supply voltage of 13,5 V. The transistor is resistance stabilized and is guaranteed to withstand severe load mismatch conditions with a supply over-voltage 16,5 V.

It has a 3/8" capstan envelope with a ceramic cap. All leads are isolated from the stud.

QUICK REFERENCE DATA

R.F. performance up to T_h = 25 °C in an unneutralized common-emitter class-B circuit

MODE OF OPERATION	V_{CE} V	f MHz	P_L W	G_p dB	η %	$\bar{z}_i$ Ω	$\bar{Y}_L$ mS
c.w.	**13,5**	**175**	**8**	**> 12,0**	**> 60**	**2,2 + j0,4**	**96 − j28**
c.w.	12,5	175	8	typ. 11,5	typ. 65	–	–

PIN CONFIGURATION

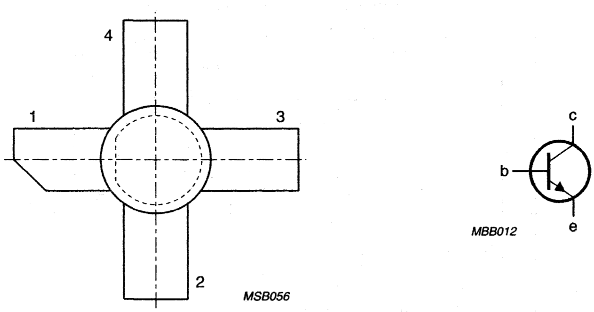


Fig.1 Simplified outline and symbol.

PINNING - SOT120

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (V_{BE} = 0)				
peak value	V_{CESM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	18	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V
Collector current (average)	$I_{C(AV)}$	max.	1,5	A
Collector current (peak value); f > 1 MHz	I_{CM}	max.	4,0	A
R.F. power dissipation (f > 1 MHz); T_{mb} = 25 °C	P_{rf}	max.	20	W
Storage temperature	T_{stg}	−65 to + 150		°C
Operating junction temperature	T_j	max.	200	°C

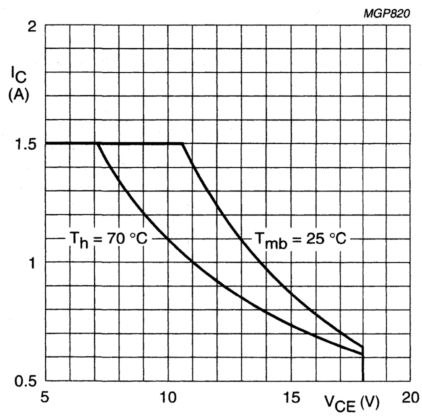
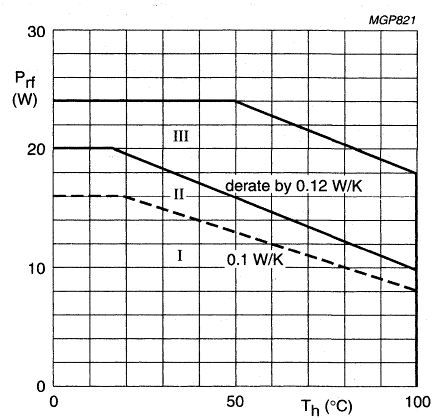


Fig.2 D.C. SOAR.



I Continuous d.c. operation
II Continuous r.f. operation
III Short-time operation during mismatch

Fig.3 R.F. power dissipation; $V_{CE} \leq$ 16,5 V; f > 1 MHz.

THERMAL RESISTANCE

(dissipation = 8 W; T_{mb} = 73,5 °C, i.e. T_h = 70 °C)

From junction to mounting base (d.c. dissipation)	$R_{th\ j\text{-}mb(dc)}$	=	10,7	K/W
From junction to mounting base (r.f. dissipation)	$R_{th\ j\text{-}mb(rf)}$	=	8,6	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,45	K/W

CHARACTERISTICS

$T_j = 25$ °C

Collector-emitter breakdown voltage				
$V_{BE} = 0$; $I_C = 5$ mA	$V_{(BR)\,CES}$	>	36	V
Collector-emitter breakdown voltage				
open base; $I_C = 25$ mA	$V_{(BR)CEO}$	>	18	V
Emitter-base breakdown voltage				
open collector; $I_E = 1$ mA	$V_{(BR)EBO}$	>	4	V
Collector cut-off current				
$V_{BE} = 0$; $V_{CE} = 18$ V	I_{CES}	<	2	mA
Second breakdown energy; L = 25 mH; f = 50 Hz				
open base	E_{SBO}	>	0,5	mJ
$R_{BE} = 10\ \Omega$	E_{SBR}	>	0,5	mJ
D.C. current gain (1)				
$I_C = 0{,}75$ A; $V_{CE} = 5$ V	h_{FE}	typ.	40	
			10 to 100	
Collector-emitter saturation voltage (1)				
$I_C = 2$ A; $I_B = 0{,}4$ A	V_{CEsat}	typ.	0,85	V
Transition frequency at f = 100 MHz (1)				
$-I_E = 0{,}75$ A; $V_{CB} = 13{,}5$ V	f_T	typ.	950	MHz
$-I_E = 2$ A; $V_{CB} = 13{,}5$ V	f_T	typ.	850	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e = 0$; $V_{CB} = 13{,}5$ V	C_c	typ.	16,5	pF
Feedback capacitance at f = 1 MHz				
$I_C = 100$ mA; $V_{CE} = 13{,}5$ V	C_{re}	typ.	12	pF
Collector-stud capacitance	C_{cs}	typ.	2	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu s$; $\delta \leq 0{,}02$.

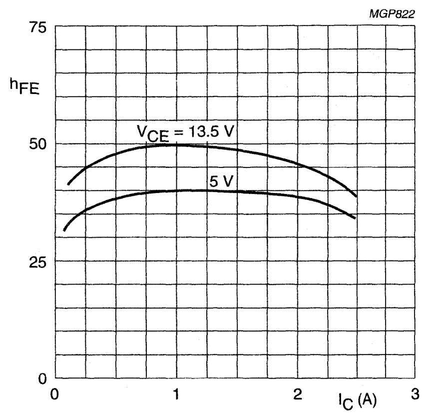


Fig.4 Typical values; $T_j = 25$ °C.

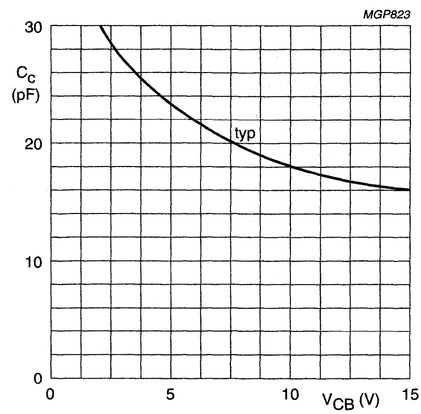


Fig.5 $I_E = I_e = 0$; f = 1 MHz; $T_j = 25$ °C.

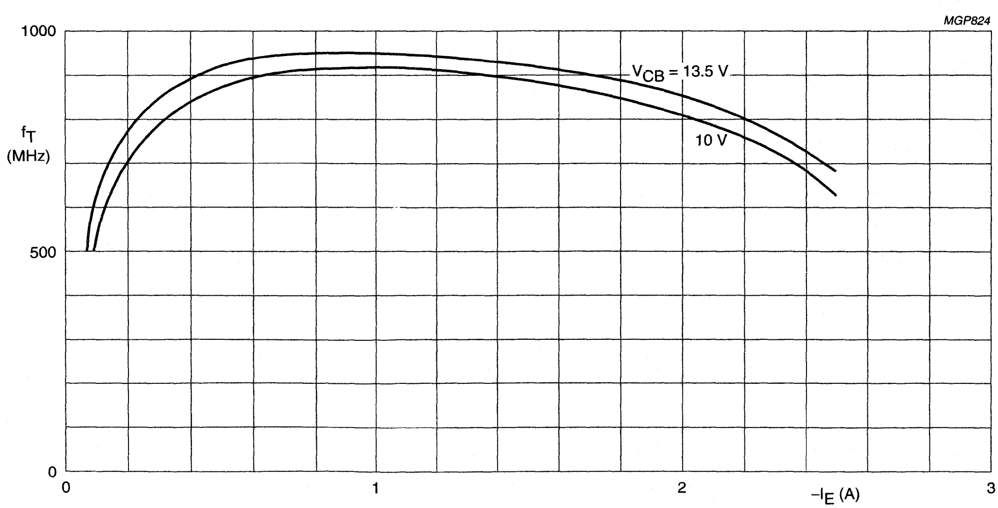


Fig.6 Typical values; f = 100 MHz; $T_j = 25$ °C.

APPLICATION INFORMATION

R.F. performance in c.w. operation (unneutralized common-emitter class-B circuit) T_h = 25 °C

f (MHz)	V_{CE} (V)	P_L (W)	P_S (W)	G_p (dB)	I_C (A)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mS)
175	**13,5**	**8**	**< 0,5**	**> 12,0**	**< 0,99**	**> 60**	**2,2 + j0,4**	**96 − j28**
175	12,5	8	−	typ. 11,5	−	typ. 65	−	−

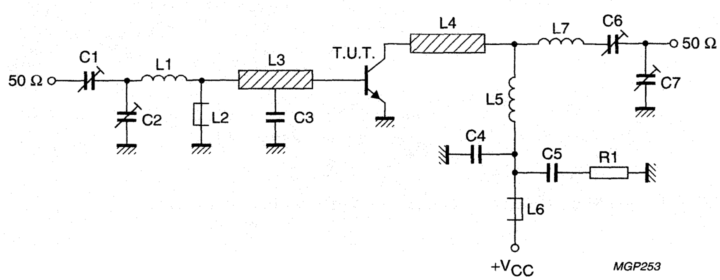


Fig.7 Test circuit; c.w. class-B.

List of components:

C1 = 2,5 to 20 pF film dielectric trimmer (cat. no. 2222 809 07004)
C2 = C6 = 4 to 40 pF film dielectric trimmer (cat. no. 2222 809 07008)
C3 = 47 pF ceramic capacitor (500 V)
C4 = 120 pF ceramic capacitor (500 V)
C5 = 100 nF polyester capacitor
C7 = 5 to 60 pF film dielectric trimmer (cat. no. 2222 809 07011)
L1 = 2 turns Cu wire (1,6 mm); int. dia. 4,5 mm; length 5,7 mm; leads 2 × 5 mm
L2 = L6 = Ferroxcube wide-band h.f. choke, grade 3B (cat. no. 4312 020 36640)
L3 = L4 = strip (12 mm × 6 mm); tap for C3 at 5 mm from transistor
L5 = 3 turns Cu wire (1,6 mm); int. dia. 7,5 mm; length 7,5 mm; leads 2 × 5 mm
L7 = 3 turns Cu wire (1,6 mm); int. dia. 6,5 mm; length 7,4 mm; leads 2 × 5 mm
L3 and L4 are strips on a double Cu-clad printed-circuit board with epoxy fibre-glass dielectric, thickness 1/16".
R1 = 10 Ω carbon resistor

Component layout and printed-circuit board for 175 MHz test circuit see Fig.8.

VHF power transistor BLY87C

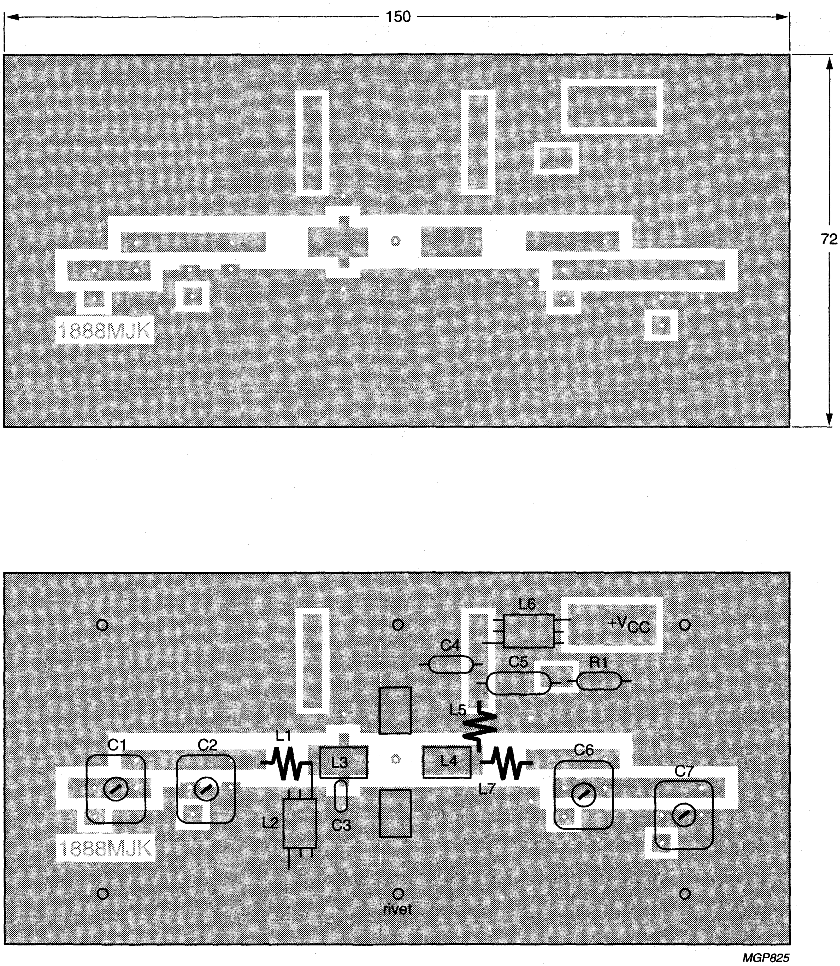


Fig.8 Component layout and printed-circuit board for 175 MHz test circuit.

The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

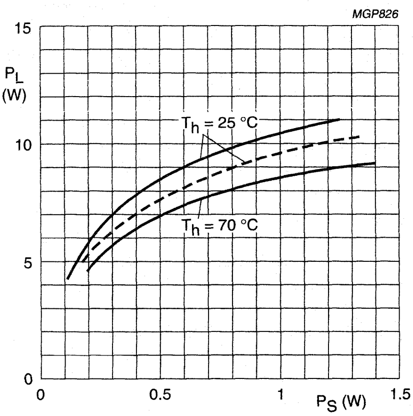


Fig.9 Typical values; f = 175 MHz;
—— V_{CE} = 13,5 V; – – – V_{CE} = 12,5 V.

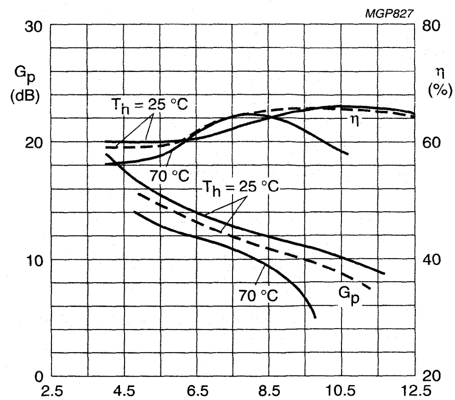


Fig.10 Typical values; f = 175 MHz;
—— V_{CE} = 13,5 V; – – – V_{CE} = 12,5 V.

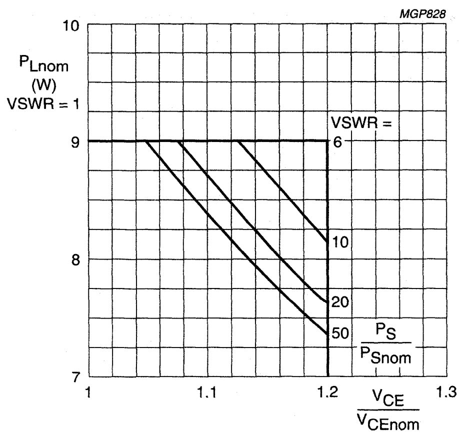
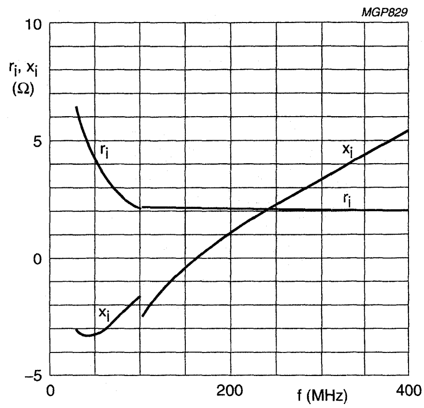


Fig.11 R.F. SOAR (short-time operation during mismatch); f = 175 MHz; T_h = 70 °C; $R_{th\ mb-h}$ = 0,45 K/W; V_{CEnom} = 13,5 V or 12,5 V; $P_S = P_{Snom}$ at V_{CEnom} and VSWR = 1.

Note to Fig.11:

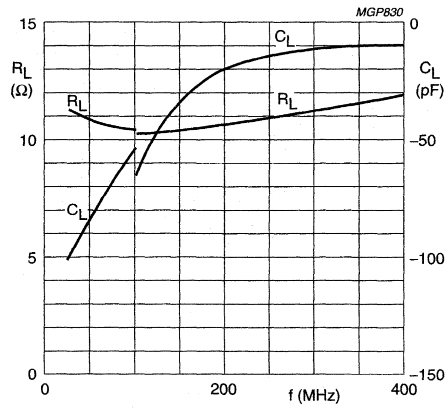
The transistor has been developed for use with unstabilized supply voltages. As the output power and drive power increase with the supply voltage, the nominal output power must be derated in accordance with the graph for safe operation at supply voltages other than the nominal. The graph shows the permissible output power under nominal conditions (VSWR = 1), as a function of the expected supply over-voltage ratio with VSWR as parameter.

The graph applies to the situation in which the drive (P_S/P_{Snom}) increases linearly with supply over-voltage ratio.



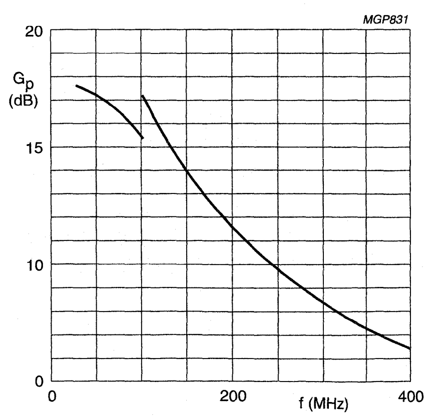
Typical values; V_{CE} = 13,5 V;
P_L = 8 W; T_h = 25 °C.

Fig.12 Input impedance (series components).



Typical values; V_{CE} = 13,5 V;
P_L = 8 W; T_h = 25 °C.

Fig.13 Load impedance (parallel components).



Typical values; V_{CE} = 13,5 V;
P_L = 8 W; T_h = 25 °C.

Fig.14

OPERATING NOTE

Below 100 MHz a base-emitter resistor of 10 Ω is recommended to avoid oscillation. This resistor must be effective for r.f. only.

FEATURES

- Diffused emitter ballasting resistors
- Self-aligned process entirely ion implanted and gold metallization
- Optimum temperature profile
- Excellent performance and reliability.

APPLICATIONS

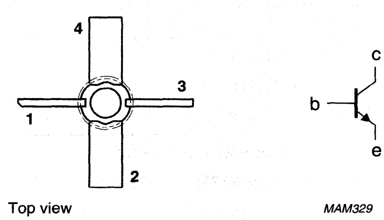
- Common emitter class-A linear power amplifiers up to 4 GHz.

DESCRIPTION

The LBE2003S and LBE2009S are NPN silicon planar epitaxial microwave power transistors in a SOT441A metal ceramic studless package.

PINNING

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter



Marking code: LBE2003S = 407; LBE2009S = 409.

Fig.1 Simplified outline and symbol (SOT441A).

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common emitter class-A amplifier.

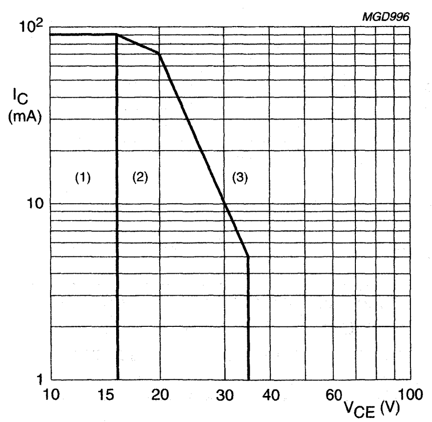
TYPE NUMBER	MODE OF OPERATION	f (GHz)	V_{CE} (V)	I_C (mA)	P_{L1} (mW)	G_{po} (dB)	Z_i (Ω)	Z_L (Ω)
LBE2003S	Class-A (CW) linear	2	18	30	≥200	≥10	6.2 + j30	17.5 + j7
LBE2009S	Class-A (CW) linear	2	18	110	≥700	≥9	7.5 + j15	17.5 + j39

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter		40	V
V_{CER}	collector-emitter voltage				
	LBE2003S	R_{BE} = 220 Ω	–	35	V
	LBE2009S	R_{BE} = 100 Ω	–	35	V
V_{CEO}	collector-emitter voltage	open base	–	16	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)				
	LBE2003S		–	90	mA
	LBE2009S		–	250	mA
P_{tot}	total power dissipation	T_{mb} ≤ 75 °C			
	LBE2003S		–	1.4	W
	LBE2009S		–	3.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	at 0.3 mm from case; t = 10 s	–	235	°C



T_{mb} ≤ 75 °C.

(1) Region of permissible DC operation.

(2) Permissible extension provided R_{BE} ≤ 220 Ω.

(3) Second breakdown limit (independent of temperature).

Fig.2 DC SOAR; LBE2003S.

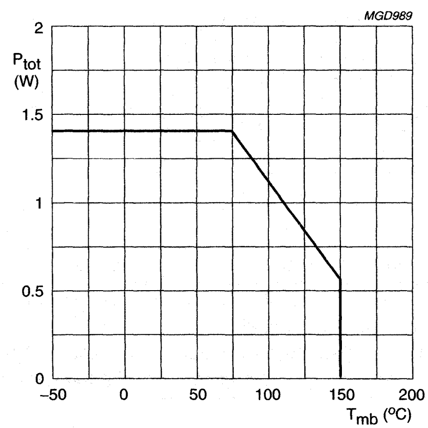
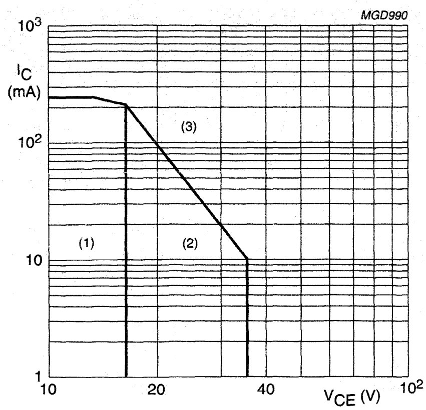


Fig.3 Power dissipation derating as a function of mounting-base temperature; LBE2003S.



$T_{mb} \leq 75$ °C.
(1) Region of permissible DC operation.
(2) Permissible extension provided $R_{BE} \leq 100\ \Omega$.
(3) Second breakdown limit (independant of temperature).

Fig.4 DC SOAR; LBE2009S.

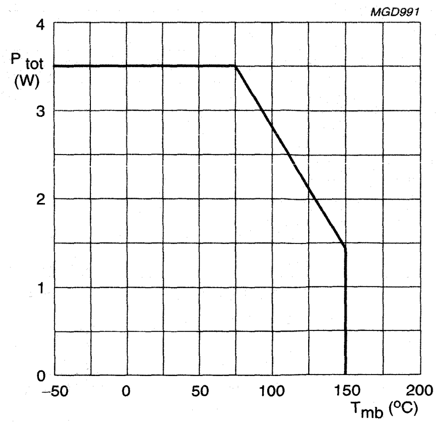


Fig.5 Power dissipation derating as a function of mounting-base temperature; LBE2009S.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	$T_j = 75$ °C		
	LBE2003S		65	K/W
	LBE2009S		36	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	$T_j = 75$ °C	1.5	K/W

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 20 V; I_E = 0	–	–	0.1	μA
I_{CBO}	collector cut-off current	V_{CB} = 40 V; I_E = 0				
	LBE2003S		–	–	150	μA
	LBE2009S		–	–	250	μA
I_{CER}	collector cut-off current					
	LBE2003S	V_{CB} = 35 V; R_{BE} = 220 Ω	–	–	500	μA
	LBE2009S	V_{CB} = 35 V; R_{BE} = 100 Ω	–	–	1000	μA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0				
	LBE2003S		–	–	0.05	μA
	LBE2009S		–	–	0.2	μA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 30 mA	15	–	150	
		V_{CE} = 5 V; I_C = 110 mA	15	–	150	
C_{cb}	collector-base capacitance	V_{CB} = 18 V; V_{EB} = 1.5 V; I_E = I_C = 0; f = 1 MHz				
	LBE2003S		–	0.3	–	pF
	LBE2009S		–	0.6	–	pF
C_{ce}	collector-emitter capacitance	V_{CE} = 18 V; V_{EB} = 1.5 V; I_E = I_C = 0; f = 1 MHz				
	LBE2003S		–	0.45	–	pF
	LBE2009S		–	0.6	–	pF
C_{eb}	emitter-base capacitance	V_{CB} = 10 V; V_{EB} = 1 V; I_E = I_C = 0; f = 1 MHz				
	LBE2003S		–	1.7	–	pF
	LBE2009S		–	3.3	–	pF

Table 1 Scattering parameters LBE2003S: V_{CE} = 18 V; I_C = 30 mA (V_{CE} and I_C regulated); T_{mb} = 25 °C; Z_o = 50 Ω; typical values. (The figures given between brackets are values in dB).

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
500	0.56	−143	0.037 (−28.6)	41	9.50 (19.6)	101	0.56	−34
600	0.55	−154	0.040 (−28.0)	39	8.28 (18.4)	93	0.51	−35
700	0.55	−164	0.040 (−27.9)	40	7.13 (17.1)	88	0.50	−36
800	0.55	−171	0.041 (−27.7)	40	6.35 (16.1)	82	0.49	−37
900	0.55	−178	0.043 (−27.4)	41	5.69 (15.1	77	0.47	−38
1000	0.55	176	0.045 (−26.9)	40	5.14 (14.2	72	0.46	−39
1100	0.55	170	0.048 (−26.4)	40	4.72 (13.5	68	0.46	−39
1200	0.55	165	0.051 (−25.9)	41	4.37 (12.8	64	0.45	−41
1300	0.56	159	0.056 (−25.1)	41	4.05 (12.2	60	0.44	−44
1400	0.55	158	0.060 (−24.5)	41	3.76 (11.5	57	0.45	−46
1500	0.55	149	0.062 (−24.2)	40	3.52 (10.9	53	0.43	−48
1600	0.55	146	0.065 (−23.8)	42	3.33 (10.5	50	0.43	−50
1700	0.56	142	0.068 (−23.3)	42	3.15 (10.0	46	0.43	−53
1800	0.57	137	0.070 (−23.1)	41	2.96 (9.4)	42	0.43	−54
1900	0.57	132	0.072 (−22.9)	40	2.80 (8.9)	39	0.43	−56
2000	0.58	128	0.074 (−22.7)	40	2.66 (8.5)	36	0.42	−57
2200	0.60	121	0.081 (−21.8)	39	2.43 (7.7)	28	0.41	−61
2400	0.62	114	0.091 (−20.8)	37	2.24 (7.0)	23	0.40	−67
2600	0.64	108	0.099 (−20.1)	36	2.08 (6.4)	16	0.39	−75
2800	0.66	102	0.105 (−19.6)	33	1.90 (5.6)	10	0.38	−82
3000	0.68	96	0.108 (−19.4)	31	1.79 (5.1)	4	0.39	−87
3200	0.71	92	0.124 (−18.7)	29	1.63 (4.3)	−2	0.37	−94
3400	0.73	89	0.125 (−18.0)	27	1.58 (4.0)	−7	0.40	−101
3600	0.75	86	0.137 (−17.3)	25	1.46 (3.3)	−13	0.39	−112
3800	0.76	82	0.142 (−17.0)	23	1.40 (2.9)	−18	0.38	−120
4000	0.77	79	0.149 (−16.6)	20	1.31 (2.3)	−24	0.38	−128
4200	0.78	75	0.155 (−16.2)	17	1.25 (1.9)	−28	0.38	−133
4400	0.80	73	0.167 (−15.5)	15	1.20 (1.6)	−34	0.39	−142
4600	0.81	69	0.177 (−15.0)	12	1.14 (1.1)	−38	0.39	−151
4800	0.81	68	0.187 (−14.6)	10	1.10 (0.8)	−43	0.42	−159
5000	0.81	65	0.194 (−14.3)	6	1.04 (0.4)	−47	0.44	−165
5200	0.80	60	0.203 (−13.8)	4	1.03 (0.3)	−53	0.47	−169
5400	0.81	56	0.219 (−13.2)	−1	0.98 (−0.2)	−57	0.48	−175
5600	0.81	51	0.229 (−12.8)	−3	0.97 (−0.3)	−62	0.49	−178
5800	0.81	48	0.243 (−12.3)	−8	0.92 (−0.7)	−68	0.51	−171
6000	0.80	44	0.245 (−12.2)	−12	0.90 (−0.9)	−72	0.55	−165

Table 2 Scattering parameters LBE2009S: V_{CE} = 18 V; I_C = 110 mA (V_{CE} and I_C regulated); T_{mb} = 25 °C; Z_o = 50 Ω; typical values. (The figures given between brackets are values in dB).

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
500	0.70	177	0.029 (−30.7)	50	7.55 (17.6)	83	0.25	−48
600	0.70	171	0.033 (−29.6)	51	6.43 (16.2)	77	0.22	−50
700	0.70	168	0.036 (−29.0)	53	5.46 (14.6)	73	0.23	−52
800	0.70	163	0.039 (−28.4)	54	4.80 (13.6)	68	0.22	−54
900	0.71	159	0.041 (−27.8)	54	4.27 (12.6)	64	0.22	−56
1000	0.71	155	0.045 (−27.0)	55	3.84 (11.7)	60	0.21	−59
1100	0.71	151	0.049 (−26.2)	54	3.53 (11.0)	56	0.21	−62
1200	0.71	148	0.054 (−25.4)	54	3.27 (10.3)	52	0.21	−65
1300	0.71	144	0.060 (−24.5)	53	3.01 (9.6)	48	0.20	−74
1400	0.72	143	0.066 (−23.6)	54	2.80 (9.0)	45	0.20	−79
1500	0.72	136	0.070 (−23.1)	52	2.61 (8.3)	41	0.21	−80
1600	0.72	133	0.075 (−22.5)	53	2.47 (7.9)	38	0.21	−83
1700	0.72	130	0.080 (−21.9)	51	2.33 (7.3)	34	0.22	−87
1800	0.73	127	0.084 (−21.5)	49	2.18 (6.8)	30	0.22	−90
1900	0.73	123	0.087 (−21.2)	48	2.05 (6.3)	26	0.22	−94
2000	0.74	120	0.090 (−20.9)	46	1.97 (5.9)	23	0.22	−97
2200	0.75	114	0.100 (−20.0)	43	1.78 (5.0)	15	0.22	−109
2400	0.77	108	0.112 (−19.0)	40	1.63 (4.3)	10	0.21	−122
2600	0.79	103	0.123 (−18.2)	37	1.51 (3.6)	2	0.24	−133
2800	0.80	97	0.129 (−17.8)	33	1.36 (2.7)	−4	0.25	−143
3000	0.81	92	0.134 (−17.5)	30	1.28 (2.1)	−11	0.27	−151
3200	0.83	88	0.143 (−16.9)	26	1.15 (1.2)	−17	0.28	−163
3400	0.85	85	0.152 (−16.4)	24	1.10 (0.9)	−21	0.30	−173
3600	0.86	82	0.163 (−15.8)	20	1.00 (0)	−28	0.34	178
3800	0.87	79	0.168 (−15.5)	17	0.96 (−0.4)	−32	0.37	173
4000	0.88	75	0.175 (−15.2)	14	0.88 (−1.1)	−39	0.41	168
4200	0.88	71	0.180 (−14.9)	11	0.83 (−1.6)	−42	0.42	162
4400	0.89	69	0.193 (−14.3)	8	0.79 (−2.1)	−48	0.45	155
4600	0.90	66	0.200 (−14.0)	5	0.74 (−2.6)	−51	0.48	149
4800	0.90	64	0.211 (−13.5)	2	0.71 (−3.0)	−56	0.52	145
5000	0.90	61	0.214 (−13.4)	−2	0.66 (−3.6)	−59	0.55	144

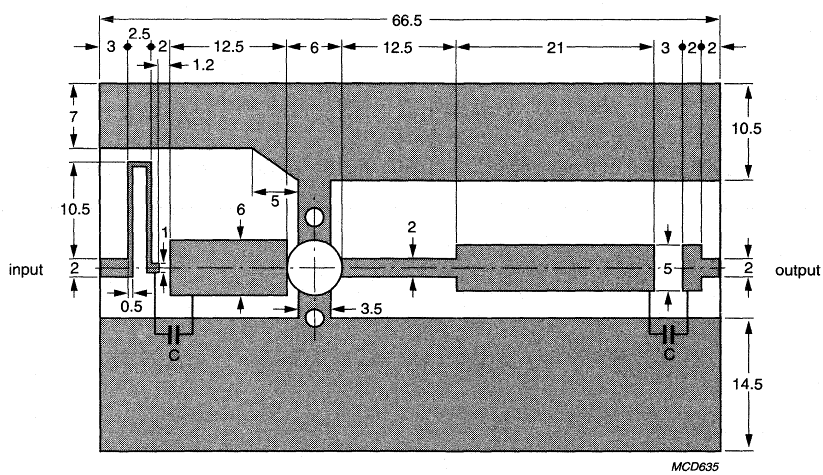
APPLICATION INFORMATION

Microwave performance for LBE2003S up to T_{mb} = 25 °C in a common emitter class-A test circuit; note 1.

MODE OF OPERATION	f (GHz)	V_{CE} (V) (2)	I_C (mA) (2)	P_{L1} (mW) (3)	G_{po} (dB) (4)	Z_i (Ω)	Z_L (Ω)
Class-A (CW)	2	18	30	≥200 (23) typ. 250 (24)	≥10 typ. 11	6.2 + j30	17.5 + j7

Notes

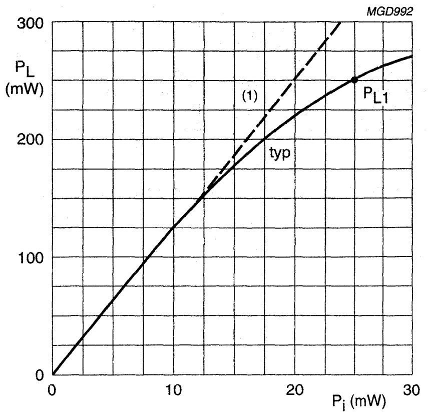
1. Circuit consists of prematching circuit boards in combination with complementary input and output slug tuners.
2. I_C and V_{CE} regulated.
3. Load power for 1 dB compressed power gain.
4. Low level power gain associated with P_{L1}.



Dimensions in mm.

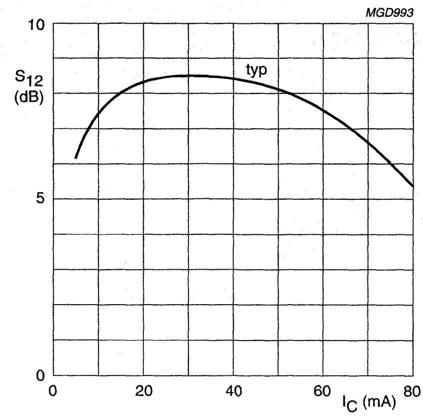
Striplines on a double copper-clad printed-circuit board with PTFE fibreglass dielectric (ε_r = 2.54); thickness: 0.8 mm.

Fig.6 Prematching test circuit board for 2 GHz.



f = 2 GHz; T_{mb} = 25 °C.
V_{CE} = 18 V; I_C = 30 mA.
(1) G_{po} = 11 dB.

Fig.7 Load power as a function of input power.



Class-A operation.
f = 2 GHz; T_{mb} = 25 °C; V_{CE} = 18 V.

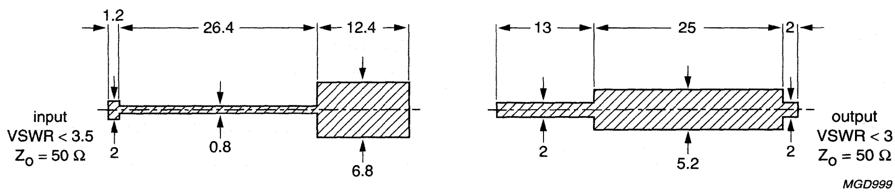
Fig.8 s_{12} as a function of collector current.

Microwave performance for LBE2009S up to T_{mb} = 75 °C in a common emitter class-A test circuit; note 1.

MODE OF OPERATION	f (GHz)	V_{CE} (V) (2)	I_C (mA) (2)	P_{L1} (mW) (3)	G_{po} (dB) (4)	Z_i (Ω)	Z_L (Ω)
Class-A (CW)	2	18	110	≥700 (28.5) typ. 900 (29.5)	≥9 typ. 9.8	7.5 + j14.5	17.5 + j38.5

Notes

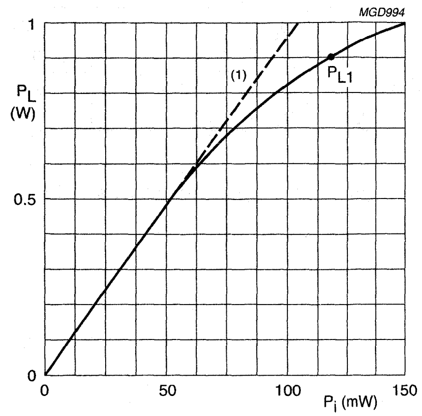
1. Circuit consists of prematching circuit boards in combination with complementary input and output slug tuners.
2. I_C and V_{CE} regulated.
3. Load power for 1 dB compressed power gain.
4. Low level power gain associated with P_{L1}.



Dimensions in mm.

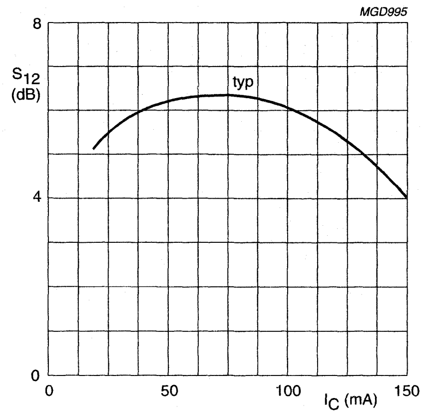
Striplines on a double copper-clad printed-circuit board with PTFE fibreglass dielectric (ε_r = 2.54); thickness: 0.8 mm.

Fig.9 Prematching test circuit board for 2 GHz.



f = 2 GHz; T_{mb} = 25 °C.
V_{CE} = 18 V; I_C = 110 mA.
(1) G_{po} = 9.8 dB.

Fig.10 Load power as a function of input power.



Class-A operation.
f = 2 GHz; T_{mb} = 25 °C; V_{CE} = 18 V.

Fig.11 S_{12} as a function of collector current.

NPN microwave power transistor | LTE21009R

FEATURES

- Diffused emitter ballasting resistors
- Self-aligned process entirely ion implanted and gold sandwich metallization
- optimum temperature profile
- excellent performance and reliability
- Input matching cell improves input impedance and facilitates the design of wideband circuits.

APPLICATIONS

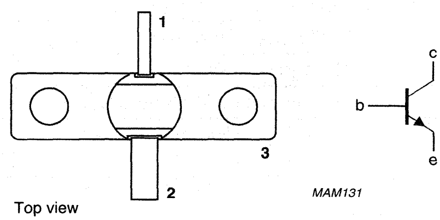
- Common emitter class-A linear power amplifiers up to 4.2 GHz.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT440A metal ceramic flange package with the emitter connected to the flange.

PINNING - SOT440A

PIN	DESCRIPTION
1	collector
2	base
3	emitter connected to flange



Marking code: 435

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common emitter class-A amplifier.

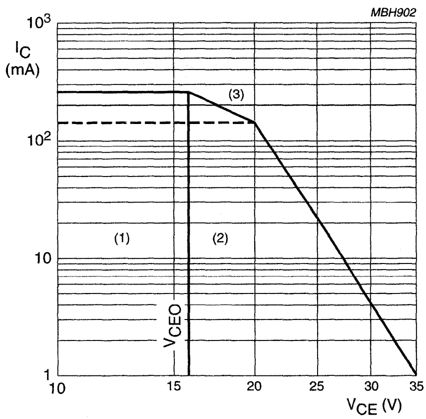
MODE OF OPERATION	f (GHz)	V_{CE} (V)	I_C (mA)	P_{L1} (W)	G_{po} (dB)
Class-A	2.1	16	150	≥0.6	≥10

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CER}	collector-emitter voltage	$R_{BE} = 100\ \Omega$	–	35	V
V_{CEO}	collector-emitter voltage	open base	–	16	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	DC collector current (DC)		–	250	mA
P_{tot}	total power dissipation	$T_{mb} \leq 75$ °C	–	4	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.3 mm from case; $t \leq 10$ s	–	235	°C



$T_{mb} = 75$ °C.
(1) Region of permissible DC operation.
(2) Permissible extension provided $R_{BE} < 100\ \Omega$.
(3) Second breakdown limit (independent of temperature).

Fig.2 DC SOAR.

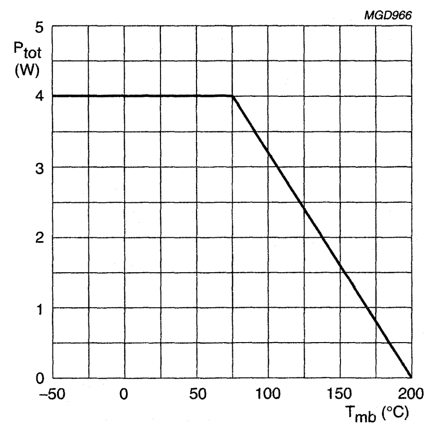


Fig.3 Power dissipation derating as a function of mounting-base temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C	36	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.7	K/W

Note

1. See "*Mounting recommendations in the General part of handbook SC19a*".

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 20 V; I_E = 0	–	50	μA
		V_{CB} = 40 V; I_E = 0	–	0.4	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	–	200	nA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 150 mA	15	150	

NPN microwave power transistor | LTE42005S

FEATURES

- Diffused emitter ballasting resistors provide excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Input matching cell improves input impedance and allows an easier design of circuits

APPLICATION

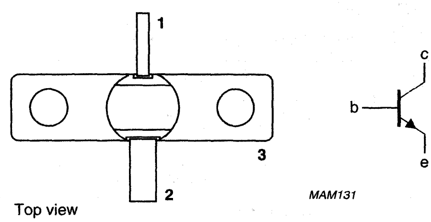
- Common emitter class-A linear power amplifiers up to 4.2 GHz.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT440A metal ceramic flange package with the emitter connected to the flange.

PINNING - SOT440A

PIN	DESCRIPTION
1	collector
2	base
3	emitter connected to flange



Marking code: 502

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common emitter class-A amplifier.

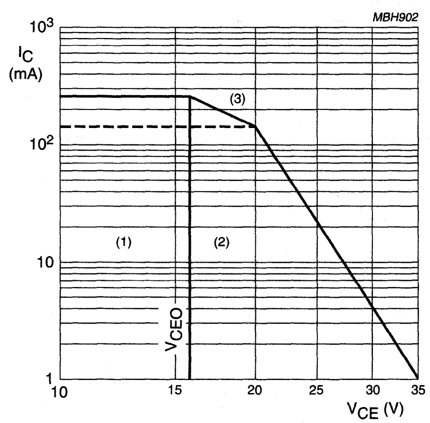
MODE OF OPERATION	f (GHz)	V_{CE} (V)	I_C (mA)	P_{L1} (mW)	G_{po} (dB)	Z_i (Ω)	Z_L (Ω)
Class-A (CW) linear	4.2	18	110	≥450	≥6.6	100 + j40	4 + j4

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CER}	collector-emitter voltage	$R_{BE} = 100\ \Omega$	–	35	V
V_{CEO}	collector-emitter voltage	open base	–	16	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	250	mA
P_{tot}	total power dissipation	$T_{mb} \leq 75$ °C	–	4	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	at 0.3 mm from case; t = 10 s	–	235	°C



$T_{mb} \leq 75$ °C.

(1) Region of permissible DC operation.

(2) Permissible extension provided $R_{BE} \leq 100\ \Omega$.

(3) Second breakdown limit (independent of temperature).

Fig.2 DC SOAR.

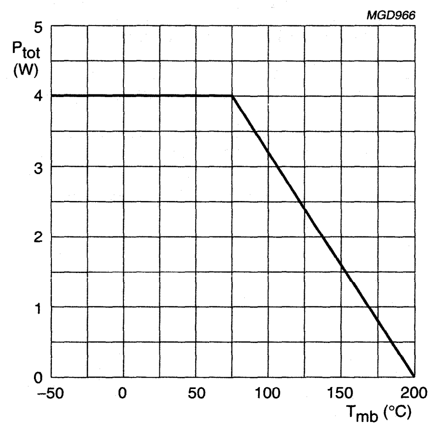


Fig.3 Power dissipation derating as a function of mounting-base temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	$T_j = 75\ °C$	36	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	$T_j = 75\ °C$; note 1	0.7	K/W

Note

1. See "*Mounting recommendations in the General part of handbook SC19a*".

CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$V_{CB} = 20\ V$; $I_E = 0$	–	–	0.1	μA
		$V_{CB} = 40\ V$; $I_E = 0$	–	–	0.25	mA
I_{CER}	emitter cut-off current	$V_{CE} = 35\ V$; $R_{BE} = 100\ \Omega$	–	–	1	mA
I_{EBO}	emitter cut-off current	$V_{EB} = 1.5\ V$; $I_C = 0$	–	–	0.2	μA
h_{FE}	DC current gain	$V_{CE} = 5\ V$; $I_C = 110\ mA$	15	–	150	
C_{cb}	collector-base capacitance	$V_{CB} = 20\ V$; $V_{EB} = 1.5\ V$; $I_E = I_C = 0$; f = 1 MHz	–	0.5	–	pF
C_{ce}	collector-emitter capacitance	$V_{CE} = 20\ V$; $V_{EB} = 1.5\ V$; $I_E = I_C = 0$; f = 1 MHz	–	1.5	–	pF
C_{eb}	emitter-base capacitance	$V_{CB} = 10\ V$; $V_{EB} = 1\ V$; $I_C = I_E = 0$; f = 1 MHz	–	6.5	–	pF

Table 1 Scattering parameters: V_{CE} = 18 V; I_C = 110 mA (V_{CE} and I_C regulated); T_{mb} = 25 °C; Z_o = 50 Ω; typical values. (The figures given between brackets are values in dB).

f (MHz)	s_{11} MAGNITUDE (ratio)	s_{11} ANGLE (deg)	s_{21} MAGNITUDE (ratio)	s_{21} ANGLE (deg)	s_{12} MAGNITUDE (ratio)	s_{12} ANGLE (deg)	s_{22} MAGNITUDE (ratio)	s_{22} ANGLE (deg)
500	0.76	−176	0.022 (−33.2)	37	8.13 (18.2)	85	0.35	−62
600	0.75	180	0.023 (−32.8)	37	6.95 (16.8)	78	0.34	−66
700	0.76	177	0.023 (−32.8)	40	5.95 (15.5)	73	0.34	−71
800	0.76	174	0.024 (−32.5)	41	5.25 (14.4)	67	0.35	−75
900	0.76	171	0.024 (−32.3)	42	4.69 (13.4)	62	0.35	−79
1000	0.75	168	0.026 (−31.8)	43	4.23 (12.5)	57	0.36	−83
1100	0.75	165	0.028 (−31.0)	43	3.88 (11.8)	53	0.37	−87
1200	0.74	163	0.031 (−30.1)	43	3.61 (11.2)	49	0.39	−90
1300	0.75	160	0.035 (−29.2)	43	3.36 (10.5)	44	0.40	−95
1400	0.74	162	0.037 (−28.5)	44	3.12 (9.9)	41	0.43	−98
1500	0.73	157	0.041 (−27.8)	46	2.95 (9.4)	37	0.43	−101
1600	0.73	155	0.045 (−27.0)	46	2.83 (9.0)	32	0.45	−104
1700	0.71	154	0.047 (−26.5)	44	2.70 (8.6)	28	0.47	−107
1800	0.70	151	0.049 (−26.1)	43	2.56 (8.2)	23	0.48	−110
1900	0.69	148	0.050 (−25.9)	42	2.44 (7.7)	19	0.50	−114
2000	0.68	143	0.051 (−25.9)	39	2.34 (7.4)	14	0.51	−116
2200	0.67	138	0.058 (−24.7)	36	2.16 (6.7)	4	0.55	−124
2400	0.65	134	0.067 (−23.5	34	2.02(6.1)	−2	0.59	−129
2600	0.62	129	0.077 (−22.3)	31	1.95 (5.8)	−12	0.64	−134
2800	0.57	122	0.082 (−21.7)	25	1.84 (5.3)	−21	0.68	−138
3000	0.52	113	0.086 (−21.3)	21	1.78 (5.0)	−32	0.72	−143
3200	0.49	104	0.093 (−20.6)	16	1.67 (4.5)	−42	0.74	−150
3400	0.45	99	0.102 (−19.8)	13	1.62 (4.2)	−52	0.80	−157
3600	0.38	92	0.113 (−18.9)	8	1.52 (3.6)	−64	0.80	−163
3800	0.29	83	0.119 (−18.5)	6	1.43 (3.1)	−76	0.82	−170
4000	0.24	69	0.137 (−17.3)	2	1.27 (2.1)	−88	0.80	−179
4200	0.20	54	0.165 (−15.7)	−5	1.08 (0.7)	−98	0.68	171
4400	0.15	28	0.202 (−13.9)	−20	0.92 (0.8	−100	0.51	172
4600	0.12	−36	0.206 (−13.7)	−38	0.93 (0.6)	−102	0.52	−174
4800	0.17	−86	0.195 (−14.2)	−52	0.97 (−0.3)	−110	0.63	−171
5000	0.24	−114	0.177 (−15.0)	−65	0.97 (−0.3)	−122	0.73	−174
5200	0.31	−137	0.164 (−15.7	−73	0.93 (−0.6)	−133	0.79	−180
5400	0.41	−152	0.154 (−16.2)	−83	0.88 (−1.1)	−145	0.83	174
5600	0.48	−161	0.134 (−17.4)	−90	0.81 (−1.8)	−156	0.85	166
5800	0.53	−168	0.122 (−18.2)	−97	0.77 (−2.3)	−167	0.87	160
6000	0.56	−179	0.105 (−19.6)	−104	0.70 (−3.1)	−178	0.89	154

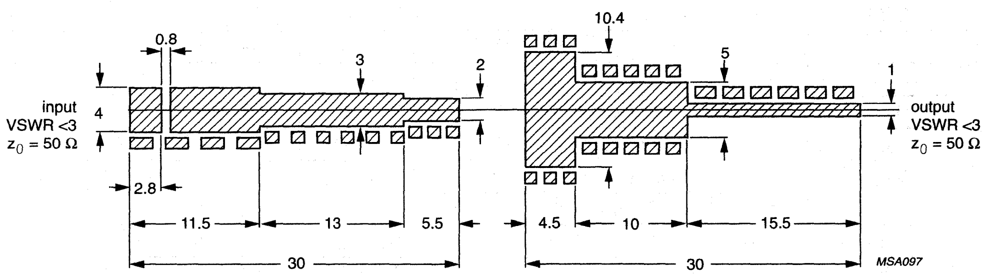
APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C in a common emitter class-A test circuit; note 1.

MODE OF OPERATION	f (GHz)	V_{CE} (V) (2)	I_C (mA) (2)	P_{L1} (mW) (3)	G_{po} (dB) (4)	Z_i (Ω)	Z_L (Ω)
Class-A (CW)	4.2	18	110	≥450 (26.5) typ. 550 (27.4)	≥6.6 typ. 7.2	100 + j40	4 + j4

Notes

1. Circuit consists of prematching circuit boards in combination with complementary input and output slug tuners.
2. I_C and V_{CE} regulated.
3. Load power for 1 dB compressed power gain.
4. Low level power gain associated with P_{L1}.

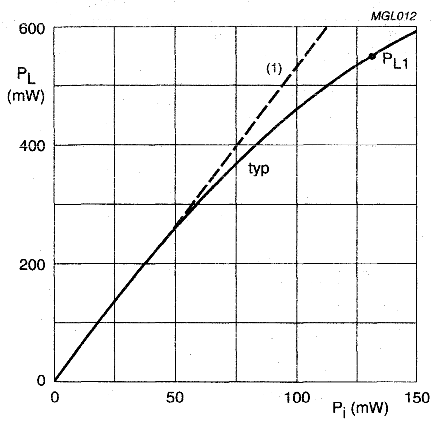


Dimensions in mm.

Input striplines on a double copper-clad printed-circuit board with PTFE fibreglass dielectric (ε_r = 2.54); thickness: 1.6 mm.

Output striplines on a double copper-clad Rexolite printed-circuit board with dielectric (ε_r = 2.4); thickness: 0.25 mm.

Fig.4 Prematching test circuit board.



f = 4.2 GHz; T_{mb} = 25 °C.
V_{CE} = 18 V; I_C = 110 mA (both regulated).
(1) G_{po} = 7.2 dB.

Fig.5 Load power as a function of input power.

NPN microwave power transistor | LTE42012R

FEATURES

- Interdigitated structure provides high emitter efficiency
- Diffused emitter ballasting resistor provides excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry gives good balance of dissipated power and low thermal resistance
- Input matching cell improves input impedance and allows an easier design of wideband circuits.

APPLICATIONS

- Common emitter class-A power amplifiers up to 4.2 GHz in CW conditions for military and professional applications.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT440A metal ceramic flange package with the emitter connected to the flange.

PINNING - SOT440A

PIN	DESCRIPTION
1	collector
2	base
3	emitter connected to flange

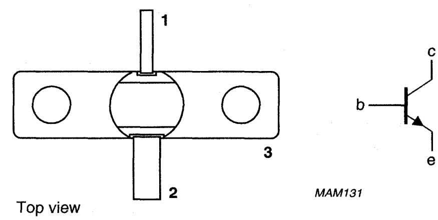


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Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common emitter class-A selective amplifier.

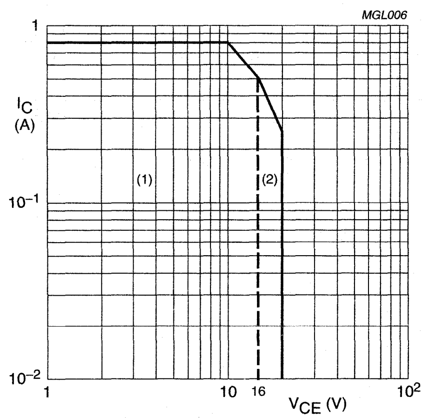
MODE OF OPERATION	f (GHz)	V_{CE} (V)	I_C (mA)	P_{L1} (W)	G_{po} (dB)	Z_i (Ω)	Z_L (Ω)
Class-A (CW)	4.2	16	400	≥1	≥6	7.5 + j12	4 – j8

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CER}	collector-emitter voltage	$R_{BE} = 70\ \Omega$	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	16	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{mb} \leq 75\ °C$	–	8	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	at 0.1 mm from ceramic; $t \leq 10$ s	–	235	°C



$T_{mb} \leq 75$ °C.

(1) Region of permissible DC operation.

(2) Permissible extension provided $R_{BE} \leq 70\ \Omega$.

Fig.2 DC SOAR.

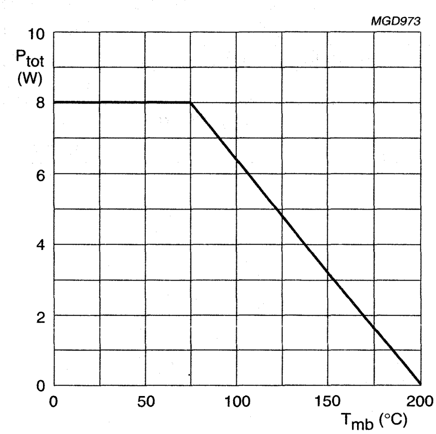


Fig.3 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	T_j = 75 °C	10	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	T_j = 75 °C; note 1	0.7	K/W

Note

1. See "*Mounting recommendations in the General part of handbook SC19a*".

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 20 V; I_E = 0	–	–	200	μA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	–	–	600	nA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 400 mA	15	–	100	
C_{cb}	collector-base capacitance	V_{CB} = 16 V; V_{EB} = 1.5 V; I_E = I_C = 0; f = 1 MHz	–	3	–	pF
C_{ce}	collector-emitter capacitance	V_{CE} = 16 V; V_{EB} = 1.5 V; I_E = I_C = 0; f = 1 MHz	–	1.5	–	pF
C_{eb}	emitter-base capacitance	V_{CB} = 10 V; V_{EB} = 1 V; I_C = I_E = 0; f = 1 MHz	–	28	–	pF

Table 1 Common-emitter scattering parameters: V_{CE} = 16 V; I_C = 400 mA; T_{mb} = 25 °C; Z_o = 50 Ω; typical values.

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
2000	0.84	163	0.049	64	0.96	47.2	0.60	179.3
2100	0.84	161	0.051	62.7	0.94	43.3	0.59	178.0
2200	0.84	159	0.054	60.4	0.93	39.8	0.59	175.6
2300	0.85	158	0.055	58.8	0.91	36.2	0.59	174.2
2400	0.85	156	0.057	57.5	0.91	32.2	0.60	172.6
2500	0.85	155	0.060	56.1	0.90	29.1	0.60	171.1
2600	0.85	154	0.064	54.9	0.89	24.6	0.60	169.8
2700	0.85	153	0.067	53.1	0.89	21.2	0.60	168.6
2800	0.85	152	0.071	51.3	0.89	17.2	0.61	167.1
2900	0.84	150	0.073	49.5	0.90	13.8	0.62	165.7
3000	0.83	149	0.076	48.0	0.90	9.3	0.62	164.7
3100	0.82	149	0.080	46.0	0.91	5.2	0.63	163.8
3200	0.80	147	0.084	44.1	0.92	0.6	0.64	163.0
3300	0.78	146	0.088	40.5	0.93	−4.3	0.65	161.5
3400	0.76	145	0.091	36.1	0.95	−9.7	0.67	160.9
3500	0.74	144	0.093	34.4	0.97	−16.1	0.69	159.6
3600	0.71	143	0.095	30.7	0.98	−23.2	0.70	158.3
3700	0.70	142	0.095	26.3	0.99	−30.6	0.73	156.2
3800	0.67	142	0.093	21.6	0.99	−37.9	0.76	153.6
3900	0.66	142	0.091	17.0	1.00	−46.6	0.79	150.7
4000	0.64	142	0.088	13.2	0.98	−55.8	0.82	147.0
4100	0.64	142	0.084	9.7	0.95	−64.9	0.85	143.1
4200	0.65	143	0.077	7.0	0.91	−73.8	0.88	138.4
4300	0.67	143	0.068	5.9	0.86	−82.6	0.90	133.6
4400	0.69	143	0.060	8.2	0.81	−92.3	0.93	129.3
4500	0.72	141	0.054	13.8	0.74	−101.7	0.94	124.9
4600	0.75	139	0.050	20.5	0.68	−110.6	0.95	120.1
4700	0.76	137	0.050	31.2	0.61	−119.7	0.96	116.5
4800	0.78	135	0.054	43.5	0.56	−129.1	0.97	113.5
4900	0.79	133	0.061	46.6	0.50	−139.5	0.97	110.1
5000	0.77	130	0.068	54.3	0.44	−148.6	0.97	106.7

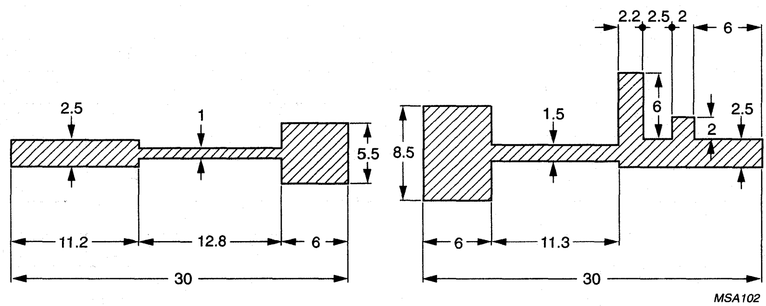
APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C in a common emitter class-A selective circuit; note 1.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	I_C (mA)	P_{L1} (W)	G_{po} (dB)	Z_i (Ω)	Z_L (Ω)
Class-A	4.2	16	400	>1 typ. 1.25	>6 typ. 7	7.5 + j12	4 – j8

Note

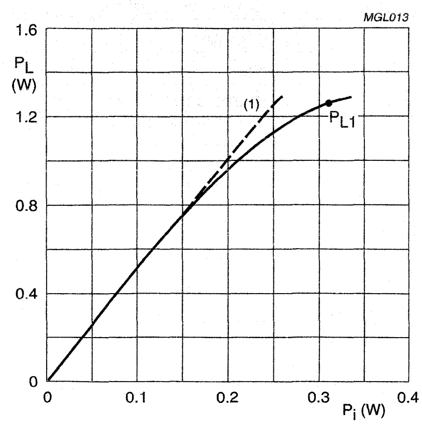
1. Circuit consists of prematching circuit boards in combination with complementary input and output slug tuners.



Dimensions in mm.

Input striplines on a double copper-clad printed-circuit board with PTFE fibreglass dielectric (ε_r = 2.54); thickness: 0.8 mm.

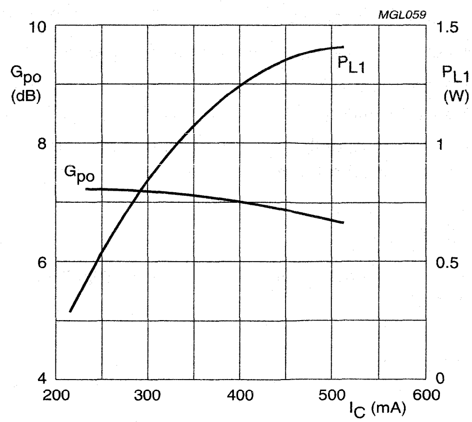
Fig.4 Prematching test circuit board.



f = 4.2 GHz; V_{CE} = 16 V; I_C = 400 mA (regulated).

(1) G_{po} = 7 dB.

Fig.5 Load power as a function of input power.



f = 4.2 GHz; V_{CE} = 16 V.

Fig.6 Low level power gain associated with P_{L1} as a function of collector current.

NPN microwave power transistor LVE21050R

FEATURES

- Diffused emitter ballasting resistors provide excellent current sharing and withstanding a high VSWR
- Self-aligned process entirely ion implanted
- Gold metallization ensures an optimum temperature profile with excellent performance and reliability
- Input matching cell improves input impedance and allows an easier design of wideband circuits.

APPLICATIONS

- Common emitter class-A linear power amplifiers up to 4.2 GHz.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT445A metal ceramic flange package with the emitter connected to the flange.

PINNING - SOT445A

PIN	DESCRIPTION
1	collector
2	base
3	emitter connected to flange

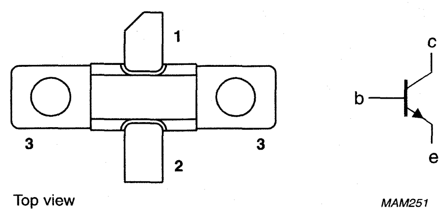


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common emitter class-A circuit.

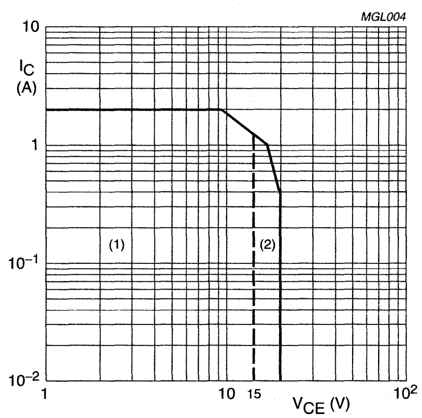
MODE OF OPERATION	f (GHz)	V_{CC} (V)	I_C (A)	P_{L1} (W)	G_{po} (dB)	Z_i; Z_L (Ω)
Class-A (CW)	2.1	16	1.1	typ. 5.5	typ. 8	see Fig 4

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CER}	collector-emitter voltage	R_{BE} = 47 Ω	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	16	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	2	A
P_{tot}	total power dissipation	$T_{mb} \leq 75$ °C	–	18	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	at 0.3 mm from case; $t \leq 10$ s	–	235	°C



$T_{mb} \leq 75$ °C.

(1) Region of permissible DC operation.

(2) Permissible extension provided $R_{BE} \leq 47$ Ω.

Fig.2 DC SOAR.

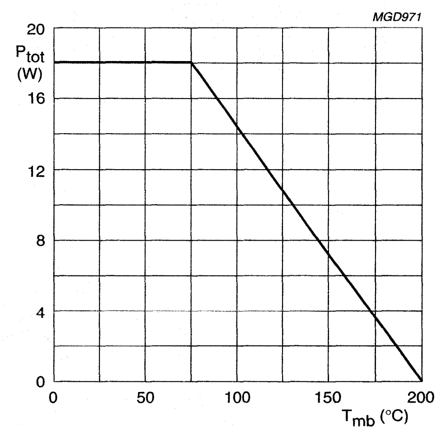


Fig.3 Power dissipation derating as a function of mounting base temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	$T_j = 75\ °C$	4	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	$T_j = 75\ °C$; note 1	0.7	K/W

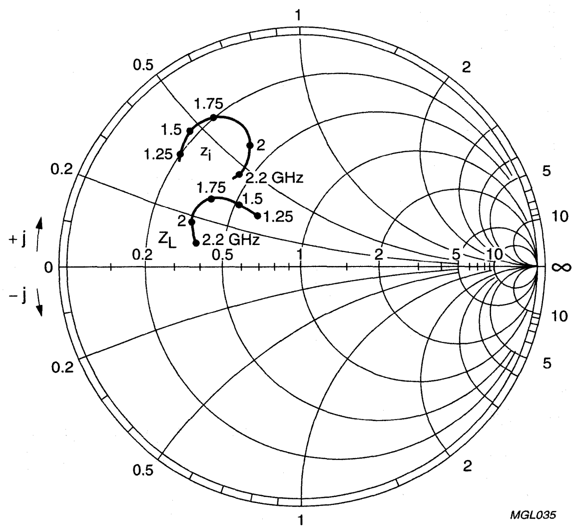
Note

1. See *"Mounting recommendations in the General part of handbook SC19a".*

CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$V_{CB} = 20\ V$; $I_E = 0$	–	–	0.5	mA
		$V_{CB} = 40\ V$; $I_E = 0$	–	–	2.5	mA
I_{CER}	collector cut-off current	$V_{CE} = 20\ V$; $R_{BE} = 47\ \Omega$	–	–	25	mA
I_{CEO}	collector cut-off current	$V_{CE} = 15\ V$; $I_B = 0$	–	–	2	mA
I_{EBO}	emitter cut-off current	$V_{EB} = 1.5\ V$; $I_C = 0$	–	–	100	μA
h_{FE}	DC current gain	$V_{CE} = 3\ V$; $I_C = 1\ A$	15	–	100	



$Z_o = 10\ \Omega$.

Fig.4 Input and optimum load impedances as functions of frequency; typical values.

Microwave power transistor | MF1011B900Y

FEATURES

- Suitable for short and medium pulse applications up to 100 μs pulse width, duty factor 10%
- Diffused emitter ballasting resistors improve ruggedness
- Interdigitated emitter-base structure provides high emitter efficiency
- Gold metallization with barrier realizes very stable characteristics and excellent lifetime
- Multicell geometry improves power sharing and reduces thermal resistance
- Internal input and output prematching networks allow an easier design of circuits.

APPLICATIONS

Intended for use in common base class C broadband pulsed power amplifiers for IFF, TCAS and Mode S applications in the 1030 MHz to 1090 MHz band. Also suitable for medium pulse, heavy duty operation within this band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT448A glued cap metal ceramic flange package, with base connected to flange.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common-base class C narrowband amplifier.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	t_p = 10 μs; δ = 1%	1.09	50	800	≥6	≥40

PINNING - SOT448A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

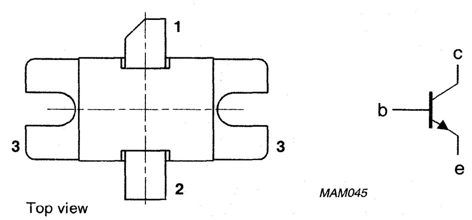


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

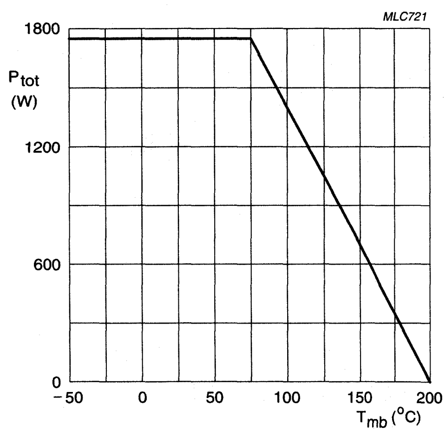
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_{CM}	peak collector current	$t_p = 10\ \mu s$; $\delta = 1\%$	–	50	A
P_{tot}	total power dissipation	$T_{mb} < 75\ °C$; $t_p \leq 10\ \mu s$; $\delta \leq 1\%$	–	1750	W
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 10\ \mu s$; $\delta = 1\%$.

Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_j = 120 °C	0.84	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.2	K/W
Z_{th}	thermal impedance from junction to heatsink	t_p = 10 μs; δ = 1%; notes 1and 2	0.01	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a"*.
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

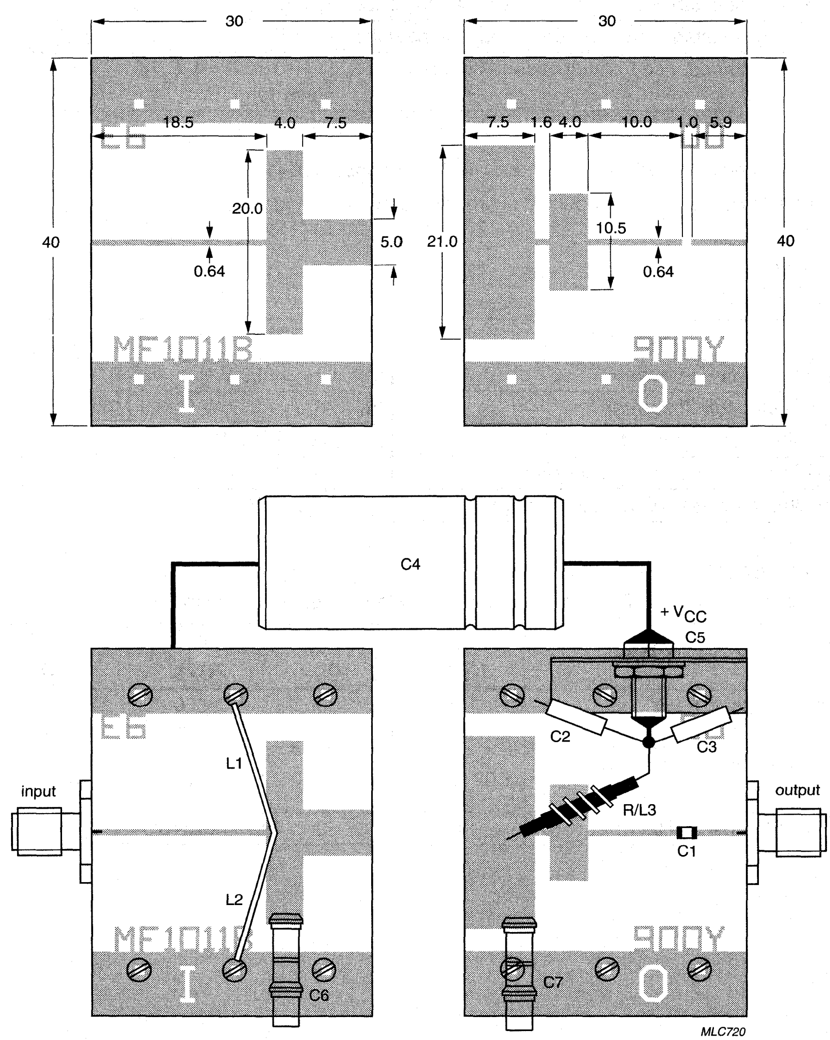
T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 50 V	27	mA
I_{CES}	collector cut-off current	V_{BE} = 0; V_{CE} = 50 V	27	mA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 1.5 V	7	mA
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 180 mA	65	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 180 mA; V_{BE} = 0	65	V

APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C in a common-base test circuit as shown in Fig.3.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	t_p = 10 μs; δ = 1%	1.09	50	≥800 typ. 900	≥6 typ. 6.5	≥40 typ. 48
	t_p = 0.5 μs; δ = 50% t_p = 112 μs; δ = 1%	1.03 to 1.09	50	typ. 750	typ. 5.7	typ. 36
	t_p = 32 μs; δ = 1%	1.09	50	typ. 870	typ. 6.3	typ. 46

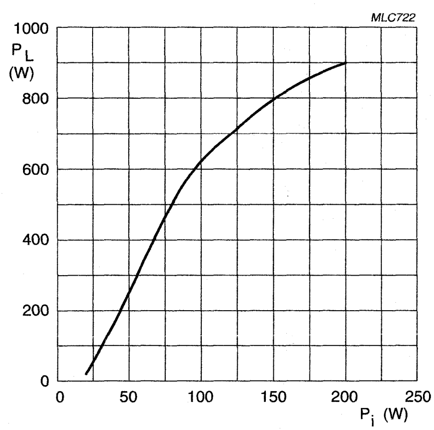


Dimensions in mm.
Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Broadband test circuit.

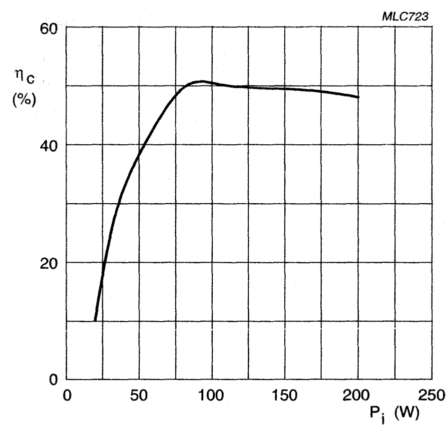
List of components (see Fig.3)

COMPONENT	DESCRIPTION	VALUE	ORDERING INFORMATION
C1	capacitor	100 pF	ATC 100A101kp50x
C2,C3	tantalum capacitor	10 μF; 50 V	
C4	electrolytic capacitor	1 mF; 63 V	
C5	feedthrough bypass capacitor		Erie 1250-003
C6, C7	variable gigatrim capacitor	0.8 to 8 pF	Tekelec 729-1
L1, L2	0.65 mm copper wire; total length = 26 mm; height of loop = 10 mm		
L3	4 turns 0.65 mm copper wire; total length = 48 mm		
R	resistor	4.7 Ω; 0.5 W	



Class C pulse operation.
$t_p = 10\ \mu s$; $\delta = 1\%$; $V_{CC} = 50$ V; f = 1.09 GHz.
In broadband test circuit as shown in Fig.3.

Fig.4 Load power as a function of input power.



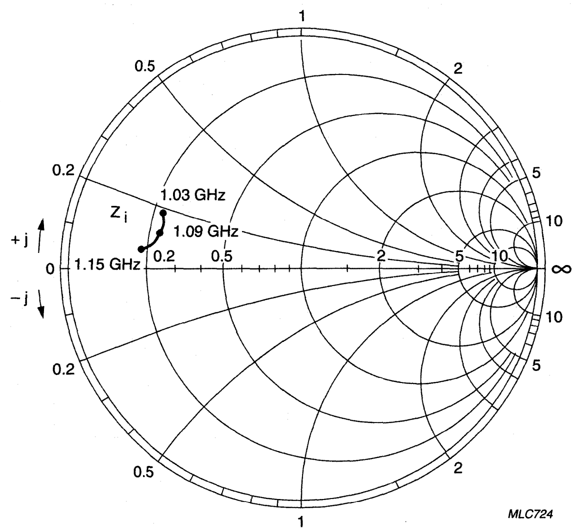
Class C pulse operation.
$t_p = 10\ \mu s$; $\delta = 1\%$; $V_{CC} = 50$ V; f = 1.09 GHz.
In broadband test circuit as shown in Fig.3.

Fig.5 Collector efficiency as a function of input power.

Input and optimum load impedances

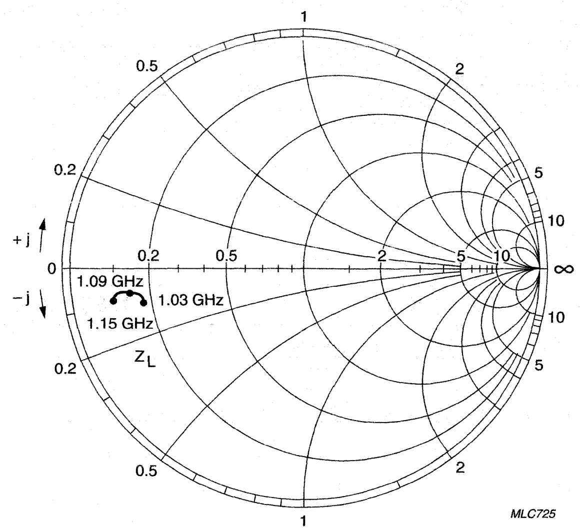
V_{CE} = 50 V; typical values at $P_L = P_{L1}$ (see Figs 6 and 7).

f (GHz)	Z_i (Ω)	Z_L (Ω)
1.03	0.22 + j0.19	0.14 – j0.10
1.09	0.23 + j0.12	0.12 – j0.08
1.15	0.19 + j0.06	0.09 – j0.09



V_{CC} = 50 V; Z_o = 10 Ω; P_o = 240 W.

Fig.6 Input impedance as a function of frequency.



V_{CC} = 50 V; Z_o = 50 Ω; P_o = 240 W.

Fig.7 Optimum load impedance as a function of frequency.

NPN microwave power transistor | MTB10010U

FEATURES

- Input prematching cell allows an easier design of circuits
- Diffused emitter ballasting resistors providing excellent current sharing and withstanding a high VSWR
- Interdigitated structure provides high emitter efficiency
- Gold metallization realizes very good characteristics stability and excellent lifetime
- Multicell geometry gives good balance of dissipated power and low thermal resistance.

APPLICATIONS

Common base class C narrowband pulsed power amplifiers at 1 030 MHz for IFF applications.

DESCRIPTION

NPN silicon planar epitaxial microwave transistor with internal input prematching cell in a SOT440A metal ceramic package with base connected to flange.

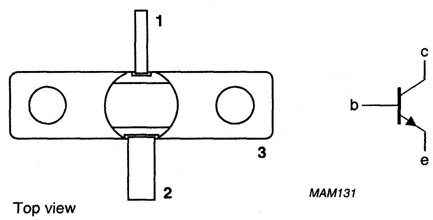
QUICK REFERENCE DATA

Microwave performance for T_{mb} = 25 °C in a common base class C narrowband amplifier.

MODE OF OPERATION	CONDITIONS	f (MHz)	V_{CC} (V)	P_L (W)	G_{PO} (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C	t_p = 1 μs; δ = 1%	1 030	24	>9.5	>9.5	>50	see Figs 5 and 6

PINNING - SOT440A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange



Marking code: 10010U.

Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

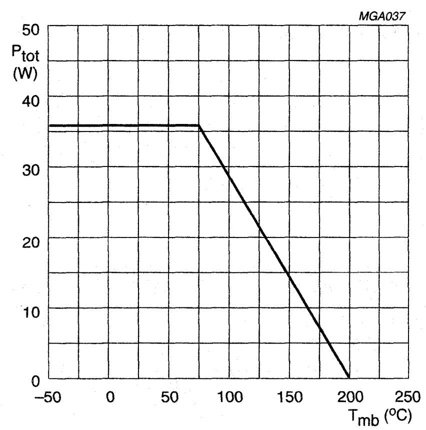
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (average)		–	0.75	A
P_{tot}	total power dissipation	$T_{mb} < 75$ °C; $t_p = 1\ \mu s$; $\delta = 1\%$	–	36	W
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

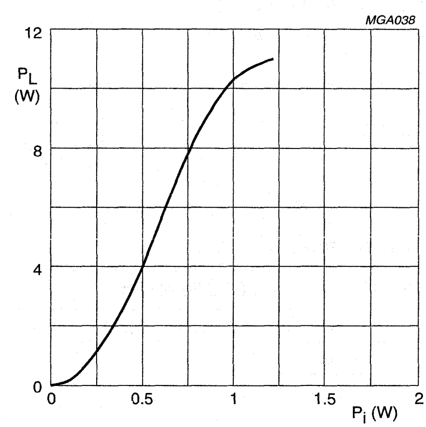
Note

1. Up to 0.3 mm from ceramic.



$P_{tot\ max}$ = 36 W under the nominal pulse conditions.

Fig.2 Power derating curve.



$V_{CC} = 24$ V; $t_p = 1\ \mu s$; $\delta = 1\%$; f = 1 030 MHz.

Fig.3 Load power as a function of input power.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_j = 100 °C	10.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.7	K/W
$Z_{th\ j\text{-}mb}$	thermal impedance from junction to mounting base	t_p = 1 μs; δ = 1%; note 1	2.5	K/W

Note

1. See *"Mounting recommendations in the General part of handbook SC19a"*.

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 30 V; I_E = 0	45	μA
I_{CES}	collector cut-off current	V_{CE} = 30 V; R_{BE} = 0	300	μA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	4.5	μA

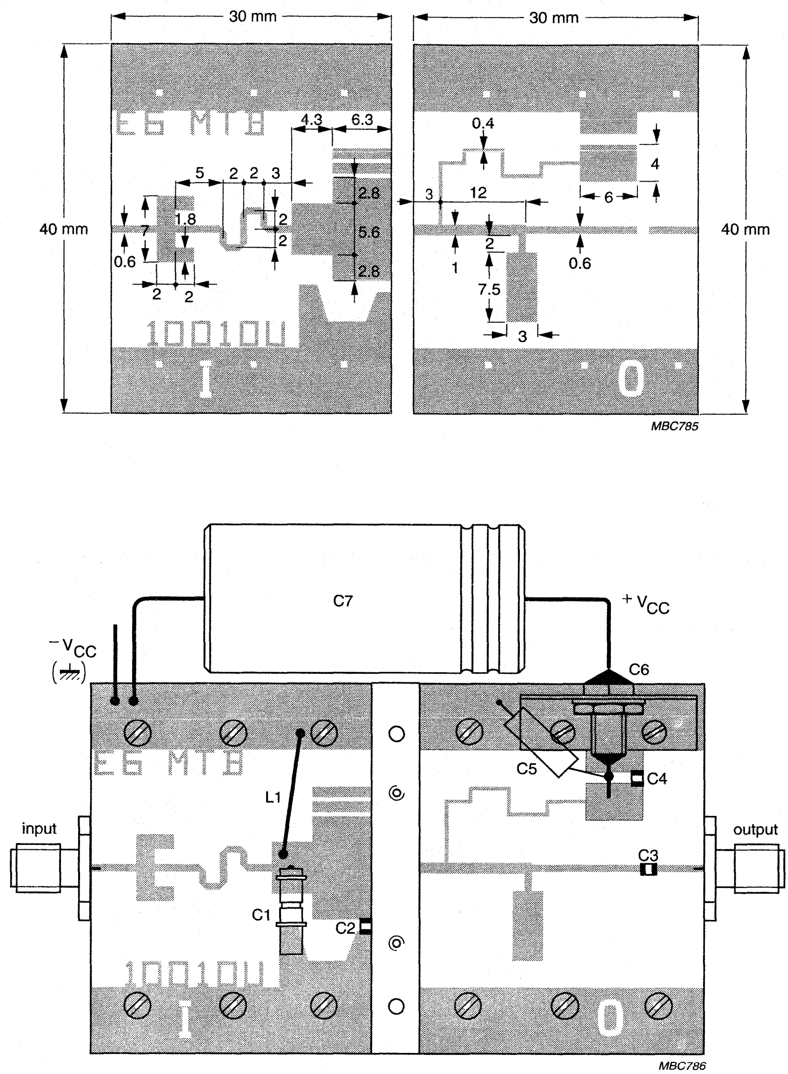
APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C and working in pulsed conditions in a narrowband test circuit as shown in Fig.4.

MODE OF OPERATION	CONDITIONS	f (MHz)	V_{CC} (V)	P_L (W)	G_{po} (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C	t_p = 1 μs; δ = 1 %	1030	24	>9.5; typ. 11	>9.5; typ. 10	>50; typ. 55	see Figs 5 and 6

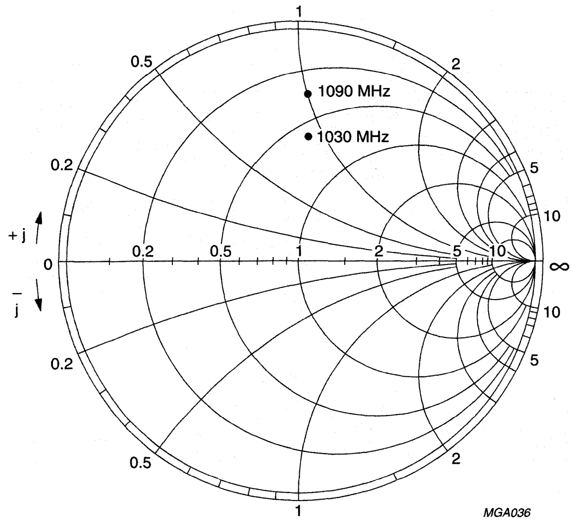
List of components (see Fig.4)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1	0.4 mm diameter copper wire	–	rectangular loop	–
C1	tuning capacitor	0.5 – 5 pF	–	Tekelec 5855
C2	chip capacitor	3 pF	–	Eurofarad CEC 23
C3	chip capacitor	10 pF	–	Eurofarad CEC 23
C4	chip capacitor	47 pF	–	Eurofarad CEC 23
C5	tantalum capacitor	10 μF, 50 V	–	–
C6	feedthrough bypass capacitor	–	–	Erie 1250-003
C7	capacitor	220 μF, 63 V	–	–



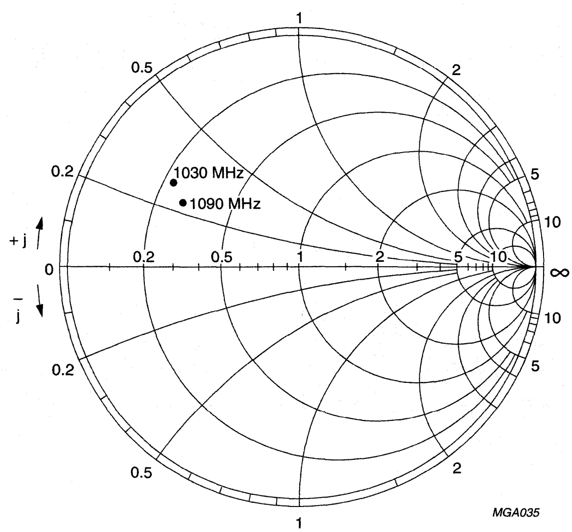
Dimensions in mm.
Substrate: Duroid 6010.
Permittivity: ε_r = 10.2.

Fig.4 Narrowband test circuit.



V_{CC} = 24 V; Z_O = 5 Ω; P_L = 10 W.

Fig.5 Input impedance as a function of frequency, associated with optimum load impedance.



V_{CC} = 24 V; Z_O = 50 Ω; P_L = 10 W.

Fig.6 Optimum load impedance as a function of frequency; associated with input impedance.

NPN microwave power transistors — MX0912B100Y; MZ0912B100Y

FEATURES

- Interdigitated structure provides high emitter efficiency
- Diffused emitter ballasting resistors providing excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry improves power sharing and low thermal resistance
- Input and output matching cell allows an easier design of circuits.

APPLICATIONS

- Common base class-C broadband pulse power amplifiers operating at 960 to 1215 MHz for TACAN application.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistors.

The MX0912B100Y has a SOT439A metal ceramic flange package and improved output prematching cells. It is recommended for new designs.

The MZ0912B100Y has a SOT443A metal ceramic flange package with the base connected to the flange. It is mounted in common base configuration and specified in class C.

PINNING

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

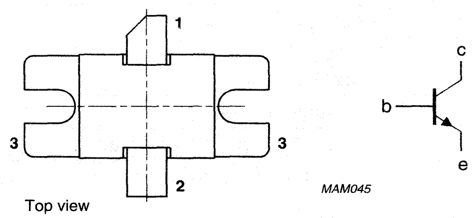


Fig.1 Simplified outline and symbol (SOT439A).

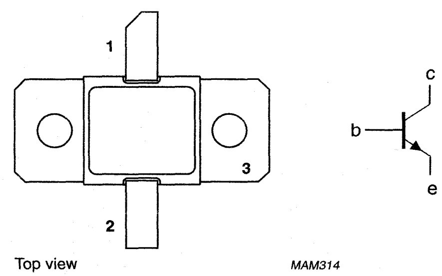


Fig.2 Simplified outline and symbol (SOT443A).

QUICK REFERENCE DATA

Microwave performance at $T_{mb} \leq 25$ °C in a common base class-C broadband amplifier.

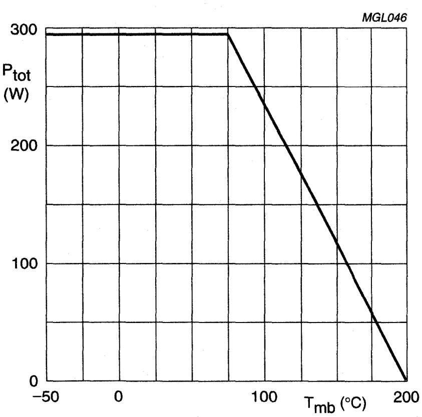
MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_P (dB)	η_C (%)	Z_i; Z_L (Ω)
Class-C; t_p = 10 μs; δ = 10 %	0.960 to 1.215	50	>100	>7	>42	see Figs 8 and 9

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)	$t_p \leq 10\ \mu s$; $\delta \leq 10$ %	–	6	A
P_{tot}	total power dissipation (peak power)	$t_p \leq 10\ \mu s$; $\delta \leq 10$ %; $T_{mb} = 75$ °C	–	290	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	up to 0.2 mm from ceramic; $t \leq 10$ s	–	235	°C



$t_p = 10\ \mu s$; $\delta = 10$ %; $P_{tot\ max} = 290$ W.

Fig.3 Maximum power dissipation derating as a function of mounting-base temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	T_j = 125 °C	3.2	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	T_j = 125 °C; note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	t_p = 10 µs; δ = 10 %; T_j = 125 °C; notes 1 and 2	0.43	K/W

Notes

1. See "*Mounting recommendations in the General part of handbook SC19a*".
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 65 V; I_E = 0	40	mA
		V_{CB} = 50 V; I_E = 0	4	mA
I_{CES}	collector cut-off current	V_{CB} = 60 V; R_{BE} = 0	40	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	400	µA

APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C measured in the test jig as shown in Fig.7 and working in class C broadband in pulse mode; note 1.

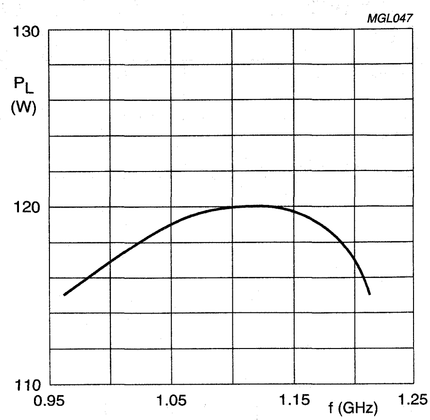
MODE OF OPERATION	f (GHz)	V_{CC} (V)(2)	P_L (W)	G_p (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C; t_p = 10 µs; δ = 10%	0.960 to 1.215	50	≥100 typ. 115	≥7 typ. 7.6	≥42 typ. 44	see Figs 8 and 9
t_p = 300 µs; δ = 10%; see Fig.6	1.03 to 1.09	50	typ. 125	typ. 8	typ. 50	

Notes

1. Operating conditions and performance for other pulse formats can be made available on request.
2. V_{CC} during pulse.

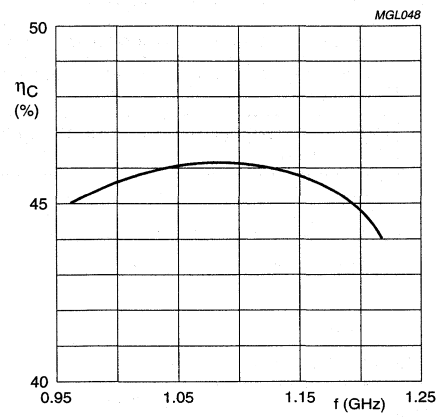
NPN microwave power transistors

MX0912B100Y; MZ0912B100Y



V_{CC} = 50 V; t_p = 10 μs; δ = 10%.

Fig.4 Load power as a function of frequency. (In broadband test circuit as shown in Fig.7)



V_{CC} = 50 V; t_p = 10 μs; δ = 10%.

Fig.5 Collector efficiency as a function of frequency. (In broadband test circuit as shown in Fig.7)

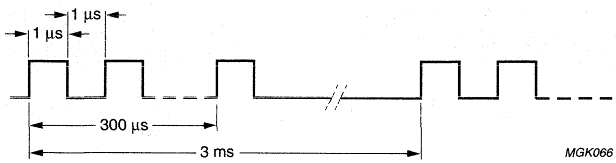
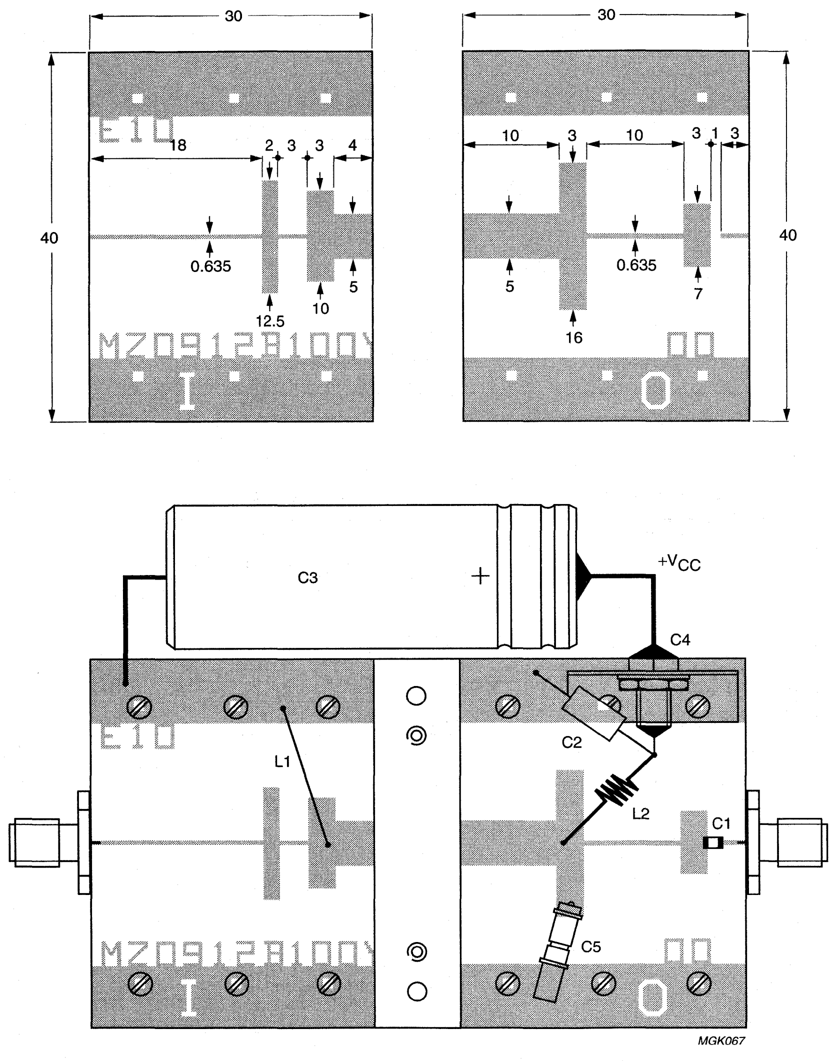


Fig.6 Pulse definition.

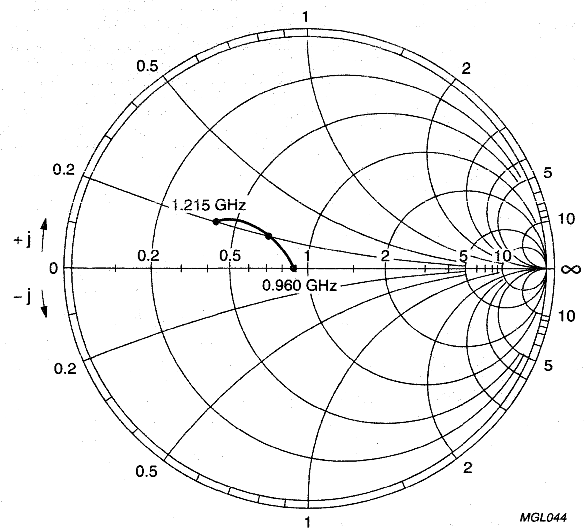
List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1	0.65 mm diameter copper wire	–	total length = 12 mm; height of loop = 12 mm	–
L2	4 turns 0.65 mm diameter copper wire	–	int. dia. 3 mm; L = 5 mm	–
C1	capacitor	100 pF	–	ATC, ref. 100A101KP50X
C2	tantalum capacitor	10 μF; 50 V	–	–
C3	electrolytic capacitor	470 μF; 63 V	–	–
C4	feedthrough bypass capacitor	–	–	Erie, ref. 1250-003
C5, C6	variable gigatrim capacitor	0.6 to 4.5 pF	–	Tekelec, ref. 727.1



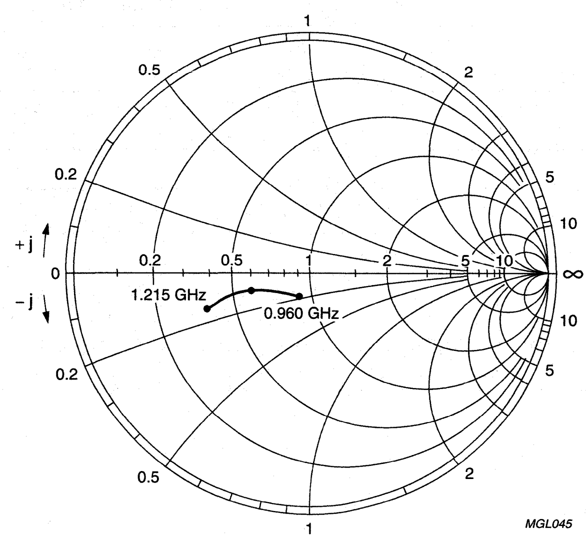
Dimensions in mm.
Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.7 Broadband test circuit.



V_{CC} = 50 V; Z_o = 10 Ω; P_L = 100 W.

Fig.8 Input impedance as a function of frequency associated with optimum load impedance.



V_{CC} = 50 V; Z_o = 10 Ω.; P_L = 100 W.

Fig.9 Optimum load impedance as a function of frequency associated with input impedance.

NPN microwave power transistor | MX0912B251Y

FEATURES

- Interdigitated structure; high emitter efficiency
- Diffused emitter ballasting resistors providing excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry gives good balance of dissipated power and low thermal resistance
- Input and output matching cell allows an easier design of circuits.

APPLICATIONS

Intended for use in common base class C broadband pulse power amplifier from 960 to 1215 MHz for TACAN application.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package, with base connected to flange. It is mounted in common base configuration, and specified in class C.

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

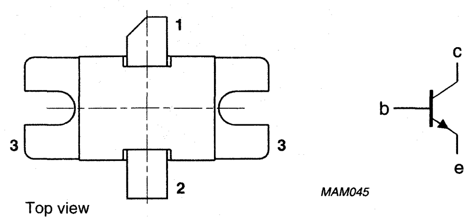


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class C broadband amplifier.

MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_{po} (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C t_p = 10 μs; δ = 10%	0.960 to 1.215	50	>235	>7	>42	see Figs 7 and 8

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

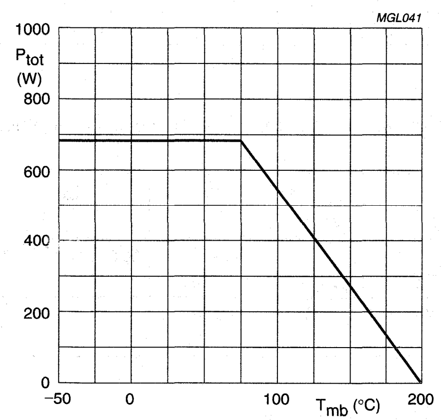
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current	$t_p \leq 10\ \mu s$; $\delta \leq 10\%$	–	15	A
P_{tot}	total power dissipation (peak power)	$T_{mb} = 75\ °C$; $t_p \leq 10\ \mu s$; $\delta \leq 10\%$	–	690	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 10\ \mu s$; $\delta = 10\%$; $P_{tot\ max} = 690$ W.

Fig.2 Maximum power dissipation derating as a function of mounting base temperature.

THERMAL CHARACTERISTICS

T_j = 125 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	CW	1.9	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	CW; note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	t_p = 10 μs; δ = 10% notes 1 and 2	0.28	K/W

Notes

1. See "*Mounting recommendations in the General part of handbook SC19a*".
2. Equivalent thermal impedance under nominal pulse microwave operating conditions.

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 65 V; I_E = 0	100	mA
		V_{CB} = 50 V; I_E = 0	10	mA
I_{CES}	collector cut-off current	V_{CE} = 60 V; R_{BE} = 0	100	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	1	mA

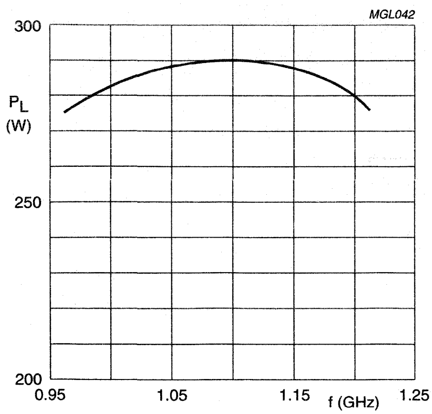
APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C measured in the test jig as shown in Fig.6 and working in class C broadband mode in pulse; note 1.

MODE OF OPERATION	f (GHz)	V_{CC} (V)(2)	P_L (W)	G_{po} (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C; t_p = 10 μs; δ = 10%	0.960 to 1.215	50	>235 typ. 275	>7 typ. 7.4	>42 typ. 47	see Figs 7 and 8
t_p = 300 μs; δ = 10%; see Fig.5	1.03 to 1.09	50	typ. 280	typ. 8	typ. 48	

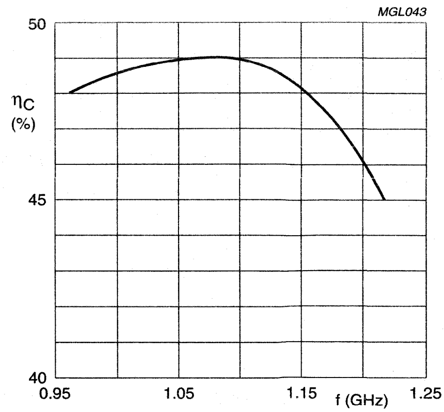
Notes

1. Operating conditions and performance for other pulse formats can be made available on request.
2. V_{CC} during pulse.



V_{CC} = 50 V; t_p = 10 µs; δ = 10%.

Fig.3 Load power as a function of frequency. (In broadband test circuit as shown in Fig.6)



V_{CC} = 50 V; t_p = 10 µs; δ = 10%.

Fig.4 Collector efficiency as a function of frequency. (In broadband test circuit as shown in Fig.6)

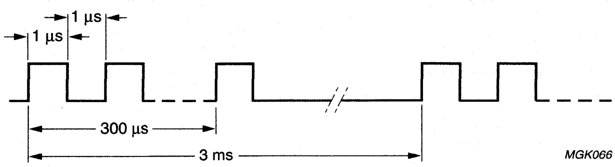


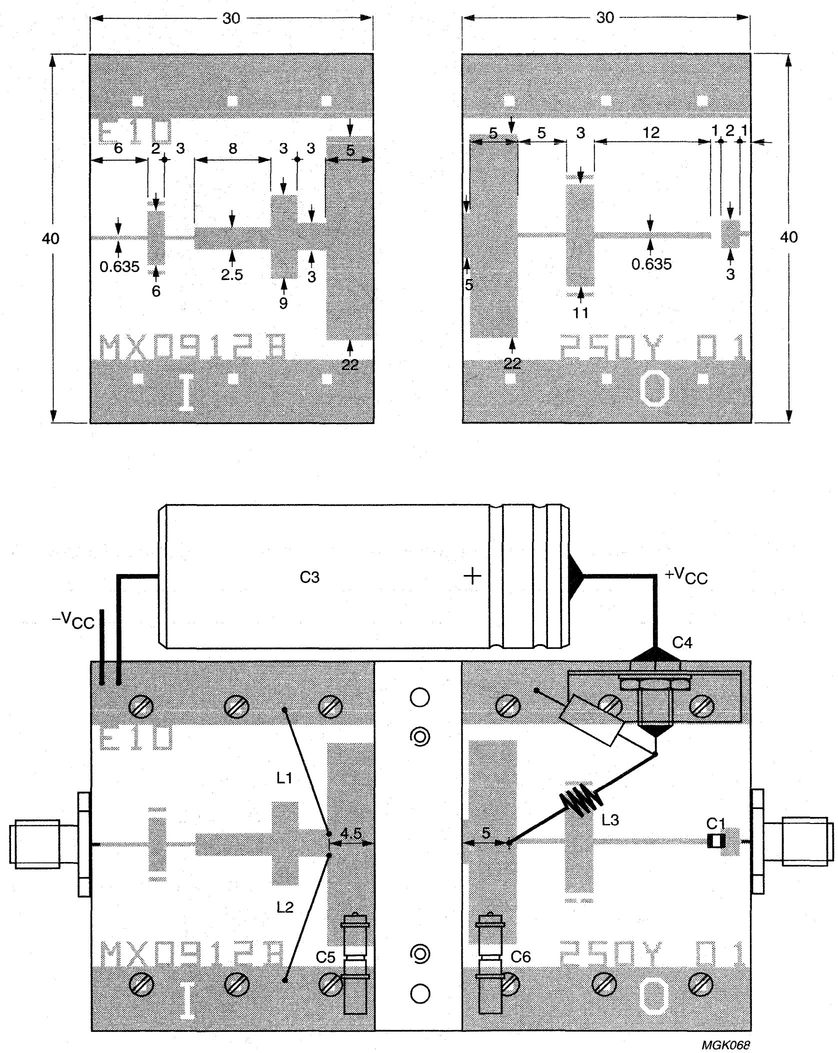
Fig.5 Pulse definition.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1, L2	0.65 mm diameter copper wire	–	total length = 12 mm; height of loop = 9 mm	–
L3	4 turns 0.65 mm diameter copper wire	–	int. diameter 3 mm; L = 5 mm	–
C1	DC block	100 pF		ATC, ref. 100A101KP50X
C2	tantalum capacitor	10 μF; 50 V		
C3	electrolytic capacitor	470 μF; 63 V		
C4	feedthrough bypass capacitor			Erie, ref. 1250-003
C5, C6	variable gigatrim capacitor	0.8 to 8 pF		Tekelec, ref. 729.1

NPN microwave power transistor

MX0912B251Y



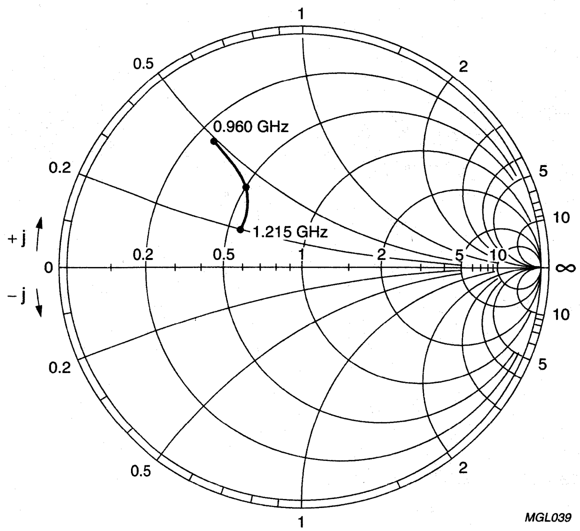
Dimensions in mm.

Substrate: Epsilam 10.

Thickness: 0.635 mm.

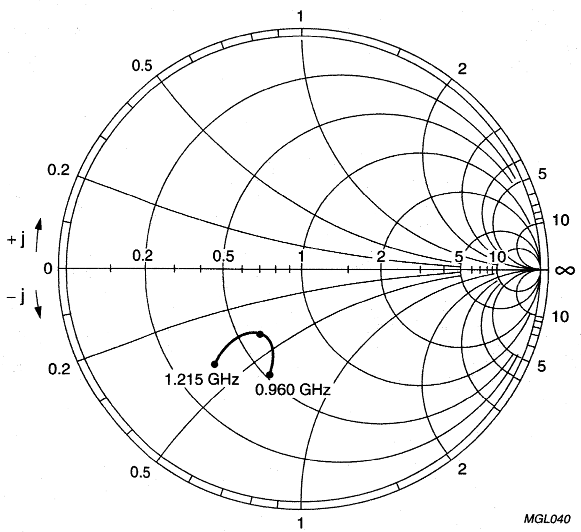
Permittivity: $\varepsilon_r = 10$.

Fig.6 Broadband test circuit.



V_{CC} = 50 V; Z_o = 5 Ω; P_L = 235 W.

Fig.7 Input impedance as a function of frequency associated with optimum load impedance.



V_{CC} = 50 V; Z_o = 5 Ω; P_L = 235 W.

Fig.8 Optimum load impedance as a function of frequency associated with input impedance.

NPN microwave power transistor MX0912B351Y

FEATURES

- Interdigitated structure; high emitter efficiency
- Diffused emitter ballasting resistors providing excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry gives good balance of dissipated power and low thermal resistance
- Input and output matching cell allows an easier design of circuits.

APPLICATIONS

Intended for use in common base class C broadband pulse power amplifier from 960 to 1215 MHz for TACAN application.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package, with base connected to flange. It is mounted in common base configuration and specified in class C.

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

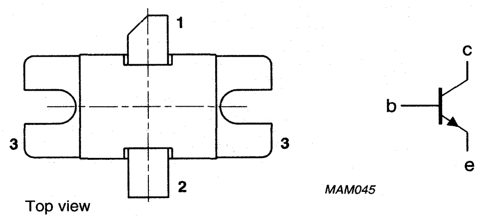


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class C broadband amplifier.

MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_{po} (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C t_p = 10 μs; δ = 10%	0.960 to 1.215	50	>325	>7	>40	see Figs 7 and 8

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

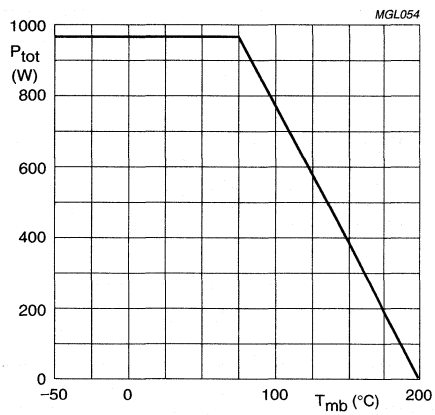
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current	$t_p \leq 10\ \mu s$; $\delta \leq 10\%$	–	21	A
P_{tot}	total power dissipation (peak power)	$T_{mb} = 75\ °C$; $t_p \leq 10\ \mu s$; $\delta \leq 10\%$	–	960	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 10\ \mu s$; $\delta = 10\%$; $P_{tot\ max} = 960$ W.

Fig.2 Maximum power dissipation derating as a function of mounting base temperature.

THERMAL CHARACTERISTICS

T_j = 125 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	CW	1.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	CW; note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	t_p = 10 μs; δ = 10% notes 1 and 2	0.13	K/W

Notes

1. See "*Mounting recommendations in the General part of handbook SC19a*".
2. Equivalent thermal impedance under nominal pulse microwave operating conditions.

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 65 V; I_E = 0	140	mA
		V_{CB} = 50 V; I_E = 0	14	mA
I_{CES}	collector cut-off current	V_{CE} = 60 V; R_{BE} = 0 Ω	140	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	1.4	mA

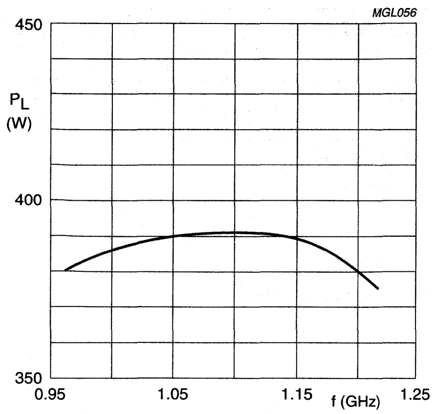
APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C measured in the test circuit as shown in Fig.6 and working in class C broadband in pulse mode; note 1.

MODE OF OPERATION	f (GHz)	V_{CC} (V)[(2)]	P_L (W)	G_{po} (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C; t_p = 10 μs; δ = 10%	0.960 to 1.215	50	>325 typ. 375	>7 typ. 7.6	>40 typ. 47	see Figs 7 and 8
t_p = 300 μs; δ = 10%; see Fig.5	1.03 to 1.09	50	typ. 350	typ. 8	typ. 48	

Notes

1. Operating conditions and performance for other pulse formats can be made available on request.
2. V_{CC} during pulse.



V_{CC} = 50 V; t_p = 10 µs; δ = 10%.

Fig.3 Load power as a function of frequency. (In broadband test circuit as shown in Fig.6)

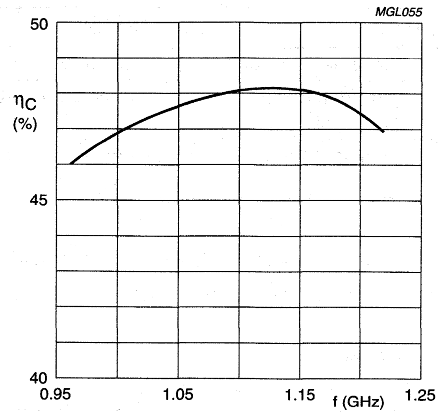


Fig.4 Collector efficiency as a function of frequency. (In broadband test circuit as shown in Fig.6)

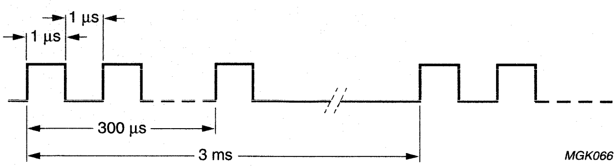
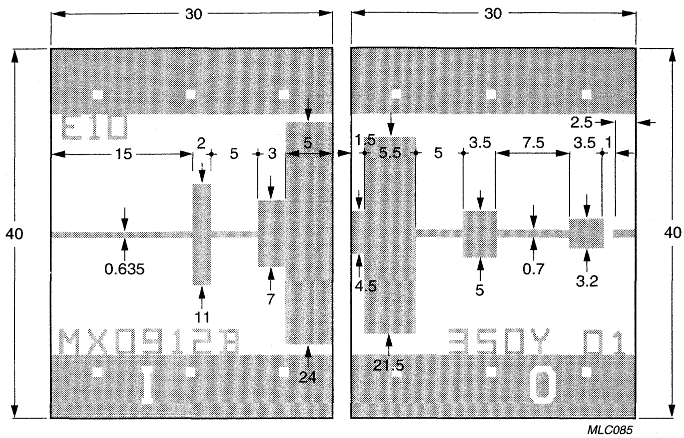
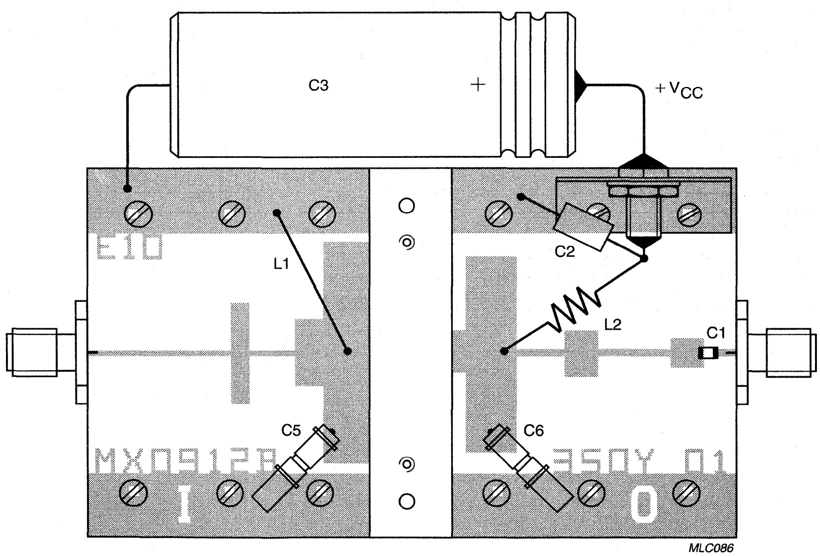


Fig.5 Pulse definition.

List of components

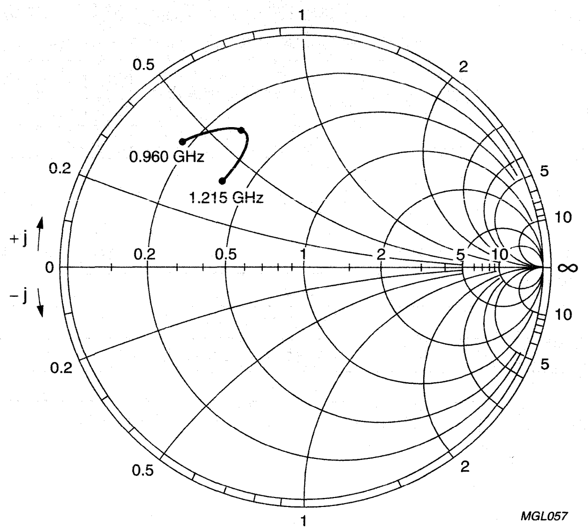
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1	0.65 mm diameter copper wire	–	total length = 12 mm; height of loop = 9 mm	–
L2	4 turns 0.65 mm diameter copper wire	–	int. diameter. 3 mm; L = 5 mm	–
C1	DC block	100 pF		ATC, ref. 100A101KP50X
C2	tantalum capacitor	10 µF; 50 V		
C3	electrolytic capacitor	470 µF; 63 V		
C4	feedthrough bypass capacitor			Erie, ref. 1250-003
C5, C6	variable gigatrim capacitor	0.8 to 8 pF		Tekelec, ref. 729.1





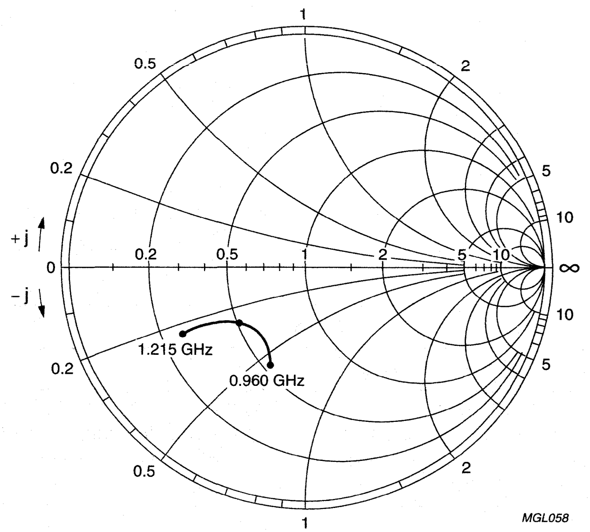
Dimensions in mm.
Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.6 Broadband test circuit.



V_{CC} = 50 V; Z_o = 5 Ω; P_L = 325 W.

Fig.7 Input impedance as a function of frequency associated with optimum load impedance.



V_{CC} = 50 V; Z_o = 5 Ω; P_L = 325 W.

Fig.8 Optimum load impedance as a function of frequency associated with input impedance.

Microwave power transistor MX1011B200Y

FEATURES

- Suitable for short and medium pulse applications up to 100 µs pulse width, 10% duty factor
- Diffused emitter ballasting resistors improve ruggedness
- Interdigitated emitter-base structure provides high emitter efficiency
- Gold metallization with barrier realizes very stable characteristics and excellent lifetime
- Multicell geometry improves power sharing reduces thermal resistance
- Internal input and output prematching networks allow an easier design of circuits.

APPLICATIONS

Intended for use in common base class C broadband pulsed power amplifiers for IFF, TCAS and Mode S applications in the 1030 MHz to 1090 MHz bandwidth. Also suitable for medium pulse, heavy duty operation within the 1030 MHz to 1150 MHz bandwidth.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package, with base connected to flange.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class C narrowband amplifier.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	t_p = 10 µs; δ = 1%	1.09	50	200	≥7.5	≥45

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

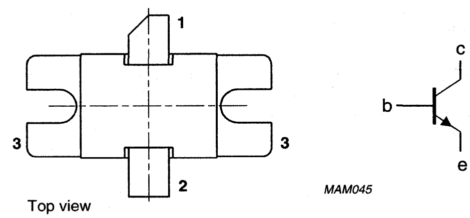


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

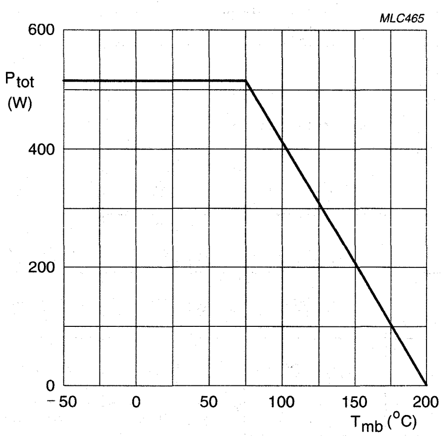
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_{CM}	peak collector current	$t_p = 10\ \mu s$; $\delta = 1\%$	–	11.5	A
P_{tot}	total power dissipation	$T_{mb} < 75\ °C$; $t_p \leq 10\ \mu s$; $\delta \leq 1\%$	–	515	W
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 10\ \mu s$; $\delta = 1\%$.

Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_j = 120 °C	2.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.2	K/W
Z_{th}	thermal impedance from junction to heatsink	t_p = 10 μs; δ = 1%; notes 1 and 2	0.16	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a"*.
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

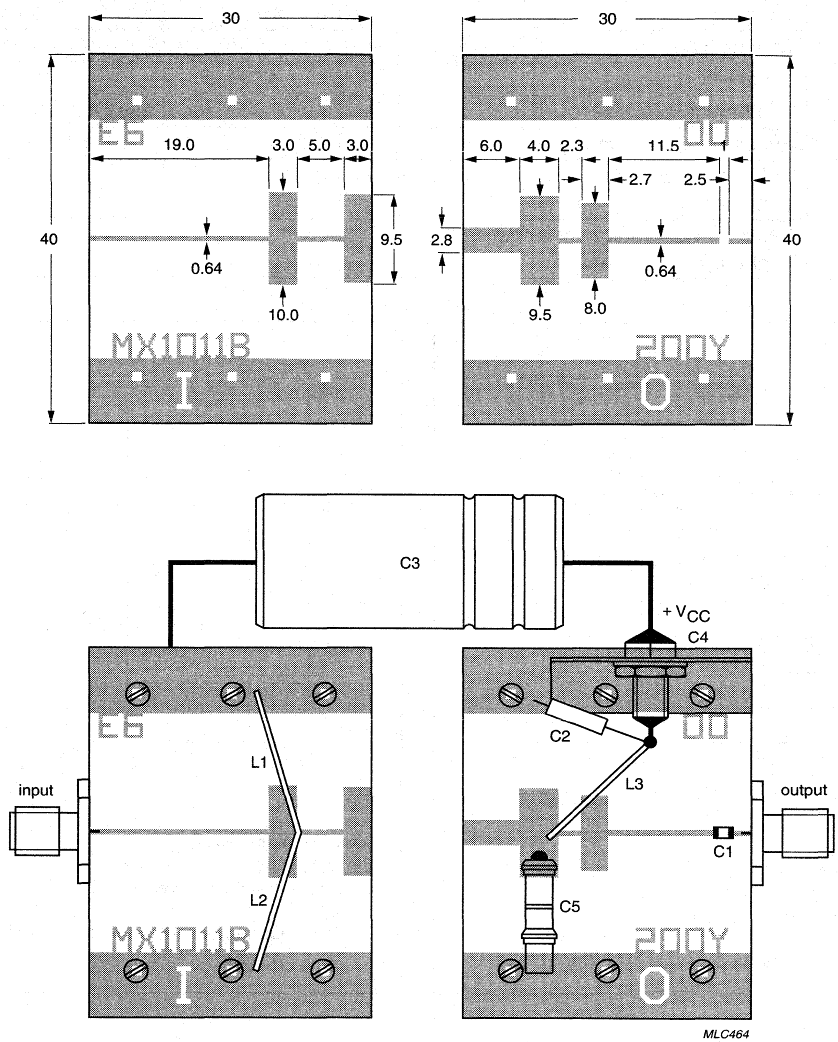
T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 50 V	6	mA
I_{CES}	collector cut-off current	V_{BE} = 0; V_{CE} = 50 V	6	mA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 1.5 V	1.5	mA
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 40 mA	65	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 40 mA; V_{BE} = 0	65	V

APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C in a common-base test circuit as shown in Fig.3.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	t_p = 10 μs; δ = 1%	1.09	50	≥200 typ. 220	≥7.5 typ. 8.3	≥45 typ. 52
	t_p = 0.5 μs; δ = 50% t_p = 112 μs; δ = 1%	1.03 to 1.09	50	typ. 220	typ. 7.5	typ. 50
	t_p = 6.6 μs; δ = 51% t_p = 3.3 μs; δ = 43%	1.03 to 1.15	50	typ. 100	typ. 6	typ. 35
	t_p = 32 μs; δ = 1%	1.09	50	typ. 210	typ. 7.5	typ. 47

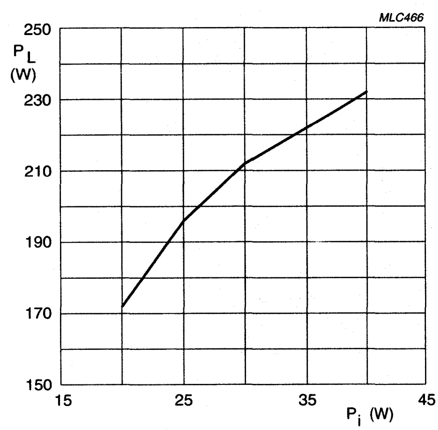


Dimensions in mm.
Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Broadband test circuit.

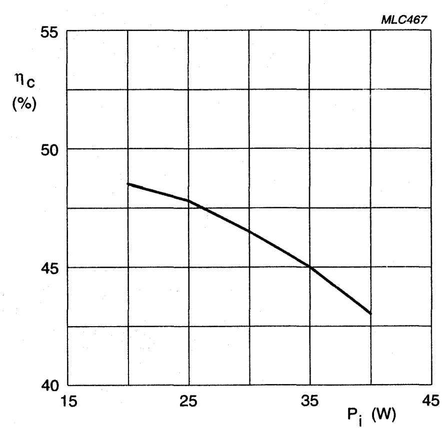
List of components (see Fig.3)

COMPONENT	DESCRIPTION	VALUE	ORDERING INFORMATION
C1	capacitor	100 pF	ATC 100A101kp50x
C2	tantalum capacitor	10 μF; 50 V	–
C3	electrolytic capacitor	63 V; 1000 μF	–
C4	feedthrough bypass capacitor	–	Erie1250-003
C5	variable gigatrim capacitor	0.8 to 8 pF	Tekelec 729-1
L1, L2	0.65 mm copper wire; total length = 26 mm; height of loop = 10 mm	–	–
L3	0.85 mm silver wire; total length = 30 mm; height of loop = 15 mm	–	–



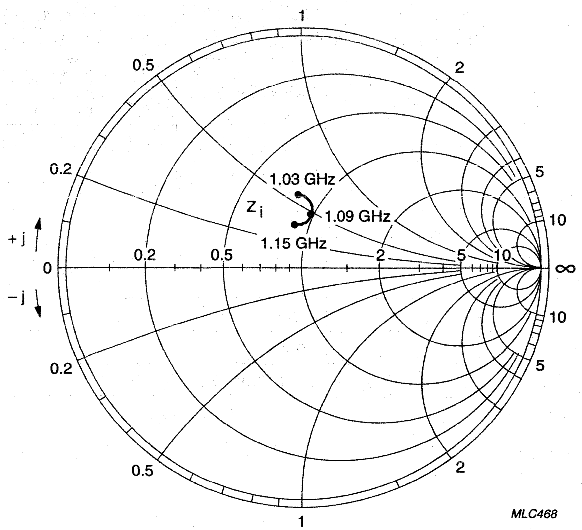
Class C pulse operation.
t_p = 10 μs; δ = 1%; V_{CC} = 50 V; f = 1.09 GHz.
In broadband test circuit as shown in Fig.3.

Fig.4 Load power as a function of input power.



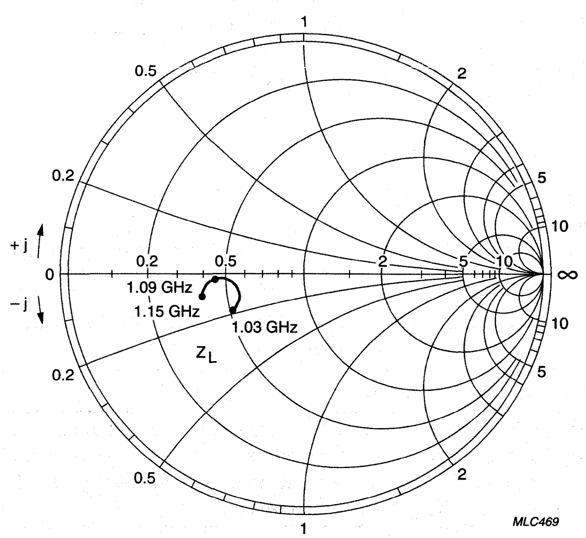
Class C pulse operation.
t_p = 10 μs; δ = 1%; V_{CC} = 50 V; f = 1.09 GHz.
In broadband test circuit as shown in Fig.3.

Fig.5 Collector efficiency as a function of input power.



V_{CC} = 50 V; Z_o = 10 Ω; P_o = 240 W.

Fig.6 Input impedance as a function of frequency.



V_{CC} = 50 V; Z_o = 50 Ω; P_o = 240 W.

Fig.7 Optimum load impedance as a function of frequency.

NPN microwave power transistor MX1011B700Y

FEATURES

- Suitable for short and medium pulse applications up to 100 μs/10%
- Internal input and output prematching networks allow an easier design of circuits
- Diffused emitter ballasting resistors improve ruggedness
- Interdigitated emitter-base structure provides high emitter efficiency
- Gold metallization with barrier realizes very good stability of the characteristics and excellent lifetime
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

Intended for use in common base, class C, broadband, pulsed power amplifiers for IFF, TCAS and Mode S applications in the 1 030 to 1 090 MHz band. Also suitable for medium pulse, heavy duty operation within the 1 030 to 1 150 MHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package with base connected to flange.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class C broadband amplifier.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_P (dB)	η_C (%)
Class C	t_p = 10 μs; δ = 1%	1.09	50	650	≥6	≥48

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

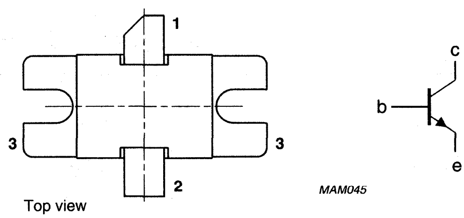


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

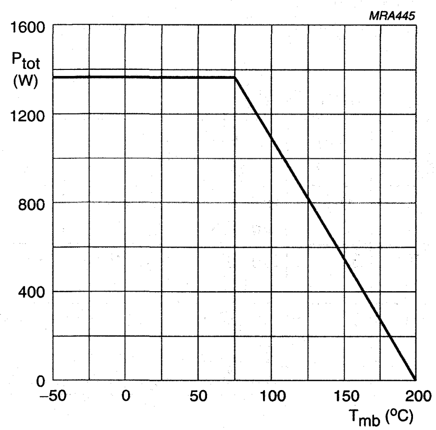
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	65	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_{CM}	peak collector current	$t_p \leq 10\ \mu s$; $\delta \leq 1\%$	–	40	A
P_{tot}	total power dissipation	$T_{mb} < 75\ °C$; $t_p \leq 10\ \mu s$; $\delta \leq 1\%$	–	1365	W
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 10\ \mu s$; $\delta = 1\%$; $P_{tot\ max} = 1365$ W.

Fig.2 Maximum power dissipation derating as a function of mounting base temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_j = 120\ °C$	1.12	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 10\ \mu s$; $\delta = 1\%$; notes 1 and 2	0.06	K/W

Notes

1. See "*Mounting recommendations in the General part of handbook SC19a*".
2. Equivalent thermal impedance under nominal pulse microwave operating conditions.

CHARACTERISTICS

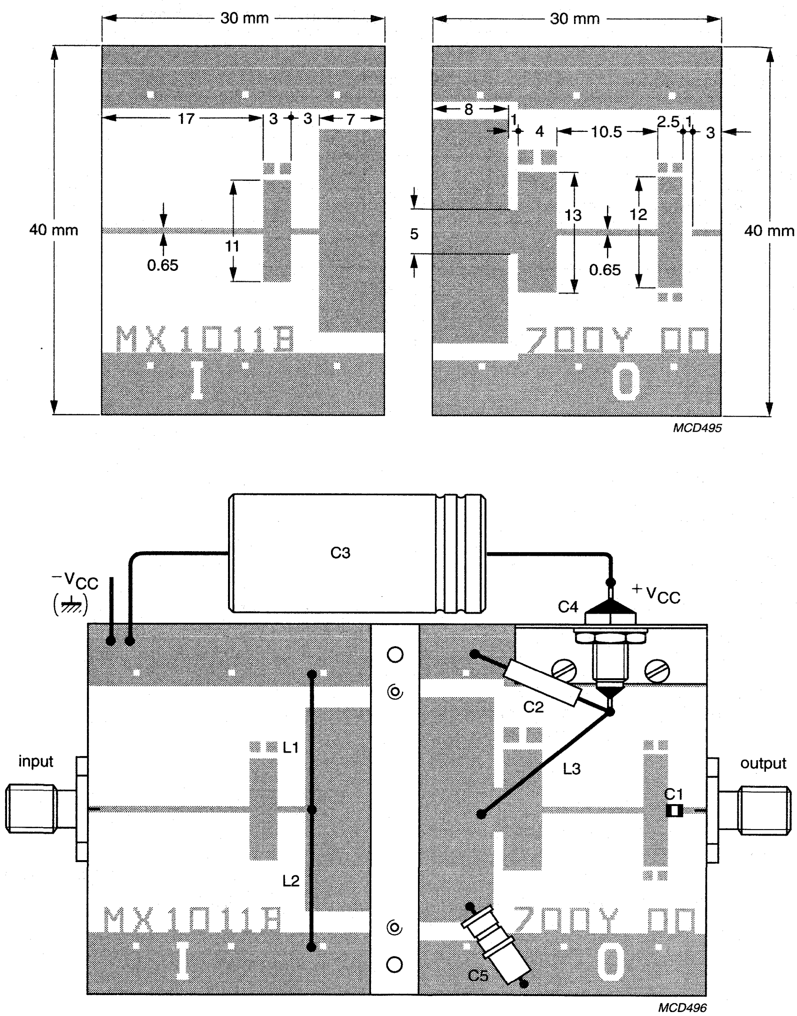
$T_{mb} = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	$V_{CB} = 50\ V$; $I_E = 0$	20	mA
I_{CES}	collector cut-off current	$V_{CE} = 50\ V$; $V_{BE} = 0$	20	mA
I_{EBO}	emitter cut-off current	$V_{EB} = 1.5\ V$; $I_C = 0$	5	mA
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 140\ mA$; $V_{BE} = 0$	65	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 140\ mA$; $V_{BE} = 0$	65	V

APPLICATION INFORMATION

Microwave performance up to $T_{mb} = 25\ °C$ in a broadband test circuit as shown in Fig.3.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_P (dB)	η_C (%)
Class C	$t_p = 10\ \mu s$; $\delta = 1\%$	1.09	50	650; typ. 740	≥6.0; typ. 7	≥48; typ. 55
	$t_p = 0.5\ \mu s$; $\delta = 50\%$; $t_p = 112\ \mu s$; $\delta = 1\%$	1.03 to 1.09	50	typ. 650	typ. 6.4	typ. 45
	$t_p = 6.6\ \mu s$; $\delta = 51\%$; $t_p = 3.3\ ms$; $\delta = 43\%$	1.03 to 1.15	50	typ. 300	typ. 7	typ. 45
	$t_p = 32\ \mu s$; $\delta = 1\%$	1.09	50	typ. 700	typ. 6.7	typ. 55

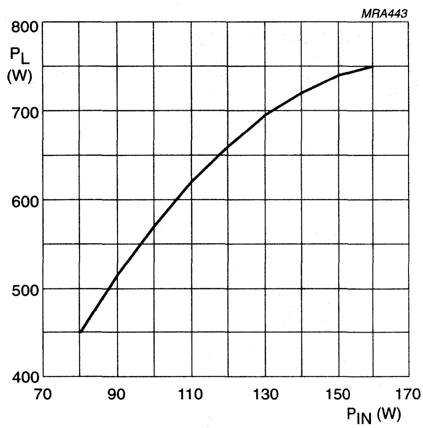


Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Broadband test circuit.

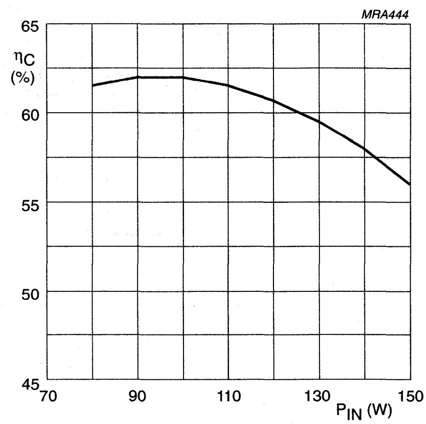
List of components (see Fig.3)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1, L2	0.65 mm diameter copper wire	–	total length = 26 mm; height of loop = 10 mm	–
L3	0.85 mm diameter silver wire	–	total length = 30 mm; height of loop = 15 mm	–
C1	capacitor	100 pF	–	ATC, ref.100A101KP50X
C2	tantalum capacitor	10 μF; 50 V	–	–
C3	electrolytic capacitor	1000 μF; 63 V	–	–
C4	feedthrough bypass capacitor		–	Erie, ref.1250-003
C5	variable gigatrim capacitor	0.8 – 8 pF	–	Tekelec, ref.729.1



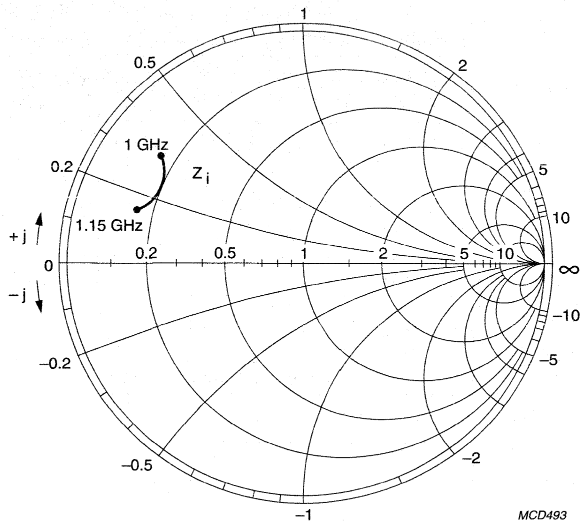
Class C pulse operation; t_p = 10 μs; δ = 1%; V_{CC} = 50 V;
f = 1.09 GHz; (In broadband test circuit as shown in Fig.3).

Fig.4 Load power as a function of input power.



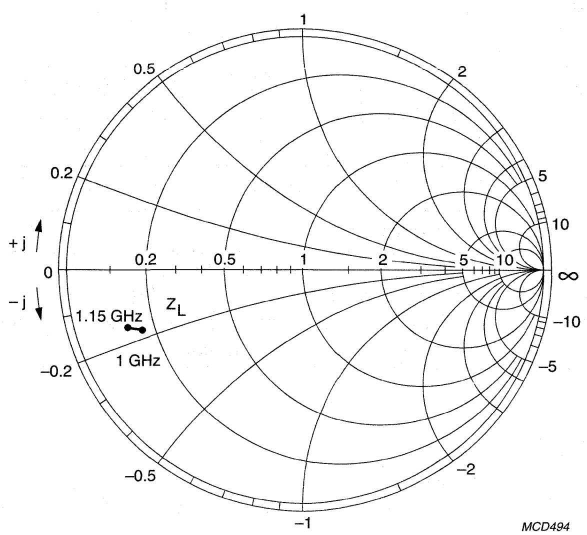
Class C pulse operation; t_p = 10 μs; δ = 1%; V_{CC} = 50 V;
f = 1.09 GHz; (In broadband test circuit as shown in Fig.3).

Fig.5 Collector efficiency as a function of input power.



V_{CC} = 50 V; Z_O = 10 Ω; P_o = 740 W.

Fig.6 Input impedance as a function of frequency, associated with optimum load impedance.



V_{CC} = 50 V; Z_O = 10 Ω; P_o = 740 W.

Fig.7 Optimum load impedance as a function of frequency; associated with input impedance.

NPN microwave power transistor

MZ0912B50Y

FEATURES

- Interdigitated structure provides high emitter efficiency
- Diffused emitter ballasting resistors providing excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry gives good balance of dissipated power and low thermal resistance
- Input and output matching cell allows an easier design of circuits.

APPLICATIONS

Common base, class C, broadband, pulse power amplifier from 960 to 1215 MHz for TACAN application.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT443A metal ceramic flange package with base connected to flange. It is mounted in common base configuration, and specified in class C.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class C broadband amplifier.

MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C; t_p = 10 μs; δ = 1%	0.960 to 1.215	50	>50	>7	>42	see Figs 6 and 7

PINNING - SOT443A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

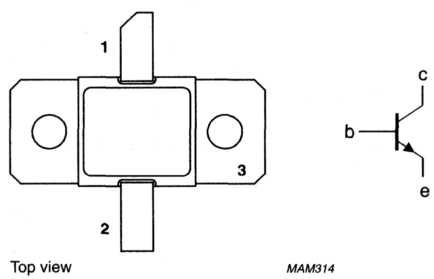


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

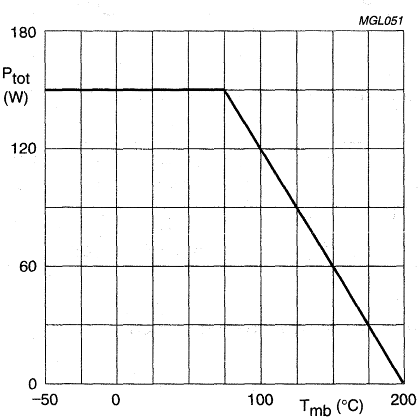
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)	$t_p \leq 10\ \mu s$; $\delta \leq 10\%$	–	3	A
P_{tot}	total power dissipation (peak power)	$T_{mb} = 75\ °C$; $t_p \leq 10\ \mu s$; $\delta \leq 10\%$	–	150	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 10\ \mu s$; $\delta = 10\%$; $P_{tot\ max} = 150$ W.

Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

T_j = 125 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	CW	4.9	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	CW; note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	notes 1 and 2	0.85	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a"*.
2. Equivalent thermal impedance under nominal pulse microwave operating conditions; t_p = 10 µs; δ = 10%.

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	V_{CB} = 65 V; I_E = 0	20	mA
		V_{CB} = 50 V; I_E = 0	2	mA
I_{CES}	collector cut-off current	V_{CE} = 60 V; R_{BE} = 0 Ω	20	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	200	µA

APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C measured in the test jig as shown in Fig.3 and working in class C broadband mode in pulse; note 1.

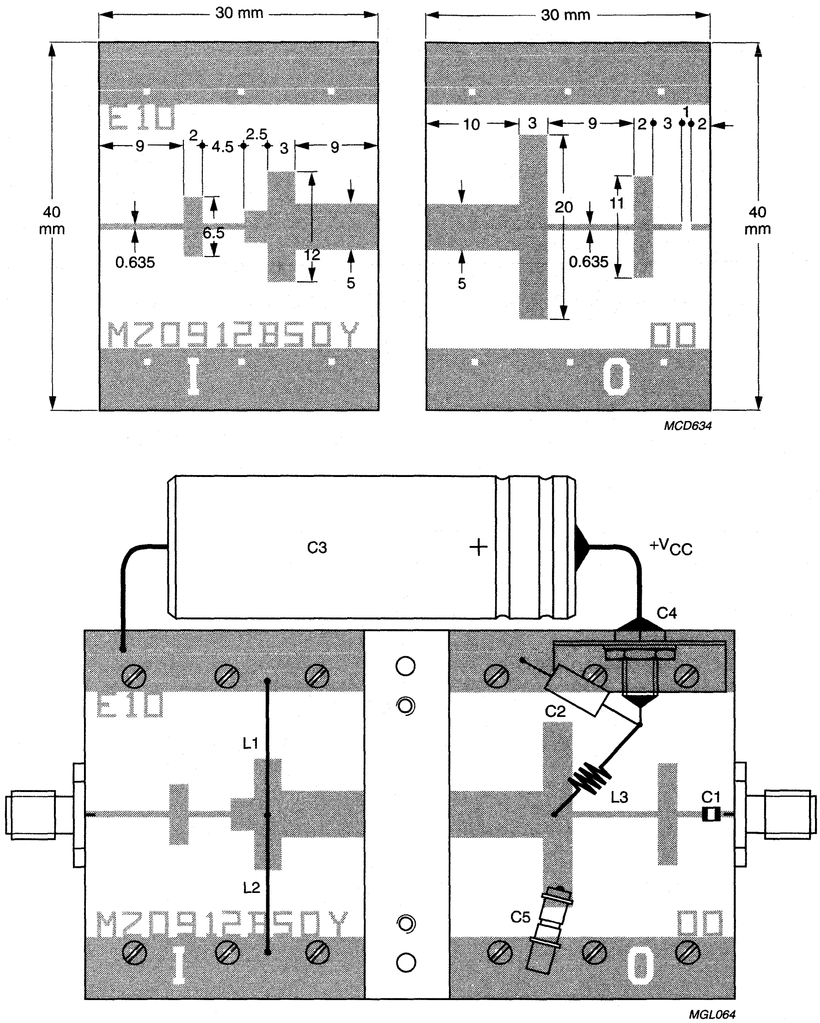
MODE OF OPERATION	f (GHz)	V_{CC} (V)(2)	P_L (W)	G_p (dB)	η_C (%)	Z_i/Z_L (Ω)
Class C; t_p = 10 µs; δ = 10%	0.960 to 1.215	50	>50 typ. 60	>7 typ. 8	>42 typ. 44	see Figs 6 and 7

Notes

1. Operating conditions and performance for other pulse formats can be made available on request.
2. V_{CC} during pulse.

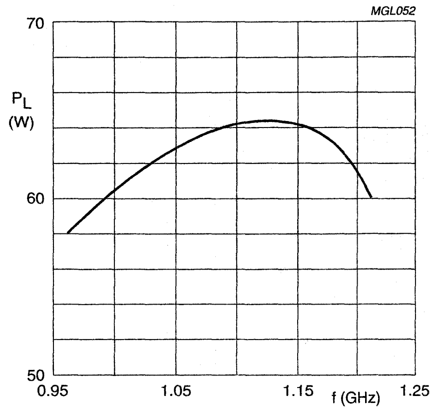
List of components (see Fig.3**).**

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1, L2	0.65 mm diameter copper wire	–	total length = 12 mm; height of loop = 9 mm	–
L3	4 turns 0.65 mm diameter copper wire;	–	int. dia. 3 mm; l = 5 mm	–
C1	capacitor	100 pF	–	ATC, ref. 100A101KP50X
C2	tantalum capacitor	10 µF; 50 V	–	–
C3	electrolytic capacitor	470 µF; 63 V	–	–
C4	feedthrough bypass capacitor	–	–	Erie, ref. 1250-003
C5, C6	variable gigatrim capacitor	0.6 to 4.5 pF	–	Tekelec, ref. 727.1



Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Broadband test circuit.



V_{CC} = 50 V; t_p = 10 μs; δ = 10%.

Fig.4 Load power as a function of frequency; (In broadband test circuit as shown in Fig.3).

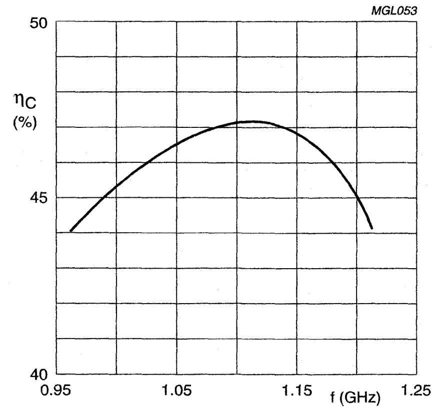
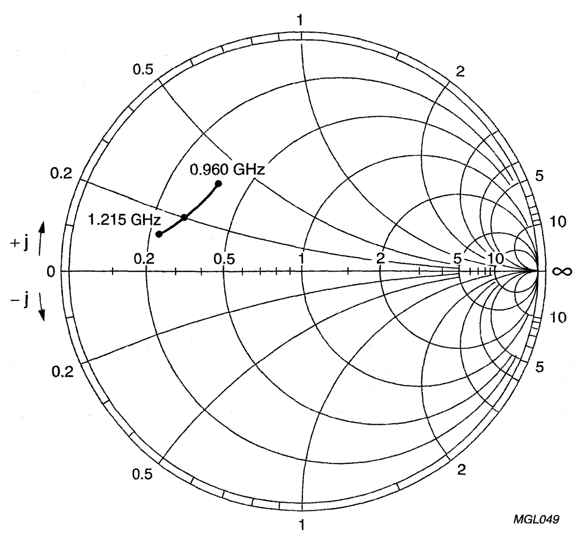
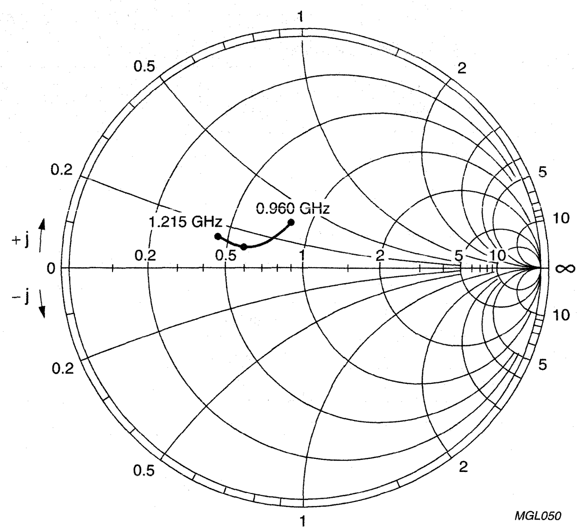


Fig.5 Collector efficiency as a function of frequency; (In broadband test circuit as shown in Fig.3).



V_{CC} = 50 V; Z_o = 10 Ω; P_L = 50 W.

Fig.6 Optimum load impedance as a function of frequency, associated with input impedance.



V_{CC} = 50 V; Z_o = 10 Ω; P_L = 50 W.

Fig.7 Input impedance as a function of frequency, associated with optimum load impedance.

Microwave power transistor — PTB23006U

FEATURES

- Very high power gain
- Diffused emitter ballasting resistors improve ruggedness
- Interdigitated emitter-base structure
- Gold metallization with barrier layer to prevent electromigration and gold diffusion during life
- Multicell geometry improves power sharing and reduces thermal resistance
- Internal input prematching network.

APPLICATIONS

Intended for use in common-base, class C power amplifiers at frequencies up to 2.3 GHz.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT440A hermetically sealed metal ceramic flange package, with base connected to flange.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common-base class C narrowband amplifier.

MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)	Z_i; Z_L (Ω)
Class C (CW)	2	28	>5	>9	>40	see Figs 5 and 6

PINNING - SOT440A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

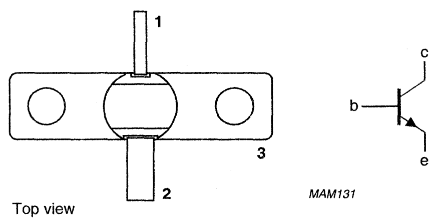


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	40	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current		–	0.75	A
P_{tot}	total power dissipation	$T_{mb} = 75$ °C	–	11	W
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C
T_{sld}	soldering temperature	t ≤ 10 s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.

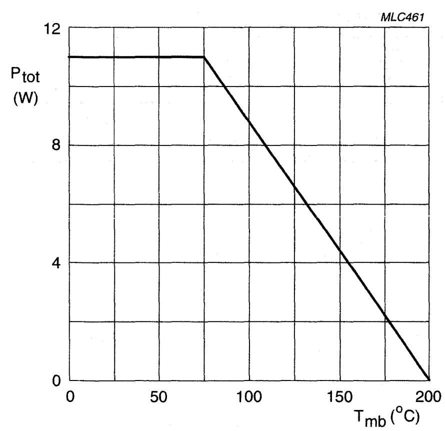


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_j = 75 °C	8.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.7	K/W

Note

1. See *"Mounting recommendations in the General part of handbook SC19a".*

CHARACTERISTICS

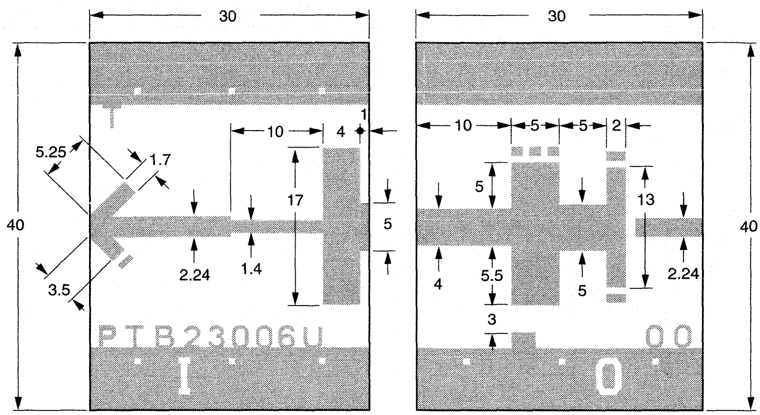
T_{mb} = 25 °C unless otherwise specified.

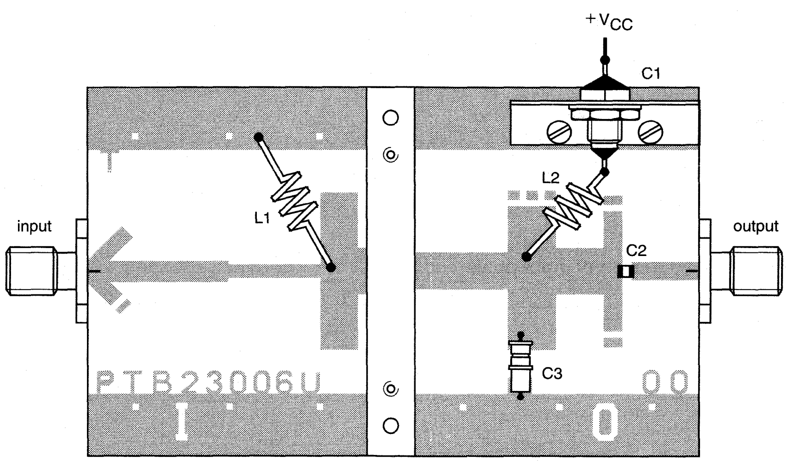
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CES}	collector cut-off current	$I_E = 0$; V_{CE} = 30 V	–	300	μA
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 3 mA; $I_E = 0$	40	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 3 mA; $R_{BE} = 0$	40	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 1.5 mA	3	–	V
h_{FE}	DC current gain	I_C = 450 mA; V_{CE} = 3 V	15	150	

APPLICATION INFORMATION

Microwave performance up to T_{mb} = 25 °C in a common-base class C test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	Z_i; Z_L (Ω)
class C (CW)	2	28	>5 typ. 5.8	>9 typ. 10.5	>40 typ. 45	see Figs 5 and 6





Dimensions in mm.
Substrate: PTFE fibreglass.
Thickness: 0.8 mm.
Permittivity: $\varepsilon_r = 2.54$.

Fig.3 Prematching test circuit.

List of components (see Fig.3)

COMPONENT	DESCRIPTION	VALUE	ORDERING INFORMATION
C1	feedthrough bypass capacitor		Erie1250-003
C2	DC blocking chip capacitor	100 pF	
C3	tuning capacitor	0.5 to 5 pF	Tekelec 5855
L1, L2	3 turns 0.5 mm copper wire; internal diameter = 2 mm		

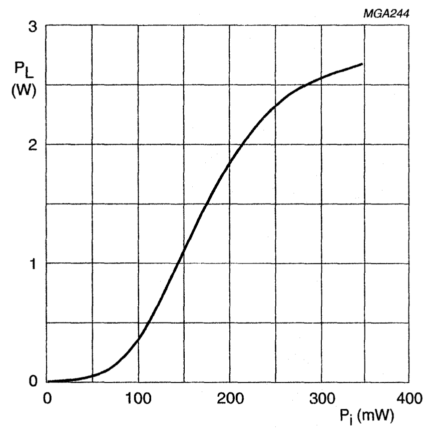
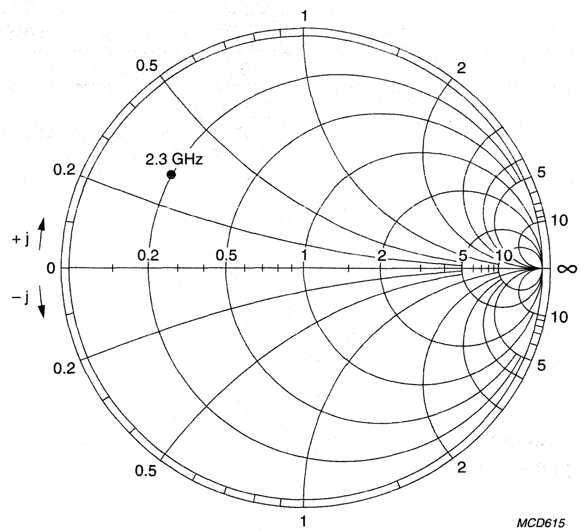
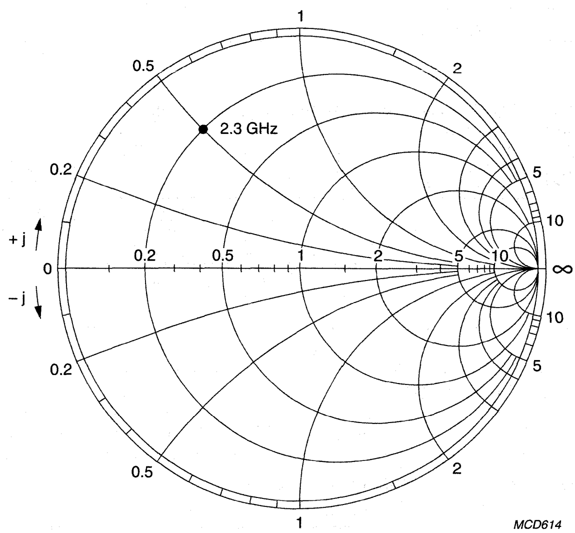


Fig.4 Load power as a function of input power.



V_{CC} = 28 V; Z_o = 50 Ω; P_L = 2.3 W.

Fig.5 Input impedance as a function of frequency.



V_{CC} = 28 V; Z_o = 50 Ω; P_L = 2.3 W.

Fig.6 Optimum load impedance as a function of frequency.

NPN microwave power transistors

PTB32001X; PTB32003X; PTB32005X

FEATURES

- Diffused emitter ballasting resistors providing excellent current sharing and withstanding a high VSWR
- Interdigitated structure provides high emitter efficiency
- Multicell geometry gives good balance of dissipated power and low thermal resistance
- Localized thick oxide auto-alignment process and gold sandwich metallization ensure an optimum temperature profile and excellent performance and reliability.

APPLICATIONS

Common-base, class B power amplifiers up to 4.2 GHz.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a metal ceramic SOT440A flange package with base connected to the flange.

MARKING

TYPE NUMBER	MARKING CODE
PTB32001X	3201X
PTB32003X	3203X
PTB32005X	3205X

PINNING - SOT440A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

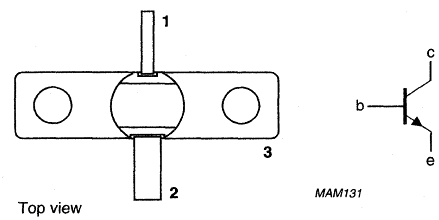


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common-base class B circuit.

TYPE NUMBER	MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_{po} (dB)	η_C (%)	Z_i (Ω)	Z_L (Ω)
PTB32001X	CW	3	24	≥1.3	≥8	≥35	15 + j31	5.5 + j10
PTB32003X	CW	3	24	≥2.5	≥8	≥35	5.5 + j29	5 – j2.2
PTB32005X	CW	3	24	≥4.5	≥8	≥35	2.8 + j20	4 – j7

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

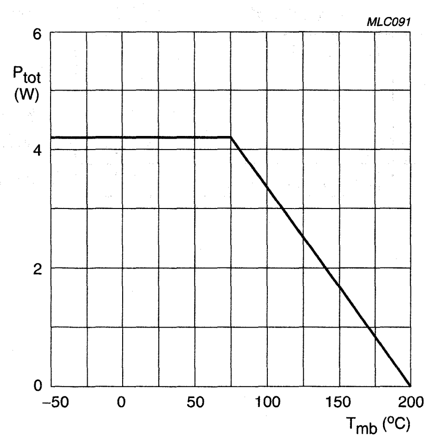
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	3.0	V
I_C	collector current (DC)				
	PTB32001X		–	0.25	A
	PTB32003X		–	0.5	A
	PTB32005X		–	0.75	A
P_{tot}	total power dissipation	$T_{mb} \leq 75$ °C; f > 1 MHz			
	PTB32001X		–	4.2	W
	PTB32003X		–	7.6	W
	PTB32005X		–	8.7	W
T_{stg}	storage temperature range		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	t ≤ 10 s; note 1	–	235	°C

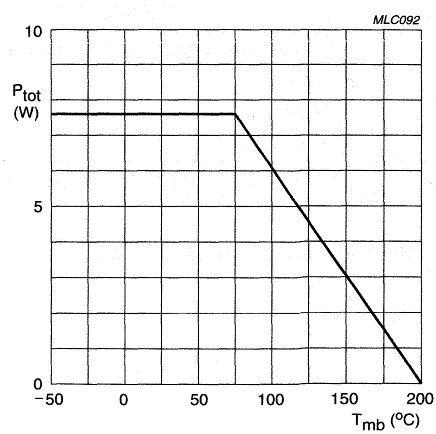
Note

1. Up to 0.3 mm from ceramic.



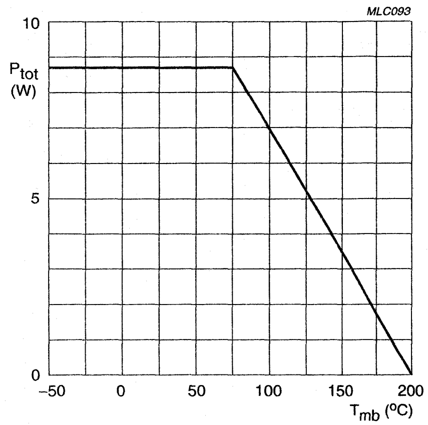
f > 1 MHz.

Fig.2 Power derating curve; PTB32001X.



f > 1 MHz.

Fig.3 Power derating curve; PTB32003X.



f > 1 MHz.

Fig.4 Power derating curve; PTB32005X.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_j = 75 °C		
	PTB32001X		22	K/W
	PTB32003X		12	K/W
	PTB32005X		10.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_j = 75 °C; note 1	0.7	K/W

Note

1. See *"Mounting recommendations in the General part of handbook SC19a"*.

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage					
	PTB32001X	I_C = 1 mA; I_E = 0	40	–	–	V
	PTB32003X	I_C = 2 mA; I_E = 0	40	–	–	V
	PTB32005X	I_C = 3 mA; I_E = 0	40	–	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 10 mA; R_{BE} = 0 Ω	40	–	–	V
I_{CBO}	collector cut-off current					
	PTB32001X	V_{CE} = 24 V; I_E = 0	–	–	10	μA
	PTB32003X	V_{CE} = 24 V; I_E = 0	–	–	20	μA
	PTB32005X	V_{CE} = 24 V; I_E = 0	–	–	30	μA
I_{EBO}	emitter cut-off current					
	PTB32001X	V_{EB} = 1.5 V; I_C = 0	–	–	0.2	μA
	PTB32003X	V_{EB} = 1.5 V; I_C = 0	–	–	0.4	μA
	PTB32005X	V_{EB} = 1.5 V; I_C = 0	–	–	0.6	μA
C_{cb}	collector-base capacitance					
	PTB32001X	$I_E = I_C$ = 0; V_{CB} = 24 V; V_{EB} = 1.5 V; f = 1 MHz	–	2.2	–	pF
	PTB32003X	$I_E = I_C$ = 0; V_{CB} = 24 V; V_{EB} = 1.5 V; f = 1 MHz	–	3	–	pF
	PTB32005X	$I_E = I_C$ = 0; V_{CB} = 24 V; V_{EB} = 1.5 V; f = 1 MHz	–	3.8	–	pF
C_{ce}	collector-emitter capacitance					
	PTB32001X	$I_E = I_C$ = 0; V_{CB} = 24 V; V_{EB} = 1.5 V; f = 1 MHz	–	0.3	–	pF
	PTB32003X	$I_E = I_C$ = 0; V_{CB} = 24 V; V_{EB} = 1.5 V; f = 1 MHz	–	0.6	–	pF
	PTB32005X	$I_E = I_C$ = 0; V_{CB} = 24 V; V_{EB} = 1.5 V; f = 1 MHz	–	0.9	–	pF

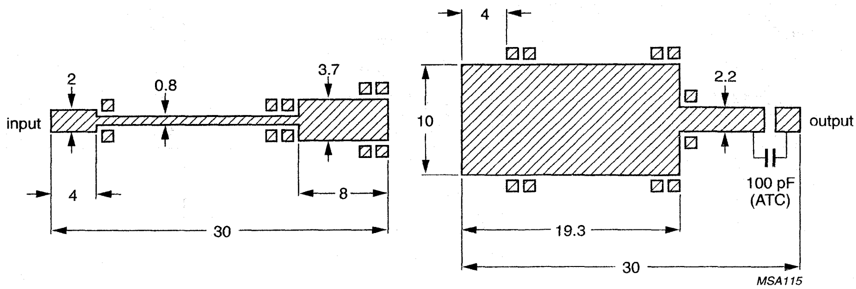
APPLICATION INFORMATION

Microwave performance in a common-base class B selective amplifier circuit; see note 1.

MODE OF OPERATION	TYPE NUMBER	f (GHz)	V_{CC} (V)	P_L (W)	G_{po} (dB)	η_C (%)
Class B (CW)	PTB32001X	3	24	>1.3; typ. 1.8	>8; typ. 9.5	>35; typ. 45
	PTB32003X	3	24	>2.5; typ. 3.0	>8; typ. 9.5	>35; typ. 45
	PTB32005X	3	24	>4.5; typ. 5.5	>8; typ. 9.5	>35; typ. 45

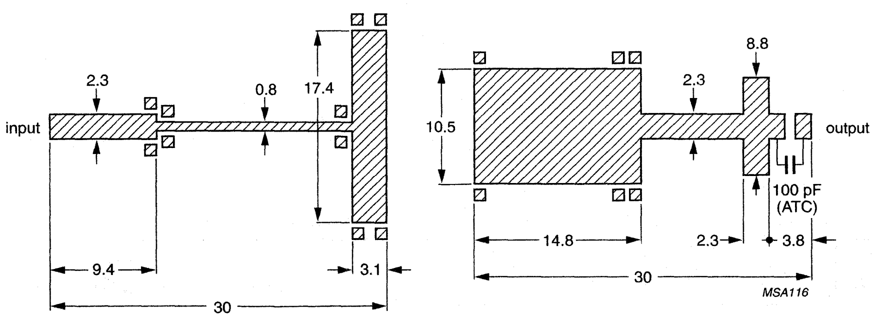
Note

1. Circuit consists of prematching circuit board in combination with complementary input and output slug tuners.



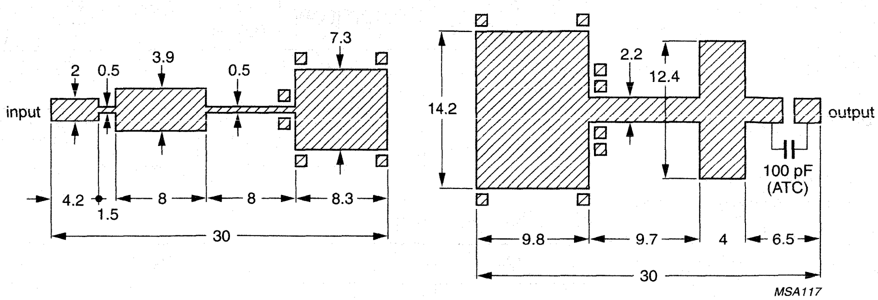
Dimensions in mm.
Thickness: 0.8 mm.
Permittivity: $\varepsilon_r = 2.55$.
Substrate: circuits on a double copper-clad printed-circuit board Teflon fibreglass dielectric.

Fig.5 Prematching test circuit board for PTB32001X.



Dimensions in mm.
Thickness: 0.8 mm.
Permittivity: $\varepsilon_r = 2.55$.
Substrate: circuits on a double copper-clad printed board Teflon fibre glass dielectric.

Fig.6 Prematching test circuit board for PTB32003X.



Dimensions in mm.

Thickness: 0.8 mm.

Permittivity: $\varepsilon_r = 2.55$.

Substrate: circuits on a double copper-clad printed board Teflon fibreglass dielectric.

Fig.7 Prematching test circuit board for PTB32005X.

NPN microwave power transistors — RX1214B80W; RX1214B130Y

FEATURES

- Suitable for short and medium pulse applications up to 1 ms pulse width, 10% duty factor
- Diffused emitter ballasting resistors improve ruggedness
- Interdigitated emitter-base structure provides high emitter efficiency
- Gold metallization with barrier realizes very stable characteristics and excellent lifetime
- Multicell geometry improves power sharing and reduces thermal resistance
- Internal input and output prematching networks allow an easier design of circuits.

APPLICATIONS

Common-base class C broadband pulsed power amplifiers for radar applications in the 1.2 to 1.4 GHz band. Also suitable for long pulse, heavy duty operation within this band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package, with base connected to flange.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common-base class C narrowband amplifier.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C RX1214B80W	t_p = 500 μs; δ = 10%	1.2 to 1.4	40	≥80	≥7	≥35
Class C RX1214B130Y	t_p = 150 μs; δ = 5%	1.2 to 1.4	50	≥130	≥7	≥35

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

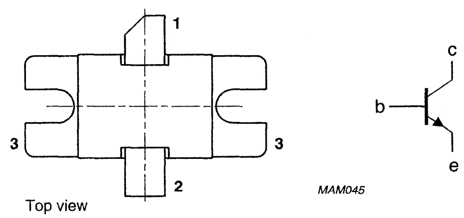


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

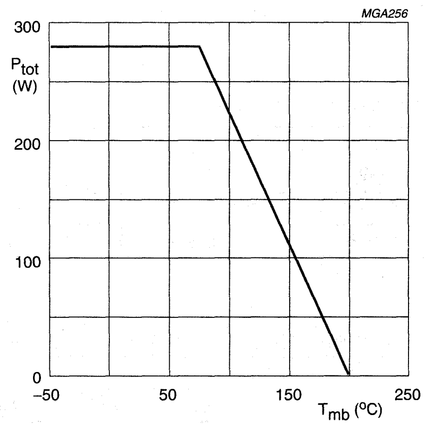
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)	$t_p \leq 150\ \mu s$; $\delta \leq 5\%$	–	9	A
P_{tot}	total power dissipation	$T_{mb} < 75\ °C$; $t_p \leq 150\ \mu s$; $\delta \leq 5\%$	–	280	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 150\ \mu s$; $\delta = 5\%$; $P_{tot\ max} = 280$ W.

Fig.2 Maximum power dissipation derating as a function of mounting base temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_j = 120 °C	1.75	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	t_p = 150 μs; δ = 5%; notes 1 and 2	0.4	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a"*.
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 50 V	–	6	mA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 1.5 V	–	0.6	mA
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 60 mA; V_{BE} = 0	60	–	V

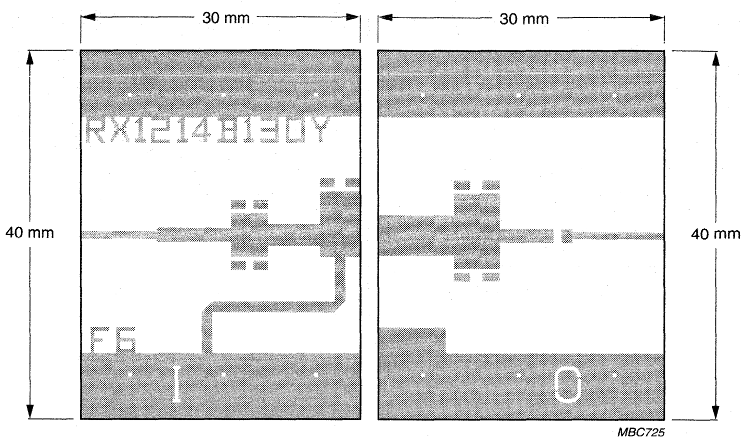
APPLICATION INFORMATION

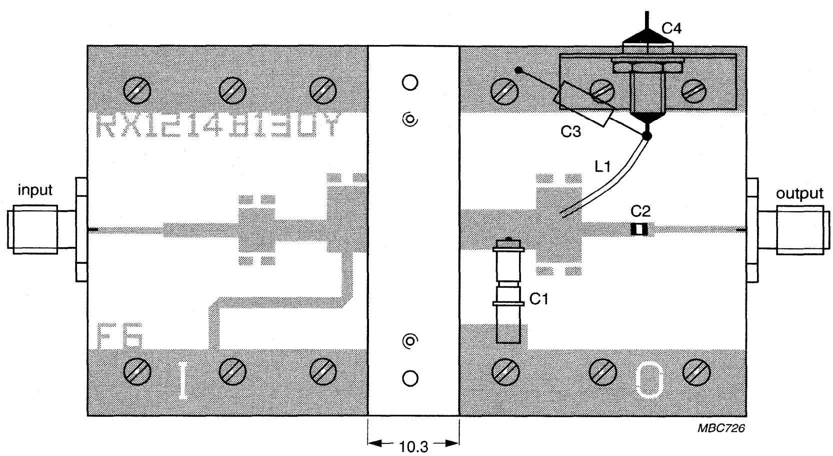
Microwave performance up to T_{mb} = 25 °C in a common-base test circuit as shown in Fig.3.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	t_p = 150 μs; δ = 5%	1.2 to 1.4	50	≥130; typ. 140	≥7; typ. 7.5	≥35; typ. 39
	t_p = 500 μs; δ = 10%	1.2 to 1.4	40	typ. 80	typ. 8.5	typ. 40

List of components (see Fig.3)

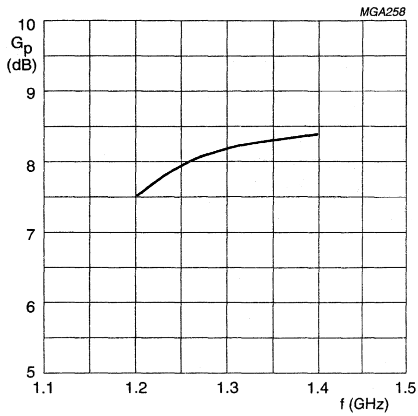
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1	0.5 mm copper wire		total length = 15 mm	
C1	trimmer capacitor	0.6 – 5 pF		Tekelec, ref AT3-7271SL
C2	chip capacitor			
C3	tantalum capacitor	10 μF, 50 V		
C4	feedthrough bypass capacitor			Erie, ref.1250-003





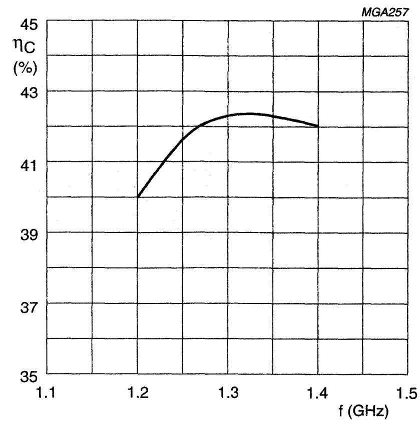
Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Broadband test circuit.



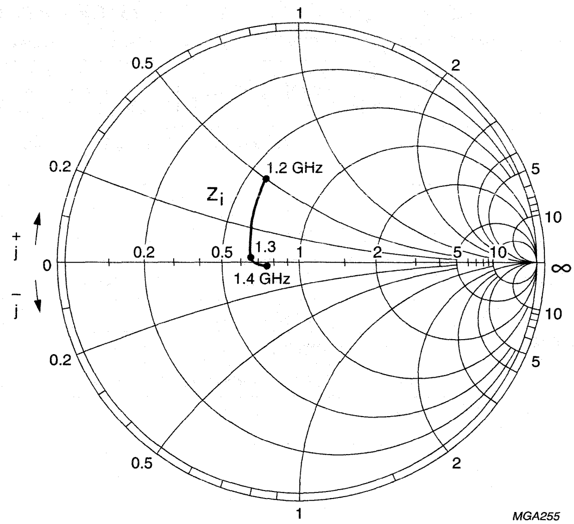
Class C pulse operation; t_p = 500 μs; δ = 5%.
V_{CC} = 50 V; P_O = 130 W.
Broadband test circuit as shown in Fig.3.

Fig.4 Power gain as a function of frequency.



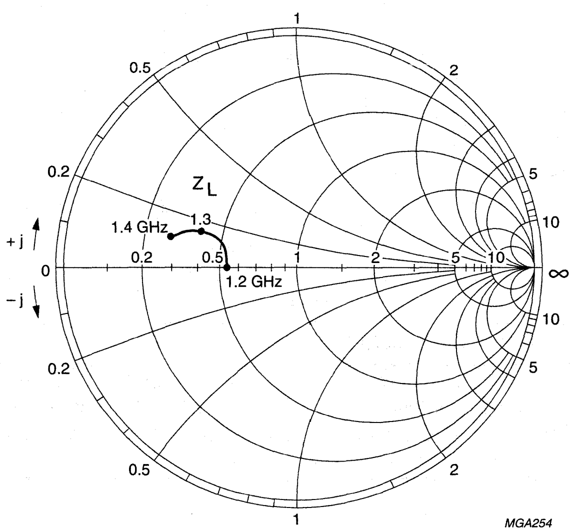
Class C pulse operation; t_p = 500 μs; δ = 5%.
V_{CC} = 50 V; P_O = 130 W.
Broadband test circuit as shown in Fig.3.

Fig.5 Collector efficiency as a function of frequency.



V_{CC} = 50 V; Z_O = 10 Ω; P_{OUT} = 130 W.

Fig.6 Input impedance as a function of frequency, associated with optimum load impedance.



V_{CC} = 50 V; Z_O = 10 Ω; P_{OUT} = 130 W.

Fig.7 Load impedance as a function of frequency, associated with optimum input impedance.

FEATURES

- Suitable for short and medium pulse applications up to 1 ms pulse width, 10% duty factor
- Diffused emitter ballasting resistors improve ruggedness
- Interdigitated emitter-base structure provides high emitter efficiency
- Gold metallization with barrier realizes very stable characteristics and excellent lifetime
- Multicell geometry improves power sharing and reduces thermal resistance
- Internal input and output prematching networks allow an easier design of circuits.

APPLICATIONS

Intended for use in common-base class C broadband pulsed power amplifiers for radar applications in the 1.2 to 1.4 GHz band. Also suitable for long pulse, heavy duty operation within this band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package, with base connected to flange.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class C narrowband amplifier.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	t_p = 500 μs; δ = 10%	1.2 to 1.4	42	≥170	≥6.7	≥40

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

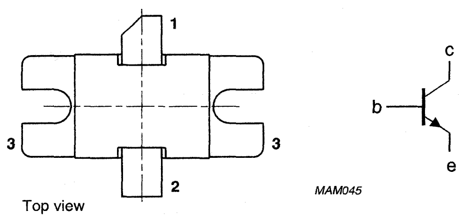


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

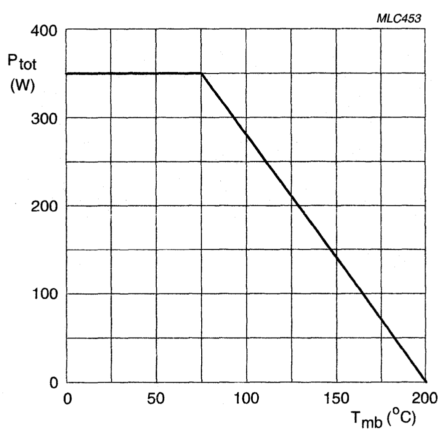
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current	$t_p \leq 150$ µs; $\delta \leq 5\%$	–	15	A
P_{tot}	total power dissipation	$T_{mb} \leq 75$ °C; $t_p \leq 150$ µs; $\delta \leq 5\%$	–	350	W
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$t_p = 150$ µs; $\delta = 5\%$.

Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_j = 120\ °C$	1.9	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.2	K/W
Z_{th}	thermal impedance from junction to heatsink	$t_p = 500\ \mu s$; $\delta = 10\%$; notes 1 and 2	0.28	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a"*.
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = 50\ V$	–	20	mA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 1.5\ V$	–	2	mA
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 60\ mA$; $V_{BE} = 0$	65	–	V

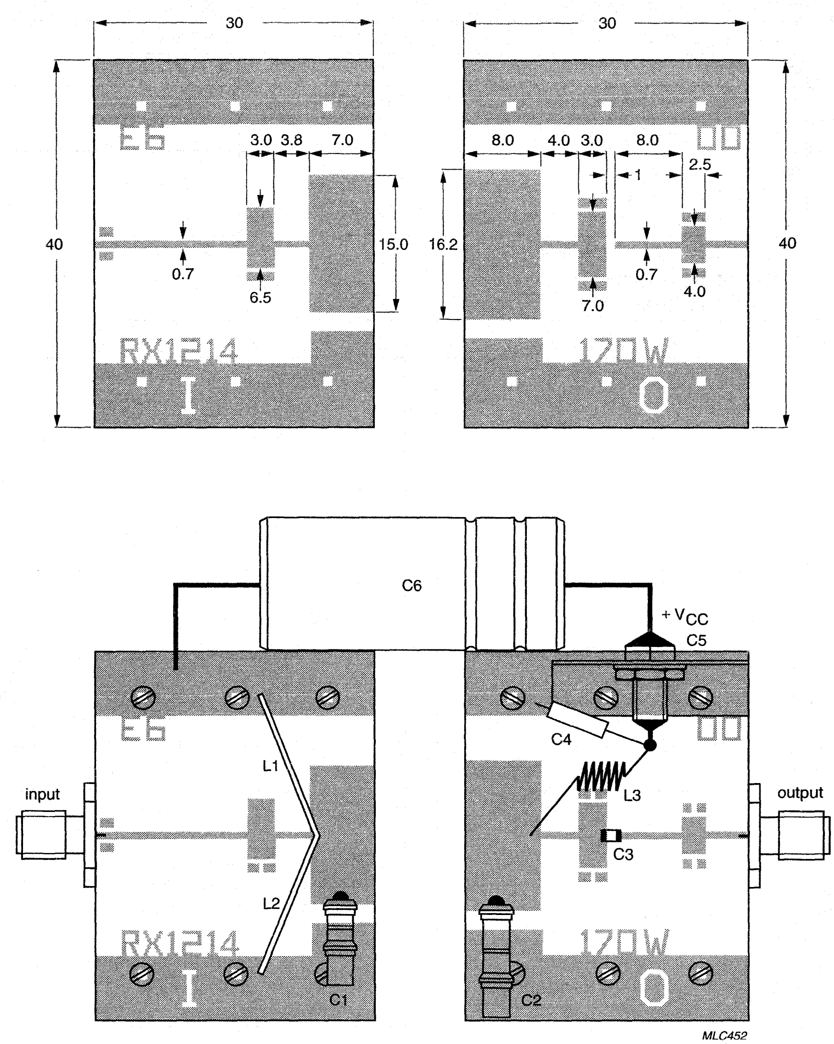
APPLICATION INFORMATION

Microwave performance up to $T_{mb} = 25\ °C$ in a common-base test circuit as shown in Fig.3; note 1.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	$t_p = 500\ \mu s$; $\delta = 10\%$	1.2 to 1.4	42	170	≥6.7 typ. 7.2	≥40 typ. 45

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

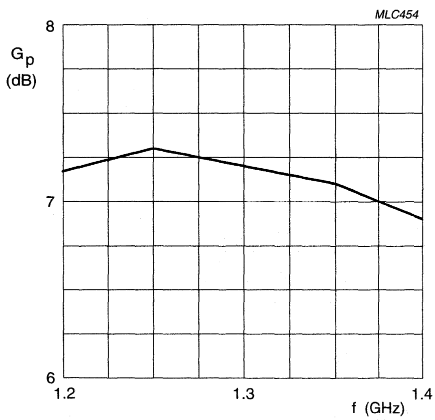


Dimensions in mm.
Substrate: Epsilam 10.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Broadband test circuit.

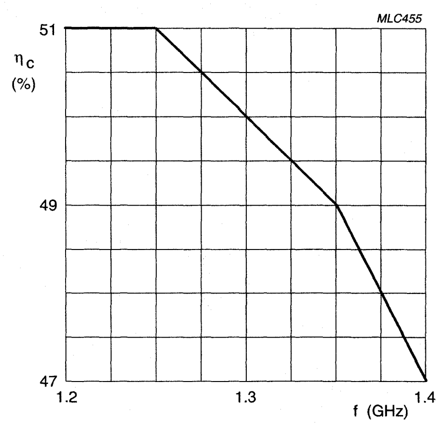
List of components (see Fig.3)

COMPONENT	DESCRIPTION	VALUE	ORDERING INFORMATION
C1	variable gigatrim capacitor	0.6 to 5 pF	Tekelec AT3-7271SL
C2	variable gigatrim capacitor	0.8 to 8 pF	Tekelec 729-1
C3	capacitor	100 pF	ATC 100A101kp50x
C4	tantalum capacitor	10 μF; 50 V	
C5	feedthrough bypass capacitor		Erie 1250-003
L1, L2	0.65 mm copper wire; total length = 24 mm; height of loop = 10 mm		
L3	4 turns 0.65 mm copper wire; total length = 4 mm; internal diameter = 3 mm		



Class C pulse operation.
t_p = 500 μs; δ = 10%; V_{CC} = 42 V; P_o = 170 W.
In broadband test circuit as shown in Fig.3.

Fig.4 Power gain as a function of frequency.



Class C pulse operation.
t_p = 500 μs; δ = 10%; V_{CC} = 42 V; P_o = 170 W.
In broadband test circuit as shown in Fig.3.

Fig.5 Collector efficiency as a function. of frequency.

NPN microwave power transistor RX1214B300Y

FEATURES

- Interdigitated structure provides high emitter efficiency
- Diffused emitter ballasting resistors providing excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry improves power sharing and reduces thermal resistance
- Internal input and output matching networks for an easy circuit design.

APPLICATIONS

- Common base class-C wideband amplifiers operating under pulsed conditions, recommended for L-band radar applications.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package with the base connected to the flange.

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

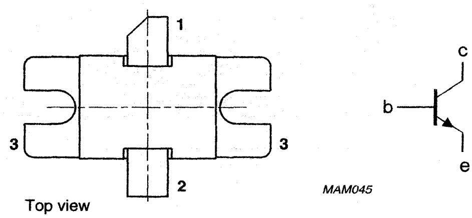


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance at $T_{mb} \leq 25$ °C in a common base class-C wideband amplifier.

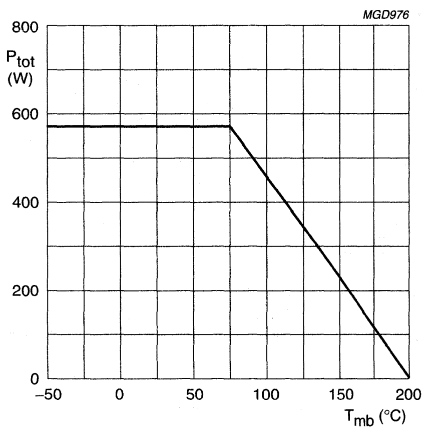
MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_P (dB)	η_C (%)	Z_i; Z_L (Ω)
Class-C $t_p = 150$ µs; $\delta = 5$ %	1.2 to 1.4	50	≥250	≥7	≥35	see Fig 6

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)	$t_p \leq 150\ \mu s$; $\delta = 5\ \%$	–	21	A
P_{tot}	total power dissipation	$t_p \leq 150\ \mu s$; $\delta = 5\ \%$; $T_{mb} = 75\ °C$	–	570	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	at 0.2 mm from case; $t \leq 10$ s	–	235	°C



$t_p = 150\ \mu s$; $\delta = 5\ \%$

Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

T_j = 100 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base		0.8	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	t_p = 150 μs; δ = 5 %; notes 1 and 2	0.22	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a".*
2. Equivalent thermal impedance under nominal pulse microwave operating conditions.

CHARACTERISTICS

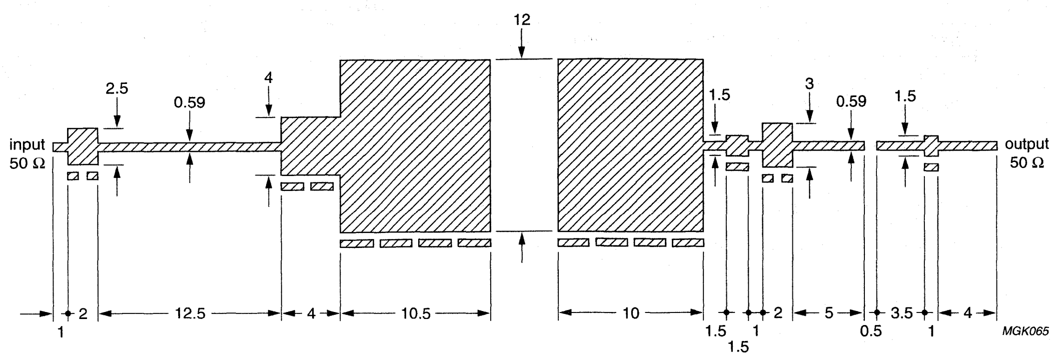
T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 140 mA; I_E = 0	65	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 140 mA; R_{BE} = 0 Ω	60	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 0; I_E = 20 mA	3	–	V
I_{CBO}	collector cut-off current	V_{CB} = 50 V; I_E = 0	–	14	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	–	1.4	mA

APPLICATION INFORMATION

Microwave performance at T_{mb} ≤ 25 °C in a common base class C wideband amplifier.

MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_P (dB)	η_C (%)	Z_i; Z_L (Ω)
Pulsed t_p = 150 μs; δ = 5 %	1.2 to 1.4	50	≥250 typ. 320	≥7 typ. 8	≥35 typ. 40	see Fig 6
t_p = 300 μs; δ = 10 %	1.2 to 1.4	50	typ. 300	typ. 7.5	typ. 35	see Fig 6



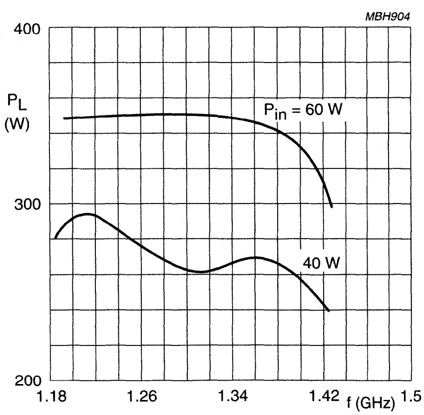
Dimensions in mm.

Substrate: Epsilam printed-circuit board.

Thickness: 0.635 mm.

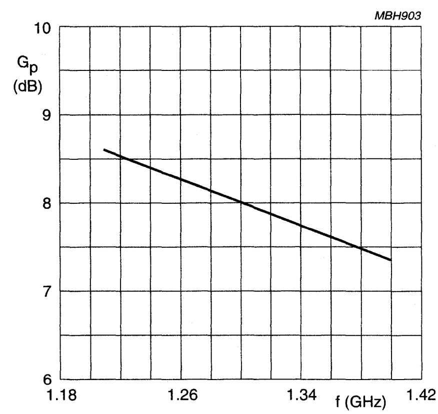
Permittivity: ε_r = 10.

Fig.3 Wideband test circuit board for 1.2 to1.4 GHz application.



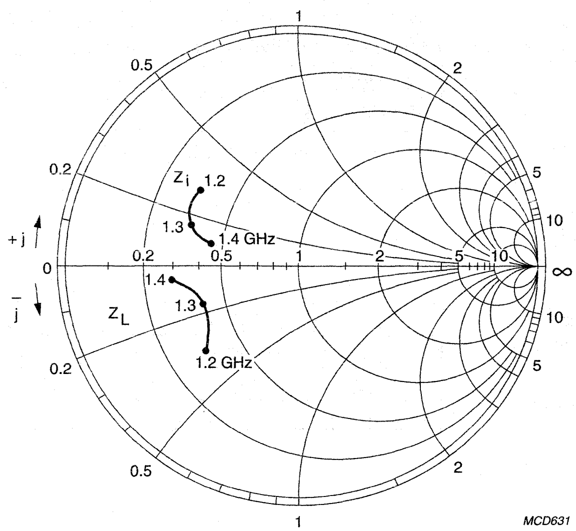
t_p = 150 μs; δ = 5 %.

Fig.4 Load power as a function of frequency; typical values.



t_p = 150 μs; δ = 5 %.

Fig.5 Power gain as a function of frequency; typical values.



Z_o = 5 Ω; V_{CC} = 50 V; P_L = 250 W; T_{mb} = 25 °C; t_p = 150 μs; δ = 5 %; class C operation.

Fig.6 Input and optimum load impedances as functions of frequency; typical values.

NPN microwave power transistor | RX1214B350Y

FEATURES

- Suitable for short and medium pulse applications up to 1 ms/10%
- Internal input prematching networks allow an easier design of circuits
- Diffused emitter ballasting resistors improve ruggedness
- Interdigitated emitter-base structure provides high emitter efficiency
- Gold metallization with barrier realizes very stable characteristics and excellent lifetime
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

Common base, class C, broadband, pulsed power amplifiers for L-Band radar applications in the 1.2 to 1.4 GHz band. Also suitable for medium pulse, heavy duty operation within this band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT439A metal ceramic flange package with base connected to flange.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class C broadband amplifier.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)
Class C	t_p = 130 μs; δ = 6%	1.2 to 1.4	50	280	≥7	≥40

PINNING - SOT439A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

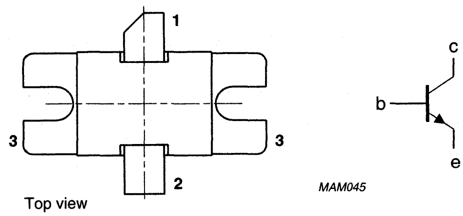


Fig.1 Simplified outline and symbol.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

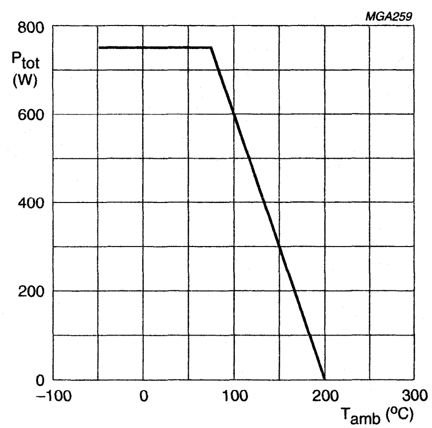
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	65	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)	$t_p \leq 130\ \mu s$; $\delta \leq 6\%$	–	25	A
P_{tot}	total power dissipation	$T_{mb} < 75\ °C$; $t_p \leq 30\ \mu s$; $\delta \leq 1\%$	–	750	W
T_{stg}	storage temperature		–65	200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	$t \leq 10$ s; note 1	–	235	°C

Note

1. Up to 0.2 mm from ceramic.



$P_{tot\ max} = 750$ W; $t_p \leq 30\ \mu s$; $\delta \leq 1\%$.

Fig.2 Maximum power dissipation derating as a function of mounting base temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_j = 120$ °C	1.2	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	$t_p = 130$ μs; $\delta = 6\%$; $T_j = 110$ °C; notes 1 and 2	0.17	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a"*.
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
I_{CBO}	collector cut-off current	$V_{CB} = 50$ V; $I_E = 0$	30	mA
I_{EBO}	emitter cut-off current	$V_{EB} = 1.5$ V; $I_C = 0$	3	mA

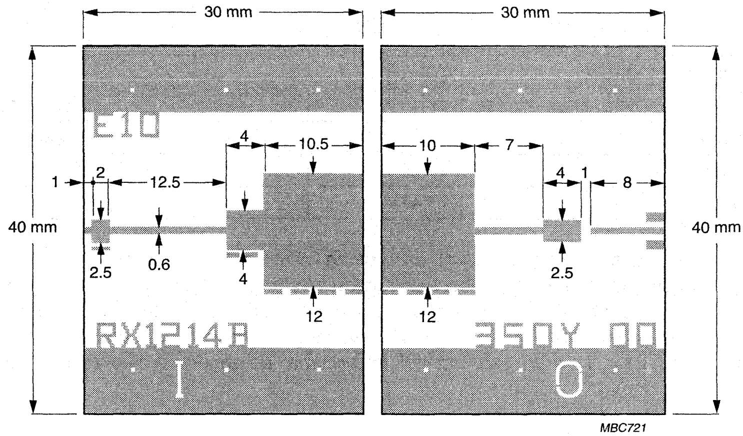
APPLICATION INFORMATION

Microwave performance up to $T_{mb} = 25$ °C in a common base test circuit as shown in Fig.3.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V) note 1	P_L (W)	G_p (dB)	η_C (%)
Class C	$t_p = 130$ μs; $\delta = 6\%$; note 2	1.2 to 1.4	50	280	≥7; typ. 8	≥40; typ. 44

Notes

1. V_{CC} during pulse.
2. Operating conditions and performances for other pulse formats can be made available on request.



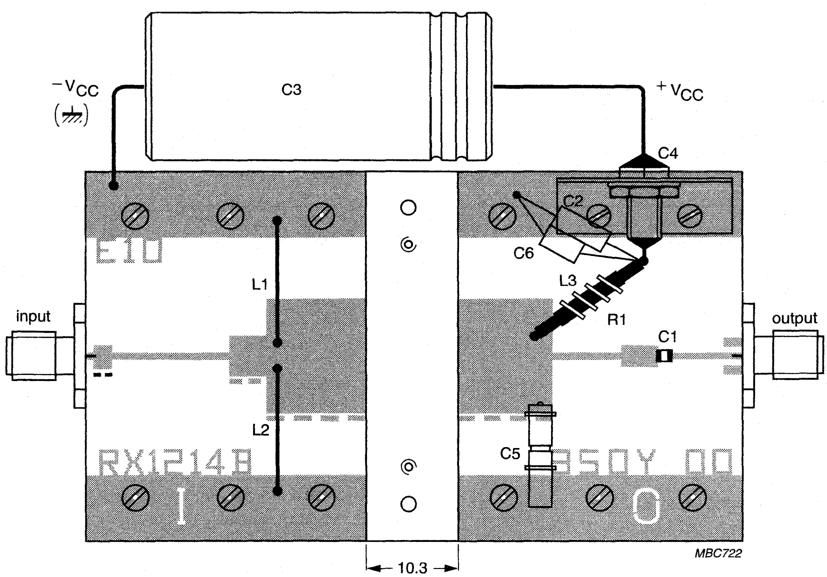
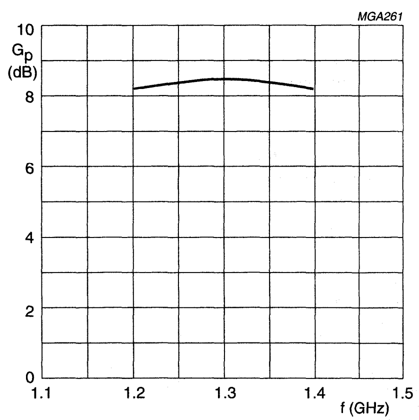


Fig.3 Broadband test circuit.

List of components (see Fig.3)

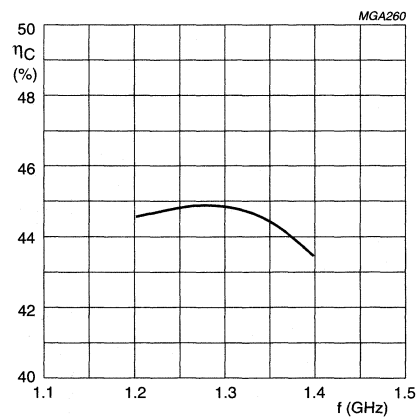
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1, L2, L3	3 turns 0.65 mm diameter copper wire		int dia. = 4 mm; length of turn = 3 mm	
C1	capacitor	100 pF		ATC, ref. 100B101KP50X
C2	tantalum capacitor	10 μF, 50 V		
C3	electrolytic capacitor	470 μF, 63 V		
C4	feedthrough bypass capacitor			Erie, ref.1250-003
C5	variable gigatrim capacitor	0.8 - 8 pF		Tekelec, ref.729.1
C6	capacitor	4.7 nF		
R1	resistor	4.7 Ω		

The test jig consists of two circuits (input and output), each being 30 mm x 40 mm in size. The two circuits are mounted on a 10 mm thick hard aluminium alloy block. A recess should be machined in the aluminium block in which the transistor can be mounted. The mounting surface must be lapped to a surface roughness of Ra <0.5 μm and the sum of the depth of the recess and the thickness of the circuits should not exceed the specified minimum dimension between mounting face and the leads of the transistor. Tolerances on this dimension may be absorbed by placing a gold plated metal shim under the leads, close to the body of the transistor.



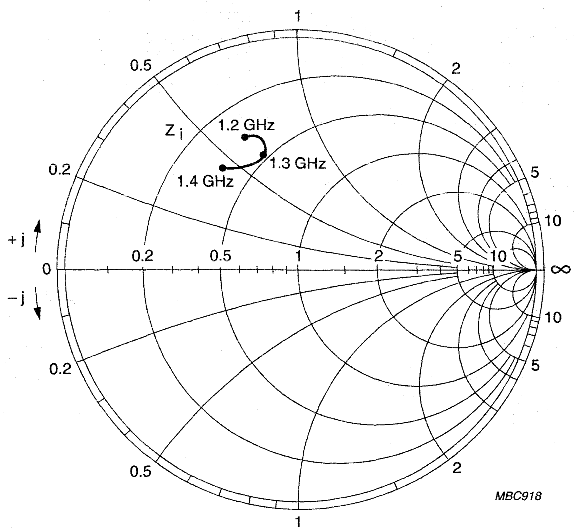
Class C pulse operation; t_p = 130 μs; δ = 6%.
V_{CC} = 50 V; P_O = 280 W.
Broadband test circuit as shown in Fig.3.

Fig.4 Power gain as a function of frequency.



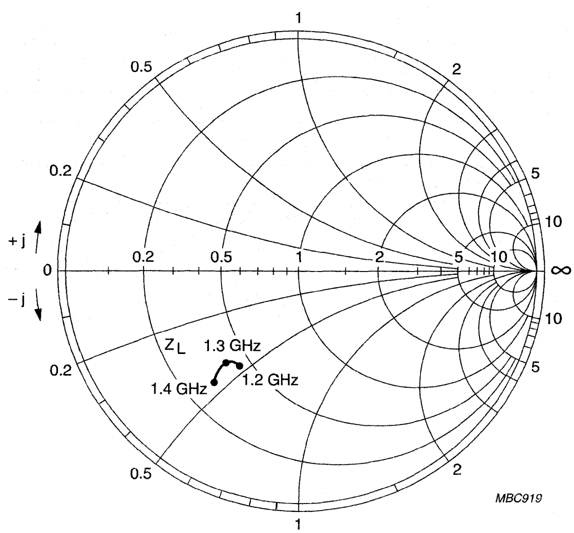
Class C pulse operation; t_p = 130 μs; δ = 6%.
V_{CC} = 50 V; P_O = 280 W.
Broadband test circuit as shown in Fig.3.

Fig.5 Collector efficiency as a function of frequency.



V_{CC} = 50 V; Z_O = 5 Ω; P_O = 280 W.

Fig.6 Input impedance as a function of frequency, associated with optimum load impedance.



V_{CC} = 50 V; Z_O = 5 Ω; P_O = 280 W.

Fig.7 Optimum load impedance as a function of frequency, associated with input impedance.

NPN microwave power transistor RZ1214B35Y

FEATURES

- Interdigitated structure provides high emitter efficiency
- Diffused emitter ballasting resistor providing excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry gives good balance of dissipated power and low thermal resistance
- Internal input matching ensures good stability and allows an easier design of wideband circuits.

APPLICATIONS

- Common base class-C wideband pulsed power amplifiers for L-band radar applications in the 1.2 to 1.4 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT443A metal ceramic flange package with the base connected to the flange.

PINNING - SOT443A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

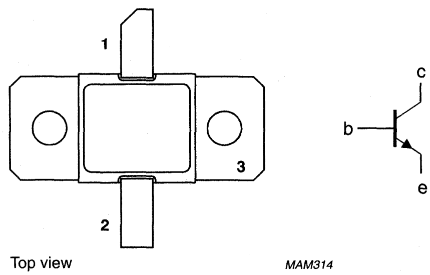


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class-C wideband amplifier.

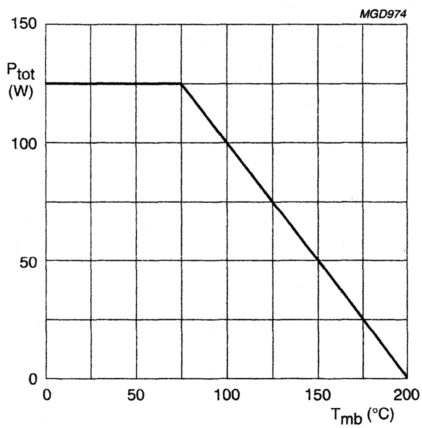
MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)	Z_i; Z_L (Ω)
Class-C; t_p = 150 μs; δ = 5%	1.2 to 1.4	50	≥35	≥7	≥30	see Fig 4

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)	$t_p \leq 150\ \mu s$; $\delta \leq 5\%\leq$	–	3	A
P_{tot}	total power dissipation	$T_{mb} \leq 75\ °C$; $t_p \leq 150\ \mu s$; $\delta \leq 5\%$	–	125	W
T_{stg}	storage temperature		–65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	at 0.2 mm from the case; $t \leq 10$ s	–	235	°C



$t_p = 150\ \mu s$; $\delta = 5\%$.

Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

T_j = 75 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base		5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	t_p = 100 µs; δ = 10 %; notes 1 and 2	1	K/W

Notes

1. See *"Mounting recommendations in the General part of handbook SC19a".*
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

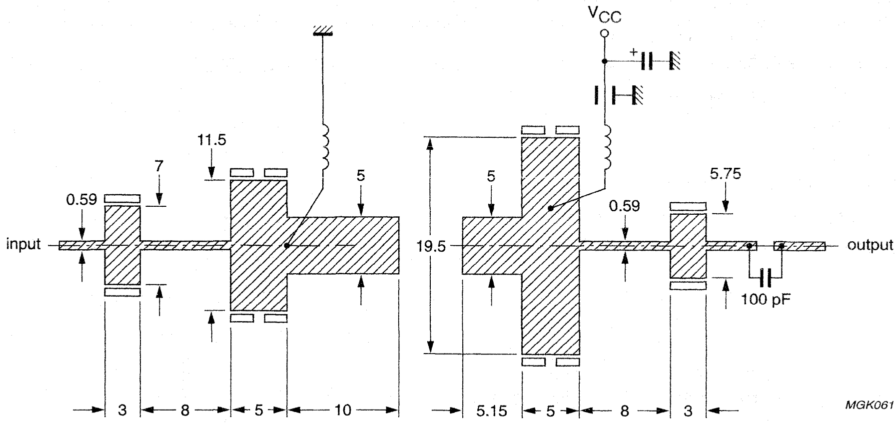
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 20 mA; I_E = 0	65	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 20 mA; R_{BE} = 0	60	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 0; I_E = 3 mA	3	–	V
I_{CBO}	collector cut-off current	V_{CB} = 50 V; I_E = 0	–	2	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	–	0.2	mA

APPLICATION INFORMATION

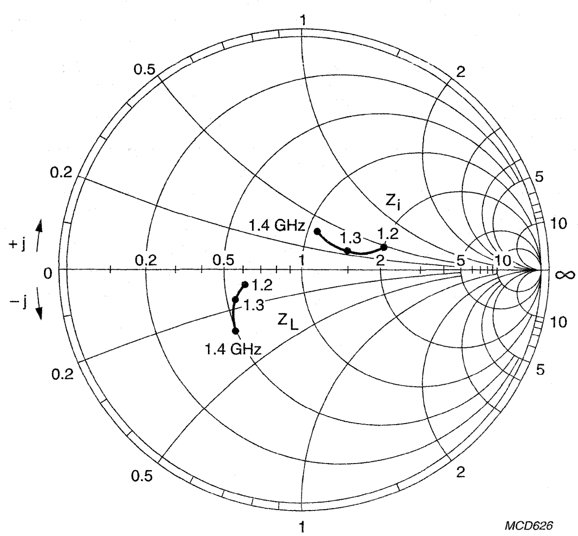
The transistors are 100% tested under the following conditions

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)	Z_i; Z_L (Ω)
Class-C	t_p = 150 µs; δ = 5%	1.2 to 1,4	50	typ.40; >35	typ.7.8; >7	typ.35; >35	see Fig 4
	t_p = 300 µs; δ = 10%	1.2 to 1,4	50	typ.40;	typ.7	typ.35	see Fig 4



Dimensions in mm.
Substrate: Epsilam.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Wideband test circuit for class C operation at 1.2 to 1.4 GHz.



Class C operation; $V_{CE} = 50$ V; $P_L = 35$ W; $Z_o = 5\ \Omega$; $t_p = 150\ \mu s$; $\delta = 5\%$.

Fig.4 Input and optimum load impedances as functions of frequency; typical values.

NPN microwave power transistor RZ1214B65Y

FEATURES

- Interdigitated structure provides high emitter efficiency
- Diffused emitter ballasting resistor providing excellent current sharing and withstanding a high VSWR
- Gold metallization realizes very stable characteristics and excellent lifetime
- Multicell geometry gives good balance of dissipated power and low thermal resistance
- Internal input and output matching ensures good stability and allows an easier design of wideband circuits.

APPLICATIONS

- Intended for use in common base class C wideband pulsed power amplifiers for L-band radar applications in the 1.2 to 1.4 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a SOT443A metal ceramic flange package with the base connected to the flange.

PINNING - SOT443A

PIN	DESCRIPTION
1	collector
2	emitter
3	base connected to flange

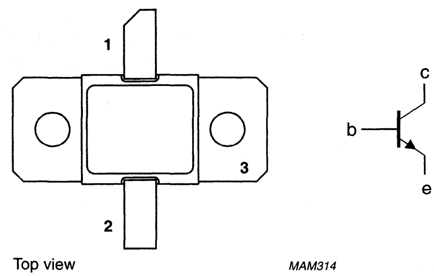


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Microwave performance up to T_{mb} = 25 °C in a common base class-C wideband amplifier.

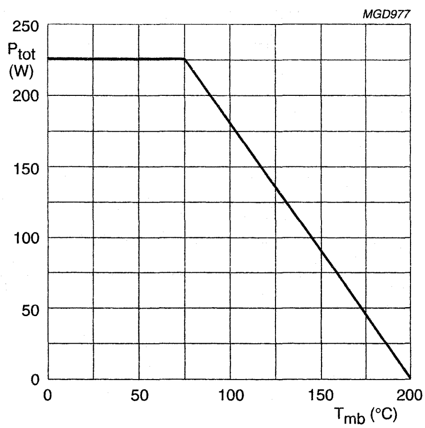
MODE OF OPERATION	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)	Z_i; Z_L (Ω)
Class-C; t_p = 150 µs; δ = 5%	1.2 to 1.4	50	≥70	≥7	≥35	see Fig 4

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO slab is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$	–	60	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)	$t_p \leq 150\ \mu s$; $\delta \leq 5\%$	–	6	A
P_{tot}	total power dissipation	$T_{mb} \leq 75\ °C$; $t_p \leq 150\ \mu s$; $\delta \leq 5\%$	–	225	W
T_{stg}	storage temperature		−65	+200	°C
T_j	operating junction temperature		–	200	°C
T_{sld}	soldering temperature	at 0.2 mm from the case; $t \leq 10$ s	–	235	°C



$t_p = 150\ \mu s$; $\delta = 5\%$.

Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

T_j = 75 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base		2.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	note 1	0.2	K/W
$Z_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	t_p = 100 μs; δ = 10 %; notes 1 and 2	0.55	K/W

Notes

1. See *"Mounting recommendations in the General part of associated Handbook".*
2. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

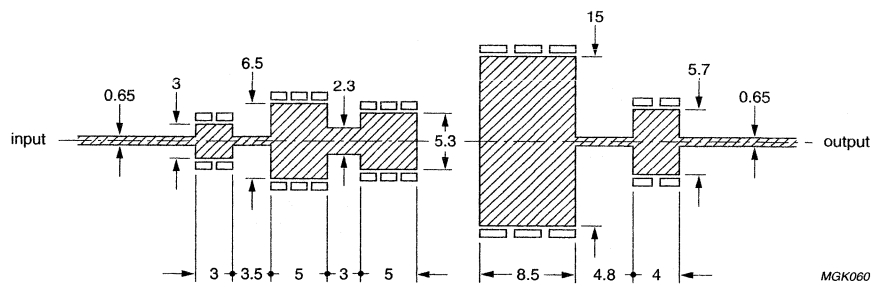
T_{mb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 40 mA; I_E = 0	65	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	I_C = 40 mA; R_{BE} = 0	60	–	V
I_{CBO}	collector cut-off current	V_{CB} = 50 V; I_E = 0	–	4	mA
I_{EBO}	emitter cut-off current	V_{EB} = 1.5 V; I_C = 0	–	0.4	mA

APPLICATION INFORMATION

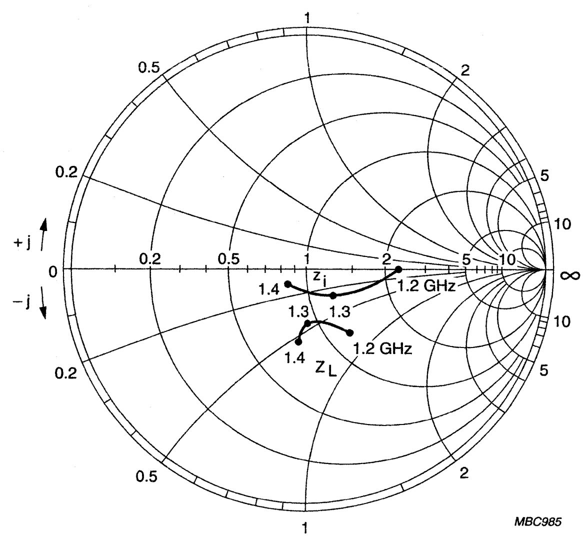
The transistors are 100% tested under the following conditions.

MODE OF OPERATION	CONDITIONS	f (GHz)	V_{CC} (V)	P_L (W)	G_p (dB)	η_C (%)	Z_i; Z_L (Ω)
Class-C	t_p = 150 μs; δ = 5%	1.2 to 1,4	50	typ.80; >70	typ.7.8; >7	typ.40; >35	see Fig 4
	t_p = 300 μs; δ = 10%	1.2 to 1,4	50	typ.80;	typ.7	typ.30	see Fig 4



Dimensions in mm.
Substrate: Epsilam.
Thickness: 0.635 mm.
Permittivity: $\varepsilon_r = 10$.

Fig.3 Wideband test circuit for class-C operation at 1.2 to 1.4 GHz.



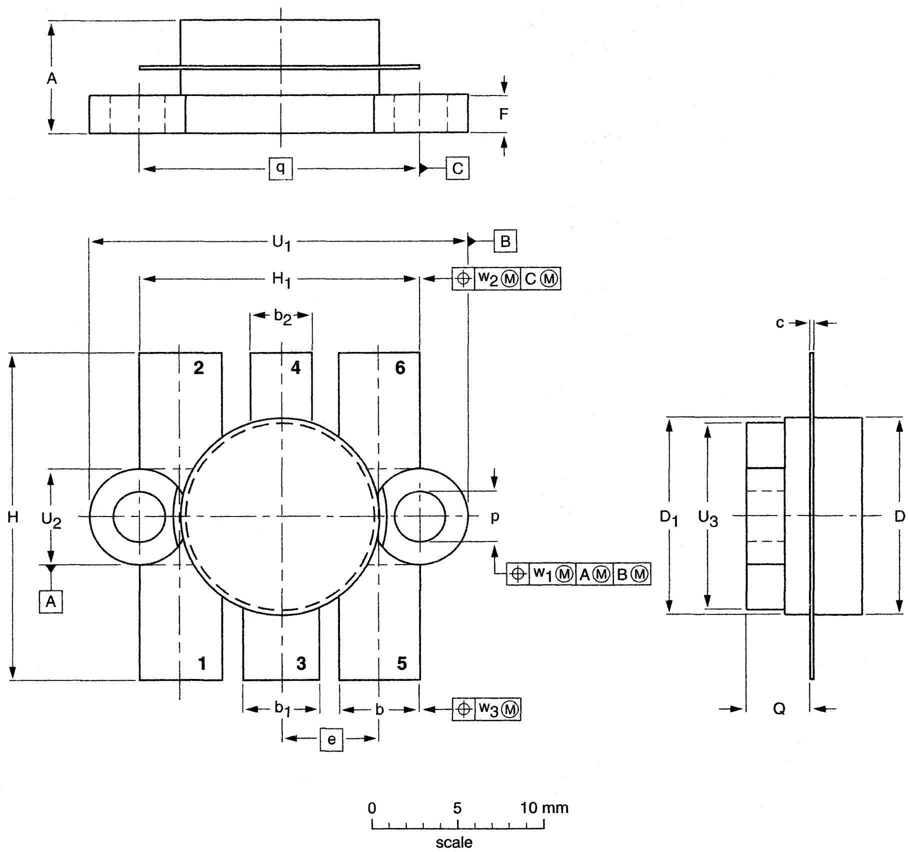
Class-C operation; $V_{CE} = 50$ V; $P_L = 65$ W; $Z_o = 5\ \Omega$; $t_p = 150\ \mu s$; $\delta = 5\%$.

Fig.4 Input and optimum load impedances as functions of frequency; typical values.

PACKAGE OUTLINES

Flanged ceramic package; 2 mounting holes; 6 leads

SOT119A

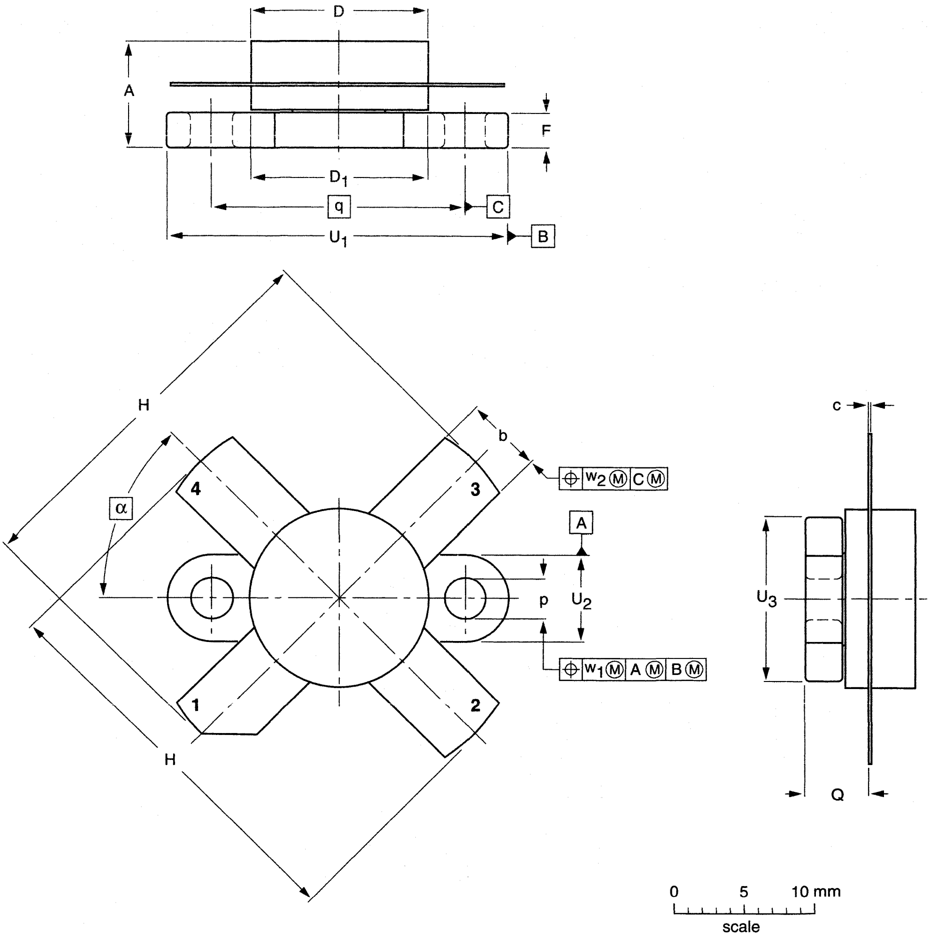


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	b_2	c	D	D_1	e	F	H	H_1	p	Q	q	U_1	U_2	U_3	w_1	w_2	w_3
mm	7.39 6.32	5.59 5.33	5.34 5.08	4.07 3.81	0.15 0.10	12.86 12.59	12.83 12.57	6.48	2.54 2.29	21.97 21.21	18.55 18.28	3.30 3.05	4.57 4.06	18.42	24.89 24.64	6.48 6.22	12.32 12.07	0.25	0.51	0.25
inches	0.291 0.249	0.220 0.210	0.210 0.200	0.160 0.150	0.006 0.004	0.505 0.496	0.505 0.495	0.255	0.100 0.090	0.865 0.835	0.730 0.720	0.130 0.120	0.180 0.160	0.725	0.980 0.970	0.255 0.245	0.485 0.475	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT119A						99-03-29

Flanged ceramic package; 2 mounting holes; 4 leads **SOT121B**



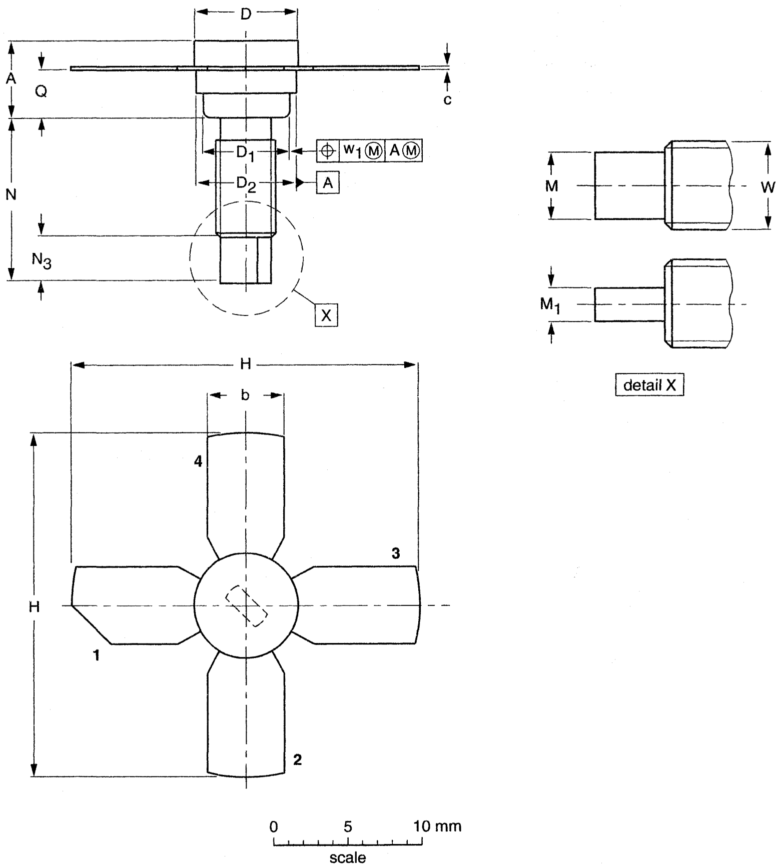
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.27 6.17	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	2.67 2.41	28.45 25.52	3.30 3.05	4.45 3.91	18.42	24.90 24.63	6.48 6.22	12.32 12.06	0.25	0.51	45°
inches	0.286 0.243	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.105 0.095	1.120 1.005	0.130 0.120	0.175 0.154	0.725	0.98 0.97	0.255 0.245	0.485 0.475	0.01	0.02	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT121B						99-03-29

Studded ceramic package; 4 leads

SOT122A

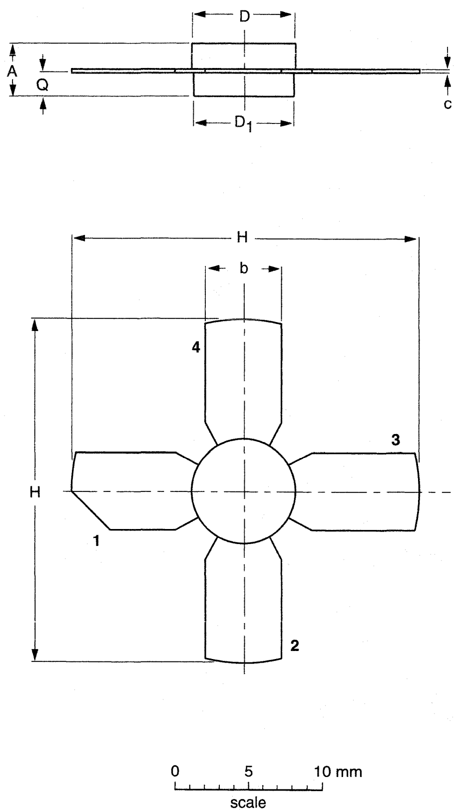


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	H	M	M_1	N	N_3	Q	W	w_1
mm	5.92 4.80	5.85 5.58	0.15 0.10	7.50 7.23	6.48 6.22	7.24 6.93	27.43 25.78	3.18 2.67	1.66 1.39	12.95 12.70	3.68 2.92	3.35 2.79	8-32 UNC	0.38
inches	0.233 0.189	0.230 0.220	0.006 0.004	0.295 0.285	0.255 0.245	0.285 0.273	1.080 1.015	0.125 0.105	0.065 0.055	0.510 0.500	0.145 0.115	0.132 0.110		0.015

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122A						99-03-29

Studless ceramic package; 4 leads **SOT122D**



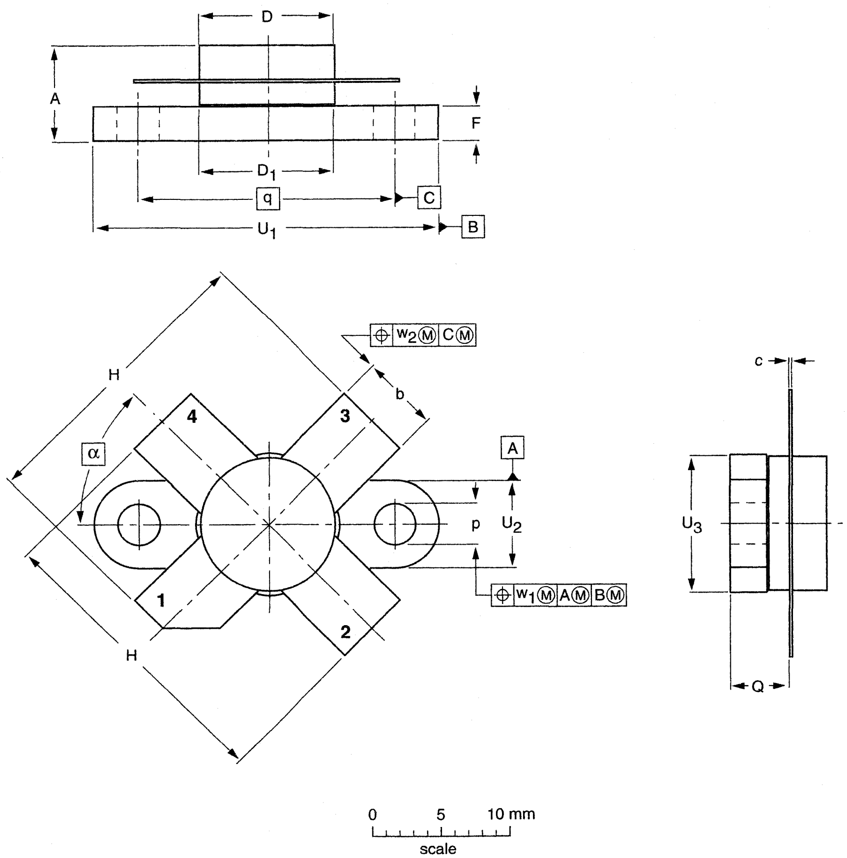
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	H	Q
mm	4.14 3.27	5.85 5.58	0.15 0.10	7.50 7.23	7.24 6.99	27.43 25.78	1.57 1.32
inches	0.163 0.129	0.230 0.220	0.006 0.004	0.295 0.285	0.285 0.275	1.080 1.015	0.062 0.052

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122D						99-03-29

Flanged ceramic package; 2 mounting holes; 4 leads

SOT123A



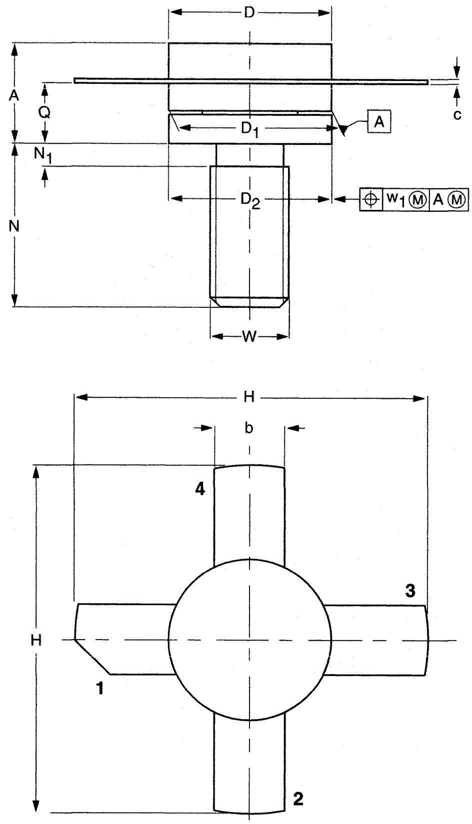
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.78 9.42	2.72 2.31	20.71 19.93	3.33 3.04	4.63 4.11	18.42	24.87 24.64	6.48 6.22	9.78 9.39	0.25	0.51	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.385 0.371	0.107 0.091	0.815 0.785	0.131 0.120	0.182 0.162	0.725	0.980 0.970	0.255 0.245	0.385 0.370	0.010	0.020	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						99-03-29

Studded ceramic package; 4 leads

SOT147A



0 5 10 mm

scale

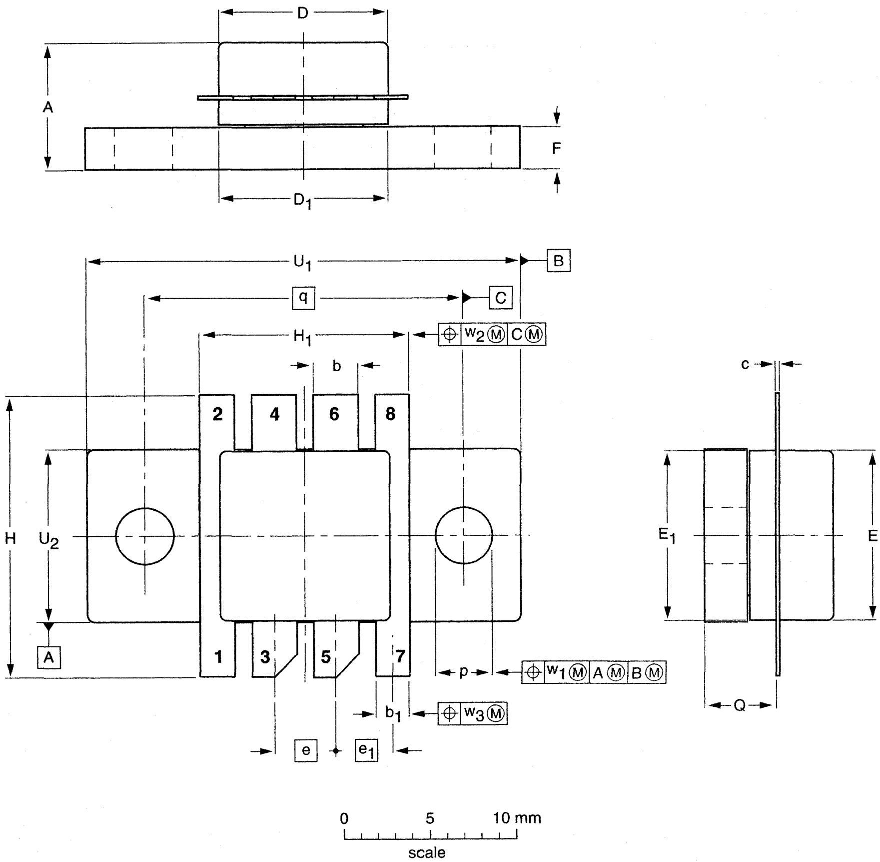
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	H	N	N_1 max.	Q	W	w_1
mm	8.06 7.18	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	12.83 12.57	28.45 27.43	13.39 12.62	1.40	5.24 4.92	1/4"× 28 UNF	0.51
inches	0.317 0.283	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.505 0.495	1.12 1.08	0.527 0.497	0.055	0.206 0.194		0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT147A						99-03-29

Flanged ceramic package; 2 mounting holes; 8 leads

SOT161A

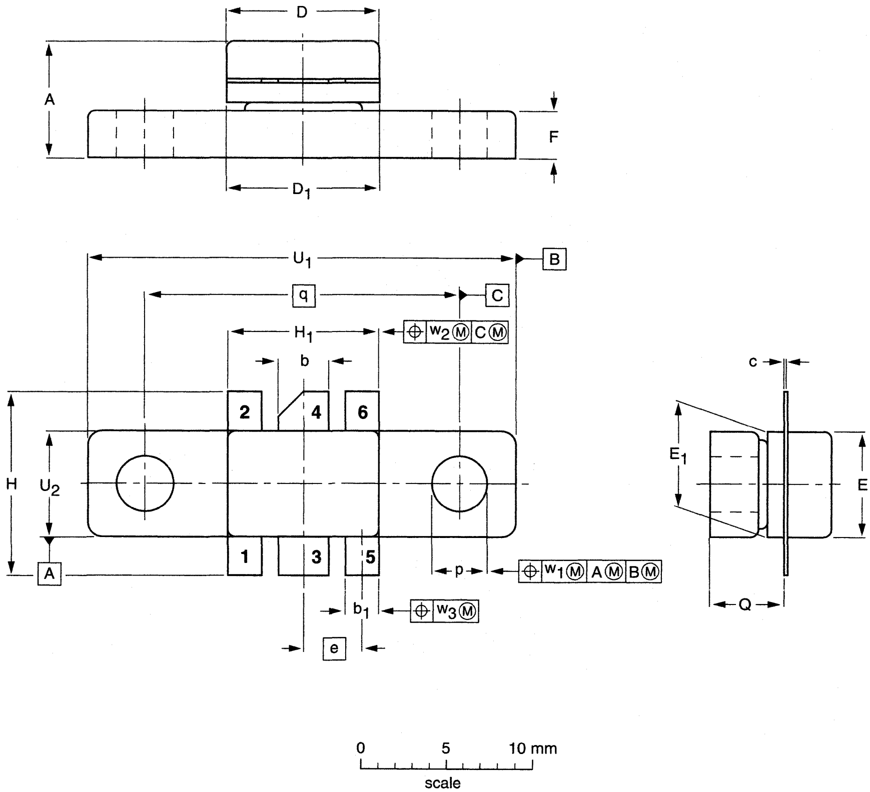


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	e_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	7.27 6.47	2.93 2.66	2.04 1.77	0.18 0.10	10.22 10.00	10.21 9.94	10.21 10.00	10.21 9.94	3.80	3.50	2.70 2.08	16.81 16.21	12.83 12.57	3.33 3.07	4.32 4.06	18.42	24.97 24.71	10.34 10.08	0.25	0.51	0.25
inches	0.286 0.255	0.115 0.105	0.080 0.070	0.007 0.004	0.402 0.394	0.402 0.391	0.402 0.394	0.402 0.391	0.150	0.138	0.106 0.082	0.662 0.638	0.505 0.495	0.131 0.121	0.170 0.160	0.725	0.983 0.973	0.407 0.397	0.010	0.020	0.010

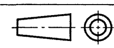
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT161A						~~99-03-29~~ 99-10-04

Flanged ceramic package; 2 mounting holes; 6 leads **SOT171A**

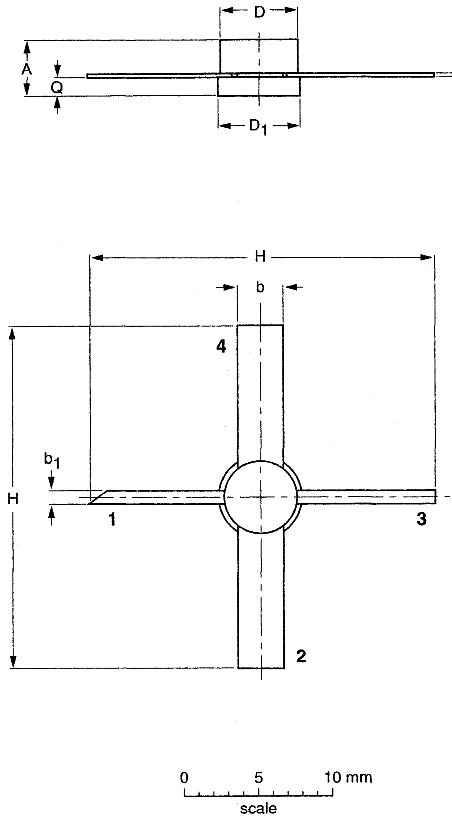


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.81 6.07	3.18 2.92	2.13 1.88	0.16 0.07	9.25 9.04	9.27 9.02	5.95 5.74	5.97 5.72	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	5.97 5.72	0.25	0.51	0.25
inches	0.268 0.239	0.125 0.115	0.084 0.074	0.006 0.003	0.364 0.356	0.365 0.355	0.234 0.226	0.235 0.225	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.235 0.225	0.010	0.020	0.010

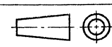
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						99-03-29

Studless ceramic package; 4 leads **SOT172D**

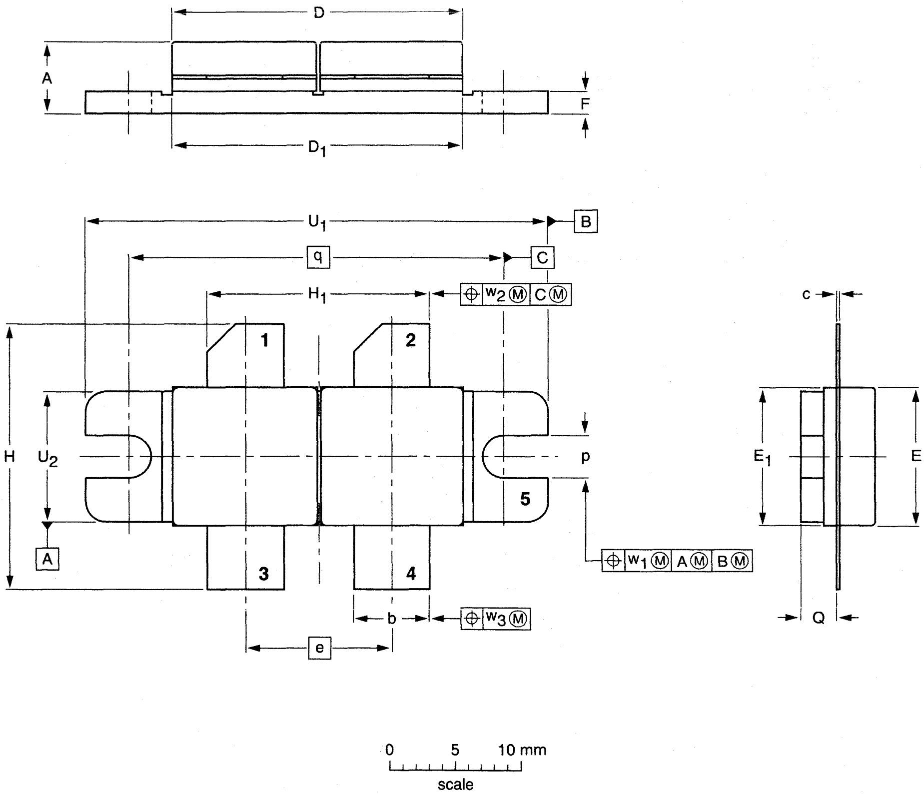


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	H	Q
mm	3.71 2.89	3.31 3.04	0.89 0.63	0.16 0.10	5.20 4.95	5.33 5.08	26.17 24.63	1.15 0.88
inches	0.146 0.114	0.13 0.12	0.035 0.025	0.006 0.004	0.205 0.195	0.210 0.200	1.03 0.97	0.045 0.035

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT172D						97-06-28

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262A1**

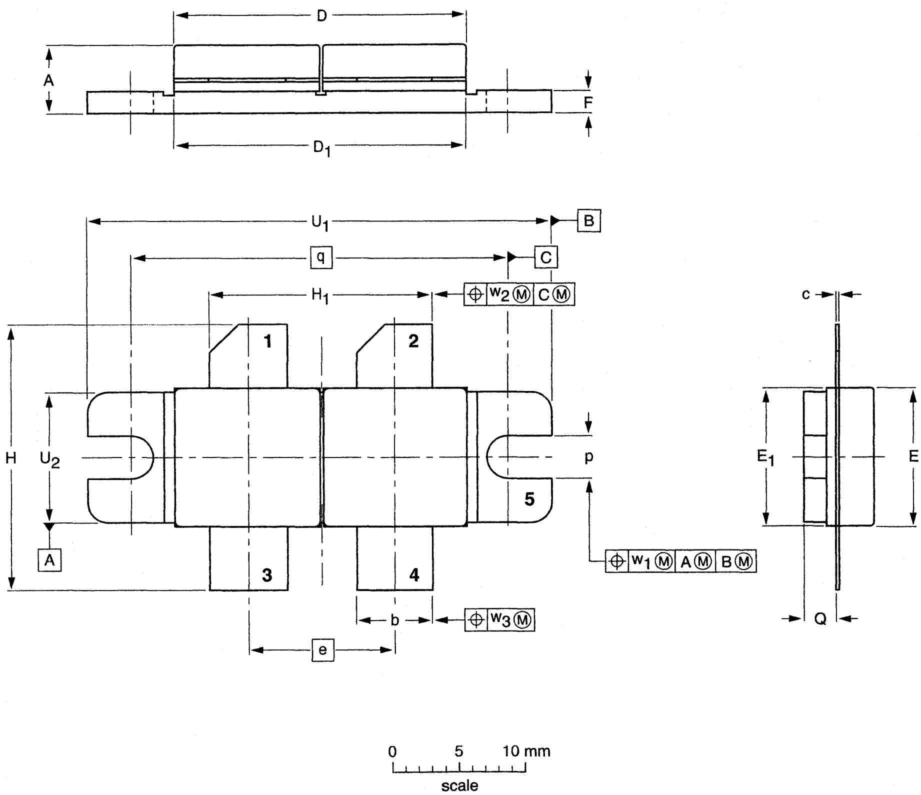


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A1						99-03-29

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262A2**

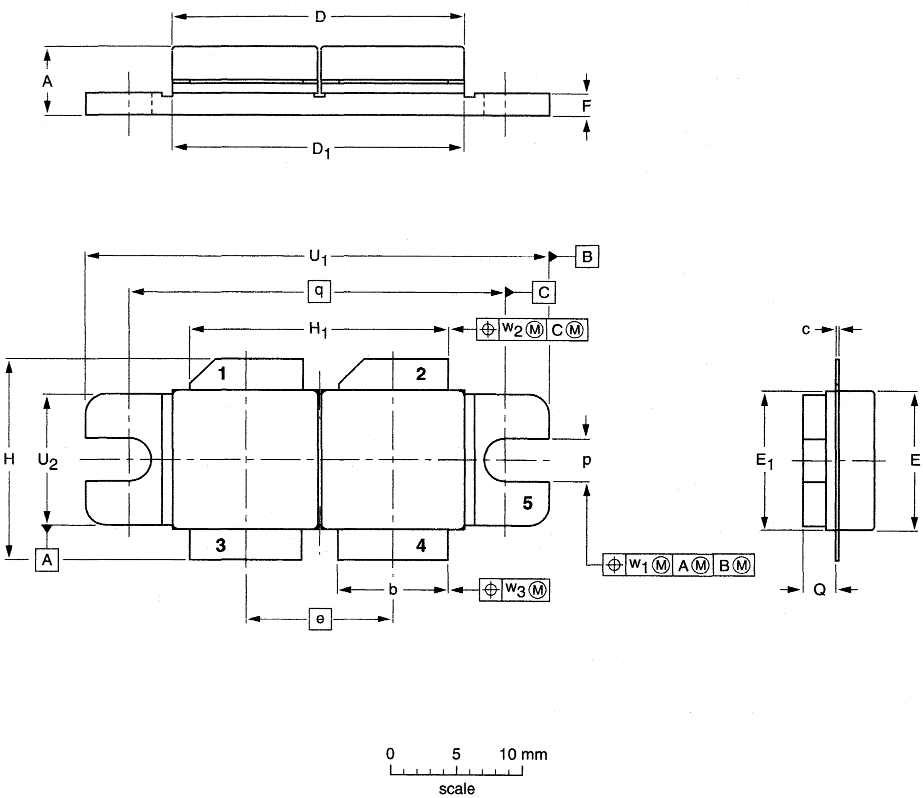


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.39 4.62	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.212 0.182	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A2						99-03-29

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262B**

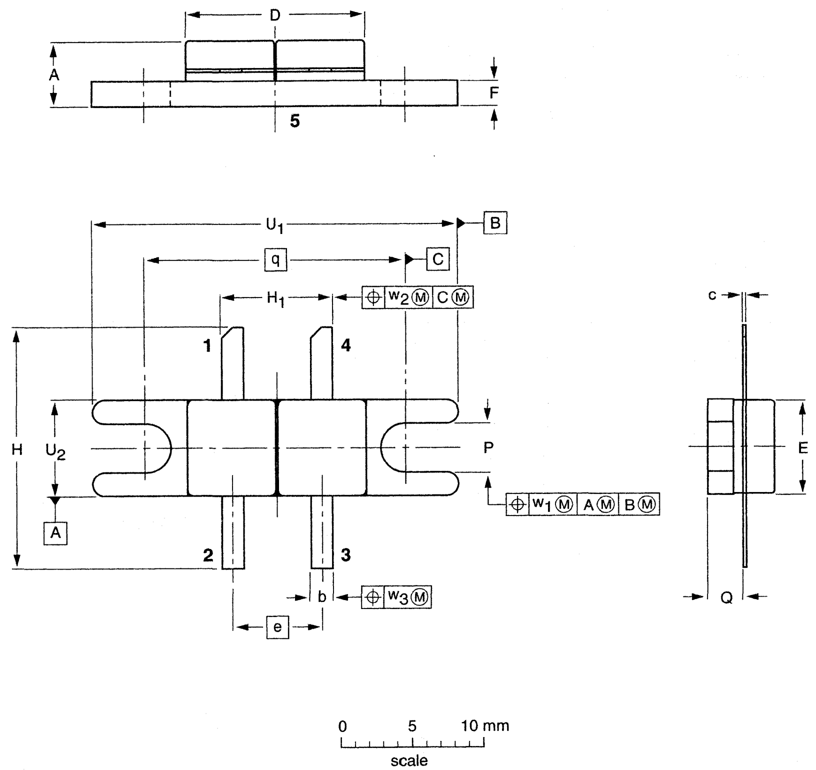


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.39 4.62	8.51 8.25	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	15.49 14.99	19.69 19.17	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.212 0.182	0.335 0.325	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.61 0.59	0.775 0.755	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262B						99-03-29

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT268A**

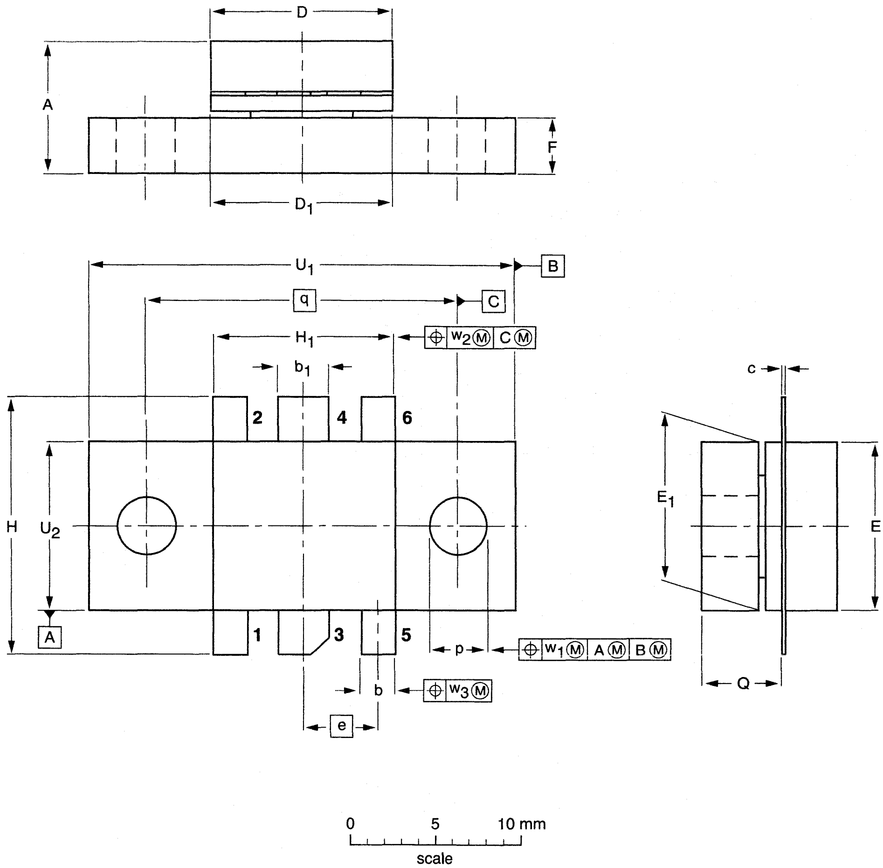


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.91 4.19	1.66 1.39	0.13 0.07	12.96 12.44	6.48 6.22	6.45	2.04 1.77	17.02 16.00	8.23 7.72	3.43 3.17	2.67 2.41	18.42	24.90 24.63	6.61 6.35	0.25	0.51	0.25
inches	0.193 0.165	0.065 0.055	0.005 0.003	0.510 0.490	0.255 0.245	0.254	0.080 0.070	0.670 0.630	0.324 0.304	0.135 0.125	0.105 0.095	0.725	0.980 0.970	0.260 0.250	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT268A						99-03-29

Flanged ceramic package; 2 mounting holes; 6 leads **SOT273A**

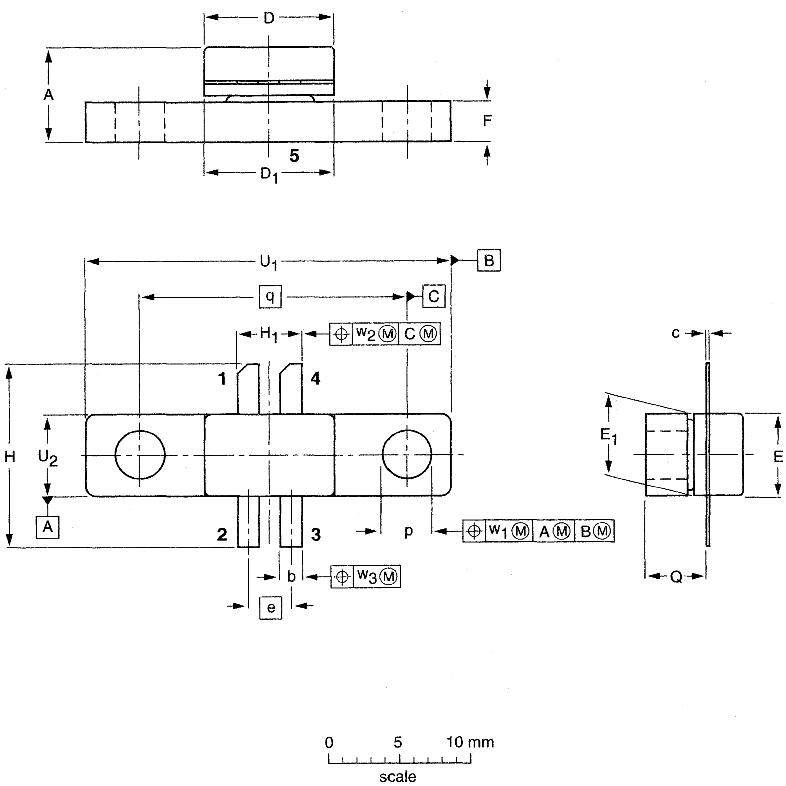


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	7.26 6.45	2.23 1.98	3.16 2.92	0.15 0.10	10.87 10.67	10.92 10.67	10.26 10.06	10.29 10.03	4.35	3.30 3.05	15.75 14.73	10.92 10.67	3.30 3.05	4.34 4.04	18.42	24.89 24.64	10.29 10.03	0.25	0.51	0.25
inches	0.286 0.254	0.088 0.078	0.125 0.115	0.006 0.004	0.428 0.420	0.430 0.420	0.404 0.396	0.405 0.395	0.171	0.130 0.120	0.620 0.580	0.430 0.420	0.130 0.120	0.171 0.159	0.725	0.980 0.970	0.405 0.395	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT273A						~~99-03-29~~ 99-10-04

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT279A**



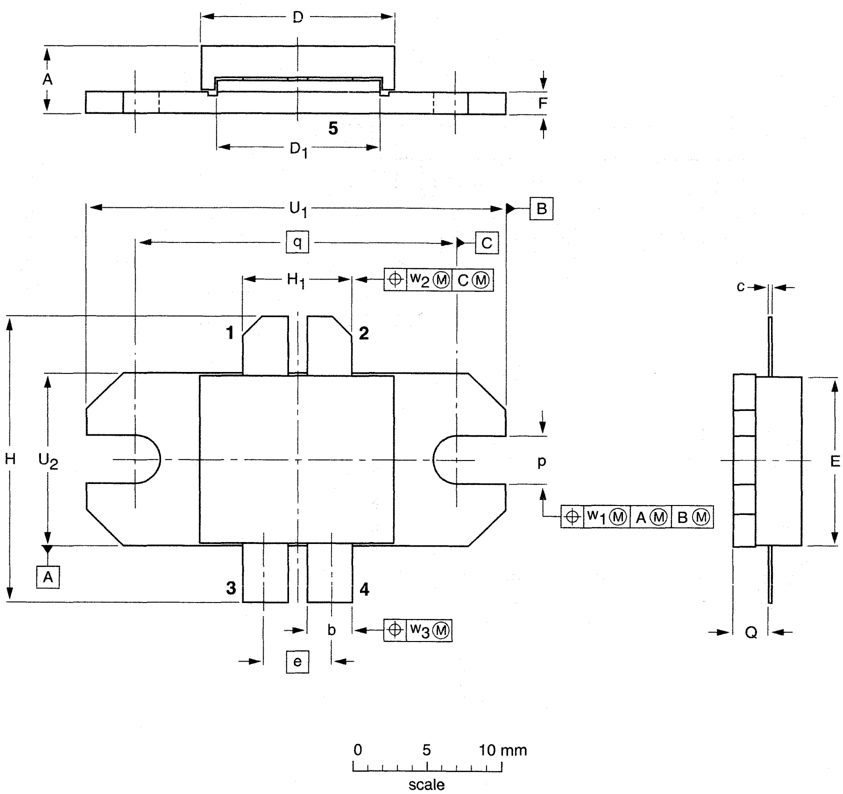
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.84 6.01	1.65 1.40	0.15 0.10	9.25 9.04	9.27 9.02	5.94 5.74	5.97 5.72	3.05	3.05 2.54	12.96 11.94	4.96 4.19	3.48 3.23	4.34 4.04	18.42	24.90 24.64	5.97 5.72	0.25	0.51	0.25
inches	0.269 0.237	0.065 0.055	0.006 0.004	0.364 0.356	0.365 0.355	0.234 0.226	0.235 0.225	0.120	0.120 0.100	0.510 0.470	0.195 0.165	0.137 0.127	0.171 0.159	0.725	0.980 0.970	0.235 0.225	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT279A						99-03-29

Flanged ceramic package; 2 mounting holes; 4 leads

SOT289A



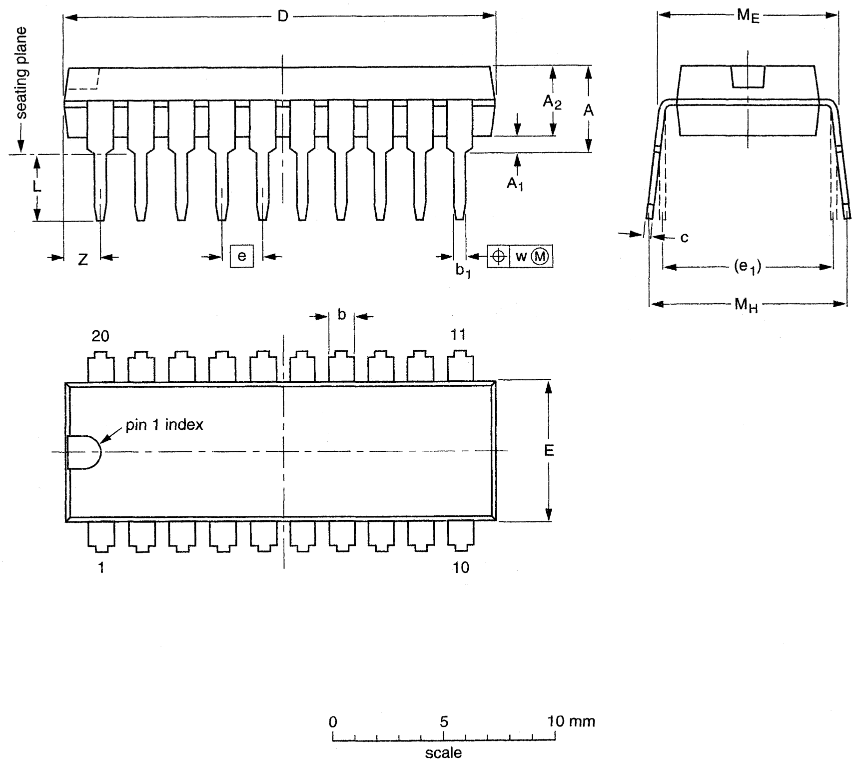
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.65 3.92	3.33 3.07	0.10 0.05	13.10 12.90	11.25 11.00	11.53 11.33	4.60	1.65 1.40	19.81 19.05	4.85 4.34	3.43 3.17	2.31 2.06	21.44	28.07 27.81	11.81 11.56	0.51	1.02	0.25
inches	0.183 0.154	0.131 0.121	0.004 0.002	0.516 0.508	0.443 0.433	0.454 0.446	0.181	0.065 0.055	0.780 0.750	0.191 0.171	0.135 0.125	0.091 0.081	0.844	1.105 1.095	0.465 0.455	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT289A						99-03-29

SDIP20: plastic shrink dual in-line package; 20 leads (300 mil)

SOT325-1



DIMENSIONS (mm are the original dimensions)

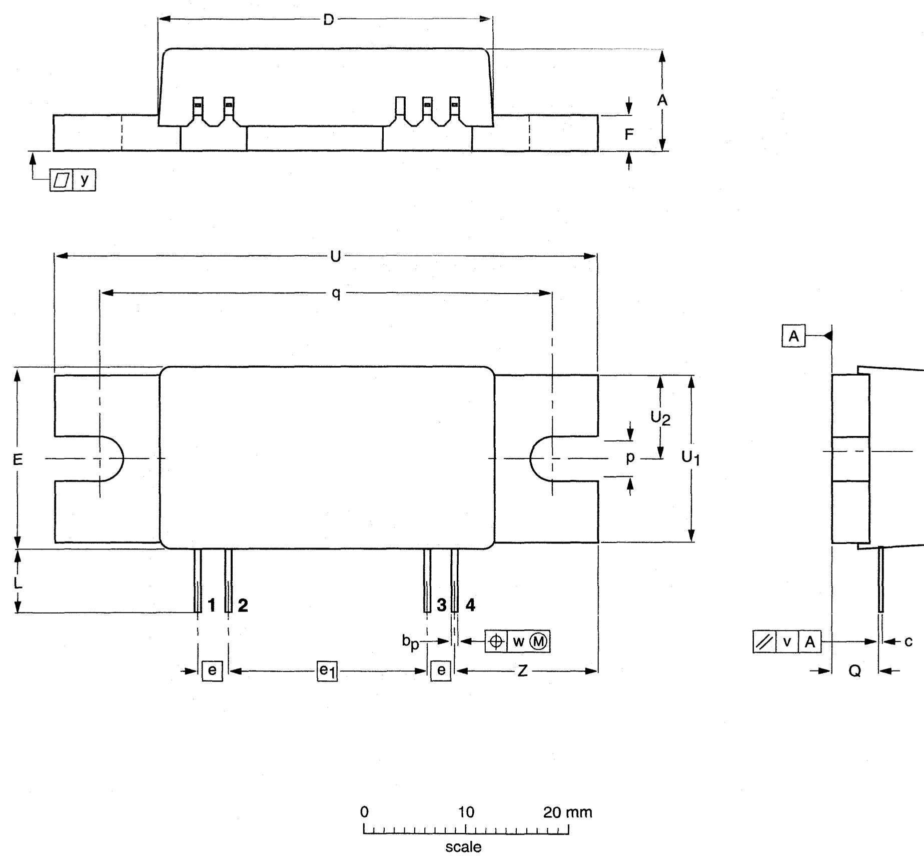
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.2	0.51	3.2	1.3 1.0	0.53 0.38	0.32 0.20	19.50 18.55	6.48 6.14	1.778	7.62	3.2 2.8	8.25 7.80	10.0 8.3	0.18	1.9

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT325-1						~~92-10-13~~ 95-02-04

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads **SOT365A**

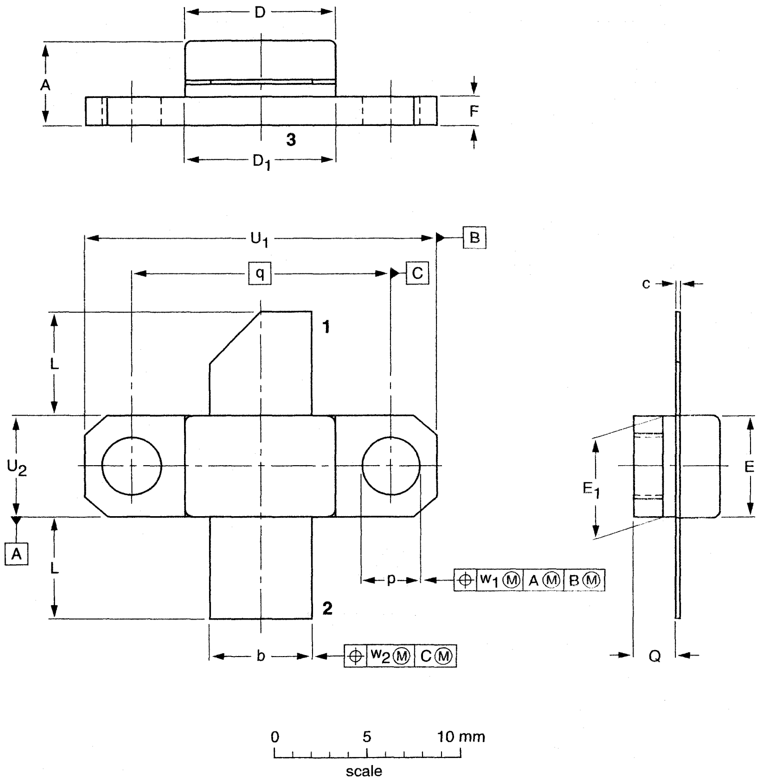


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	F	L	p	Q	q	U	U_1	U_2	v	w	y	Z
mm	9.5 9.0	0.56 0.46	0.3 0.2	30.1 29.9	18.6 18.4	2.54	17.78	3.25 3.15	6.5 6.1	4.1 3.9	4.0 3.8	40.74 40.54	48.0 48.4	15.4 15.2	7.75 7.55	0.3	0.25	0.1	12.8 12.6

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT365A						99-02-06

Flanged ceramic package; 2 mounting holes; 2 leads **SOT390A**

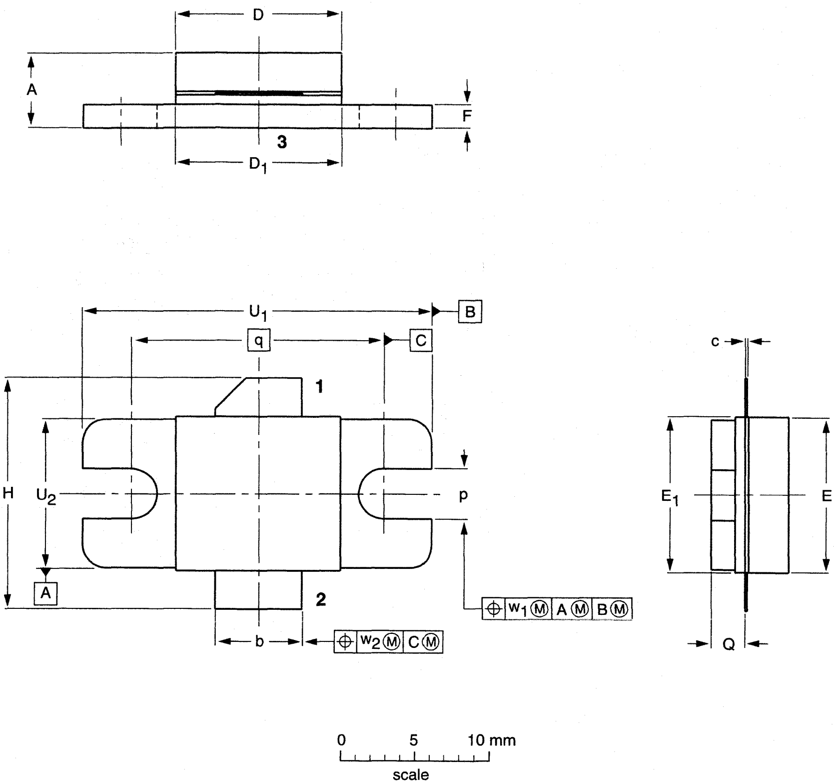


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	L	p	Q	q	U_1	U_2	w_1	w_2
mm	5.03 4.22	5.72 5.46	0.16 0.10	8.18 8.08	8.26 8.00	6.40 6.30	6.43 6.17	1.66 1.39	6.10 5.33	3.43 3.17	2.32 2.00	14.22	19.03 18.77	6.43 6.17	0.25	0.51
inches	0.198 0.166	0.225 0.215	0.006 0.004	0.322 0.318	0.325 0.315	0.252 0.248	0.253 0.243	0.065 0.055	0.24 0.21	0.135 0.125	0.091 0.079	0.560	0.749 0.739	0.253 0.243	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT390A						99-03-29

Flanged ceramic package; 2 mounting holes; 2 leads **SOT391A**



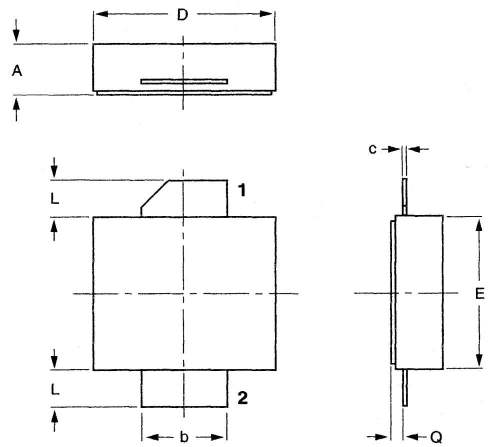
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.21 4.45	5.84 5.59	0.15 0.10	10.87 10.67	10.92 10.67	10.26 10.06	10.29 10.03	1.65 1.40	15.75 14.73	3.43 3.18	2.29 2.03	20.32	22.99 22.73	9.91 9.65	0.25	0.51
inches	0.205 0.175	0.230 0.220	0.006 0.004	0.428 0.420	0.430 0.420	0.404 0.396	0.405 0.395	0.065 0.055	0.620 0.580	0.135 0.125	0.090 0.080	0.800	0.905 0.895	0.390 0.380	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT391A						~~97-05-29~~ 99-12-08

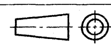
Flangeless ceramic package; 2 leads

SOT391B



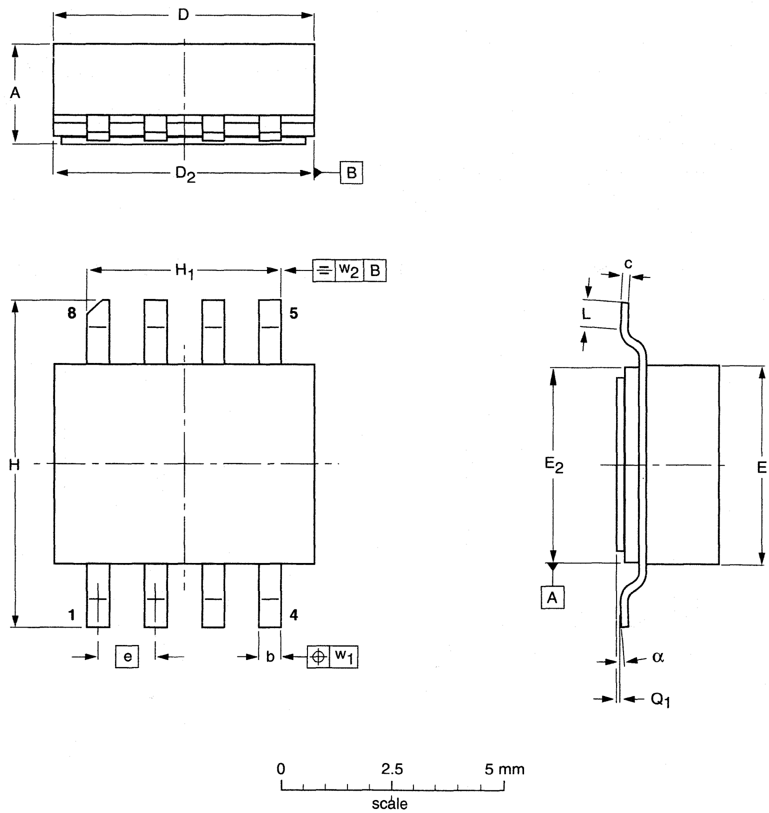
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	L	Q
mm	4.09 3.02	5.85 5.58	0.16 0.10	11.54 10.51	10.93 9.90	2.79 2.29	1.02 0.76

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT391B						97-05-29

Ceramic surface mounted package; 8 leads

SOT409A



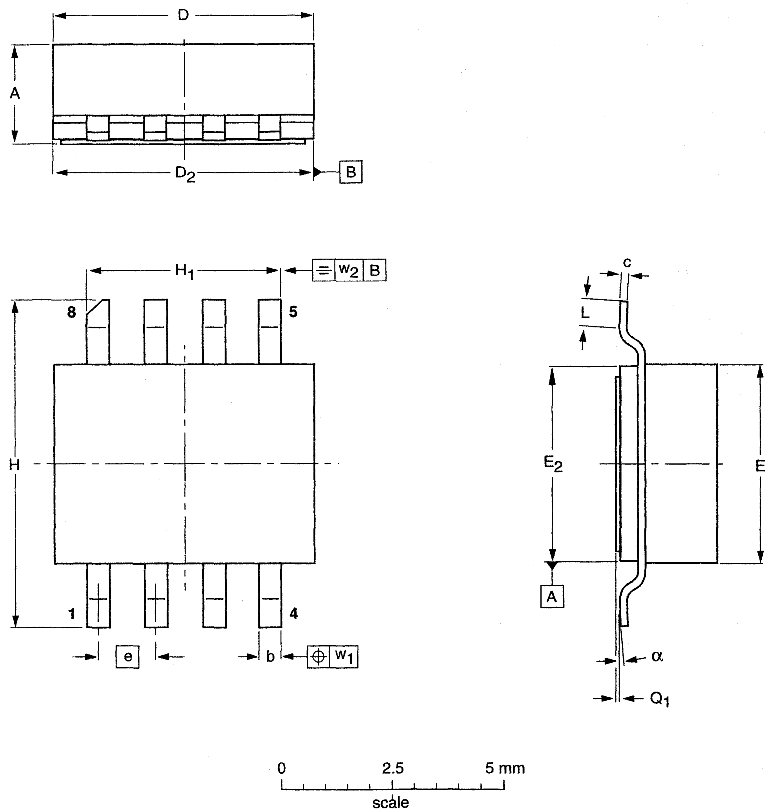
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_2	E	E_2	e	H	H_1	L	Q_1	w_1	w_2	α
mm	2.36 2.06	0.58 0.43	0.23 0.18	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	1.02 0.51	0.10 0.00	0.25	0.25	7° 0°
inches	0.093 0.081	0.023 0.017	0.009 0.007	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.040 0.020	0.004 0.000	0.010	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409A						98-01-27

Ceramic surface mounted package; 8 leads

SOT409B

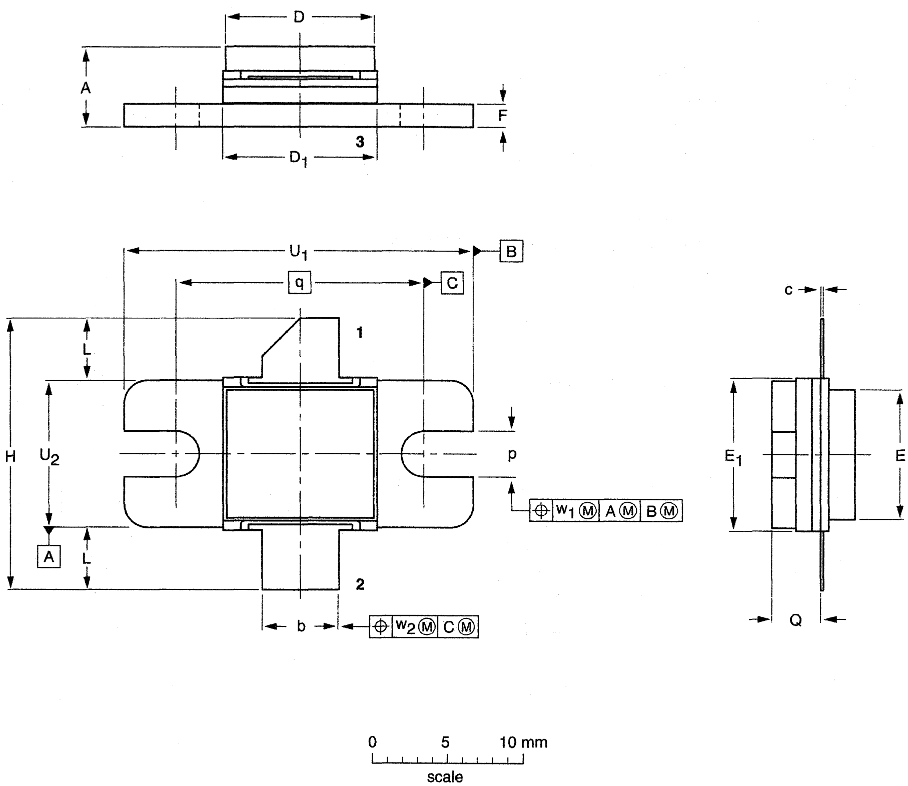


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_2	E	E_2	e	H	H_1	L	Q_1	w_1	w_2	α
mm	2.36 2.06	0.58 0.43	0.15 0.10	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	0.84 0.69	0.10 0.00	0.25	0.25	2° 0°
inches	0.093 0.081	0.023 0.017	0.006 0.004	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.033 0.027	0.004 0.000	0.010	0.010	2° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409B						98-01-27

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT422A**

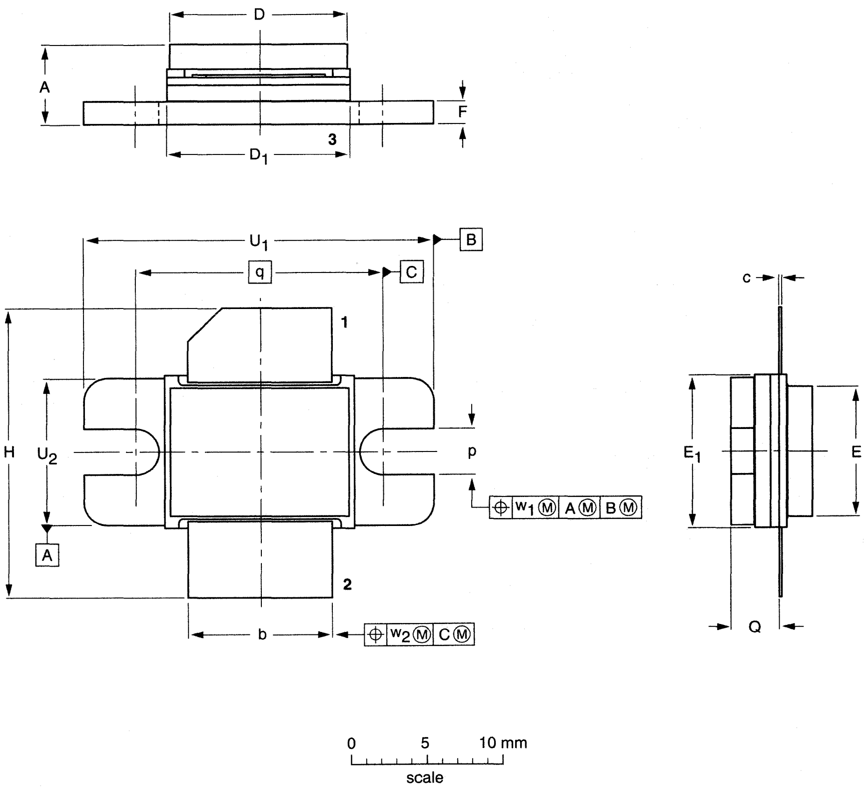


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	5.72 4.83	5.21 4.95	0.13 0.08	9.93 9.68	10.29 10.03	8.76 8.51	10.29 10.03	1.58 1.47	19.18 17.65	4.52 3.74	3.43 3.18	3.35 2.92	16.51	22.99 22.73	9.91 9.65	0.25	0.76
inches	0.225 0.190	0.205 0.195	0.005 0.003	0.391 0.381	0.405 0.395	0.345 0.335	0.405 0.395	0.062 0.058	0.755 0.695	0.178 0.147	0.135 0.125	0.132 0.115	0.65	0.905 0.895	0.390 0.380	0.01	0.03

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT422A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT423A**



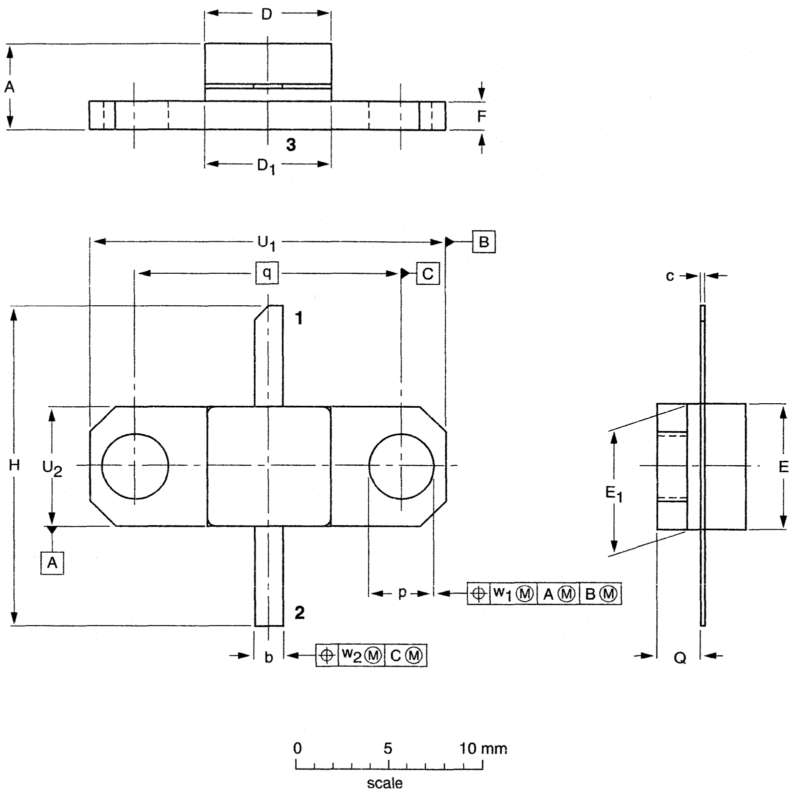
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.72 4.90	9.53 9.27	0.10 0.05	12.09 11.71	12.83 12.57	8.84 8.56	10.29 10.03	1.58 1.47	19.81 18.29	3.43 3.18	3.35 2.95	16.51	22.99 22.73	9.91 9.65	0.25	0.76
inches	0.225 0.193	0.375 0.365	0.004 0.002	0.476 0.461	0.505 0.495	0.348 0.337	0.405 0.395	0.062 0.058	0.78 0.72	0.135 0.125	0.132 0.116	0.65	0.905 0.895	0.390 0.380	0.01	0.03

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT423A						99-03-29

Flanged ceramic package; 2 mounting holes; 2 leads

SOT437A

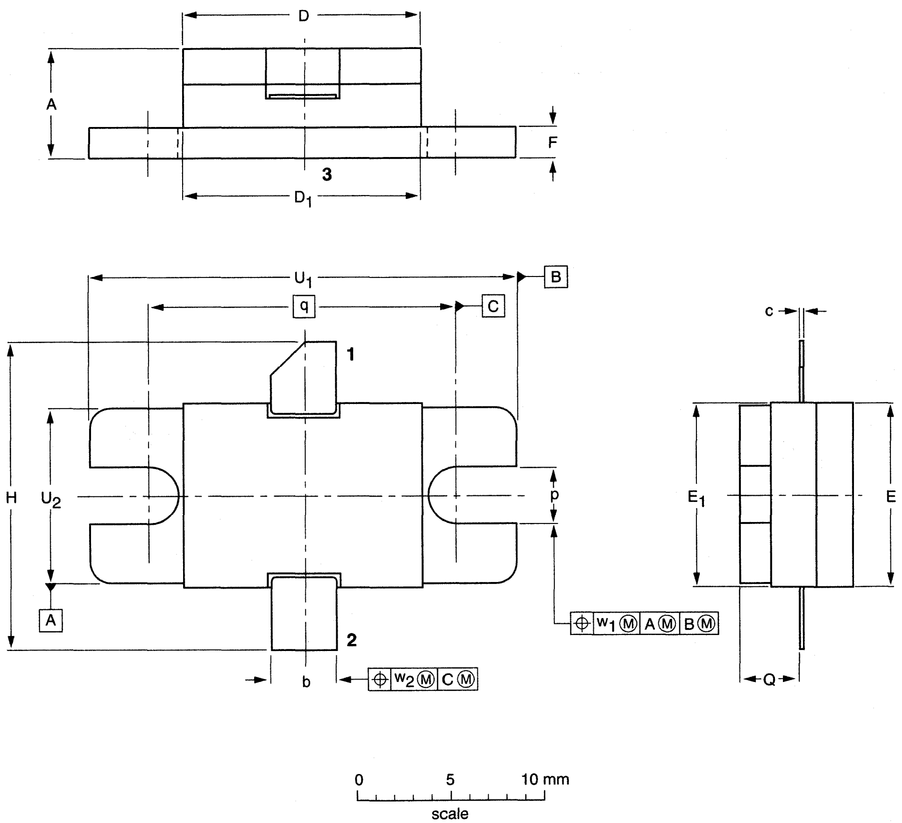


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.98 4.32	1.66 1.40	0.13 0.08	6.48 6.22	6.48 6.22	6.48 6.22	6.48 6.22	1.65 1.40	17.02 16.00	3.43 3.18	2.29 2.03	14.22	19.02 18.77	6.48 6.22	0.25	0.51
inches	0.196 0.170	0.065 0.055	0.005 0.003	0.255 0.245	0.255 0.245	0.255 0.245	0.255 0.245	0.065 0.055	0.67 0.63	0.135 0.125	0.90 0.80	0.560	0.749 0.739	0.255 0.245	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT437A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT439A**



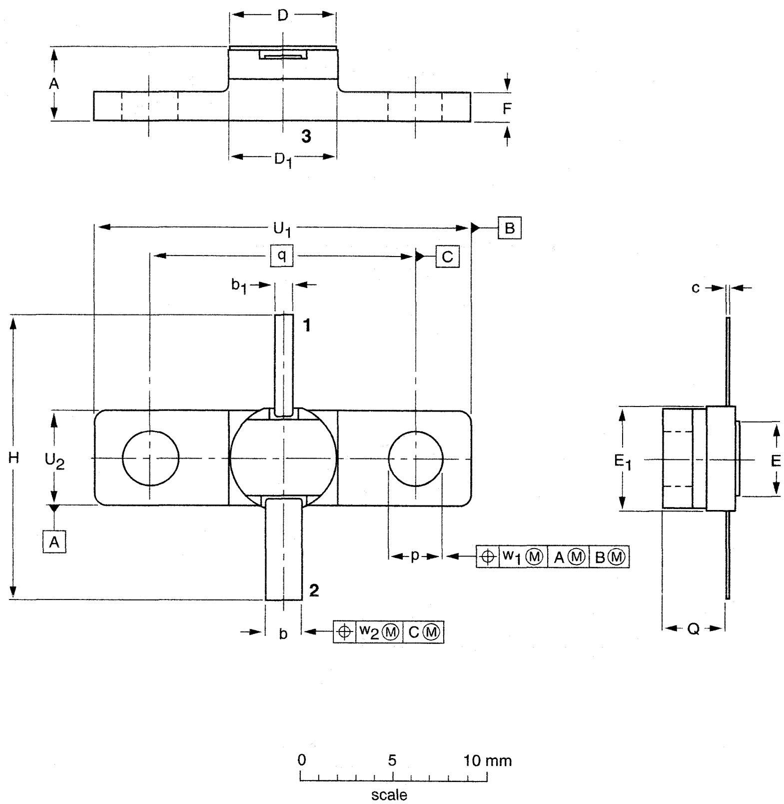
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	6.05 5.23	3.69 3.42	0.13 0.05	12.85 12.55	12.83 12.57	10.31 10.01	10.26 10.06	1.58 1.47	17.27 15.75	3.43 3.17	3.33 2.97	16.51	22.94 22.73	9.91 9.65	0.25	0.79
inches	0.238 0.206	0.145 0.135	0.005 0.002	0.506 0.494	0.505 0.495	0.406 0.394	0.404 0.396	0.62 0.58	0.680 0.620	0.135 0.125	0.131 0.117	0.650	0.905 0.895	0.390 0.380	0.010	0.031

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT439A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT440A



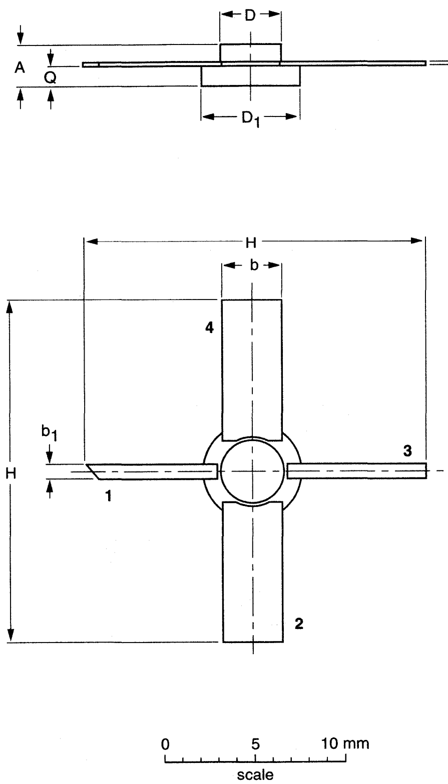
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.25 3.32	2.16 1.90	1.15 0.89	0.14 0.09	5.70 5.50	5.69 5.39	3.90 3.70	5.31 5.01	1.65 1.39	16.24 14.24	3.18 2.92	3.48 2.93	14.22	20.45 20.19	5.18 4.98	0.25	0.51
inches	0.167 0.131	0.085 0.075	0.045 0.035	0.006 0.004	0.224 0.217	0.224 0.212	0.154 0.146	0.209 0.197	0.065 0.055	0.639 0.560	0.125 0.115	0.137 0.115	0.600	0.805 0.795	0.204 0.196	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT440A						99-03-29

Studless ceramic package; 4 leads

SOT441A

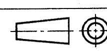


DIMENSIONS (mm are the original dimensions)

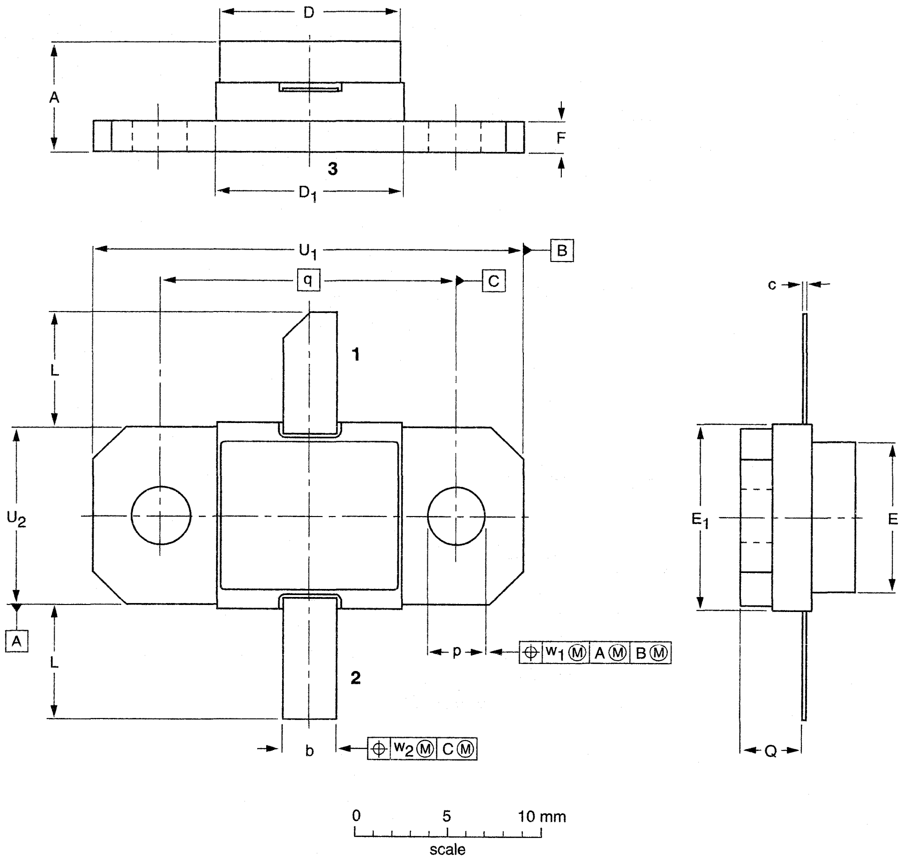
UNIT	A	b	b_1	c	D	D_1	H	Q
mm	2.48 1.60	3.23 3.13	0.81 0.71	0.16 0.10	3.38 3.08	5.34 5.08	19 17	1.15 0.89
inches	0.098 0.063	0.127 0.123	0.032 0.028	0.006 0.004	0.133 0.121	0.210 0.200	0.75 0.67	0.045 0.035

Note

1. This device contains bare beryllium oxide, the dust of witch is toxic.

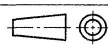
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT441A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT443A**

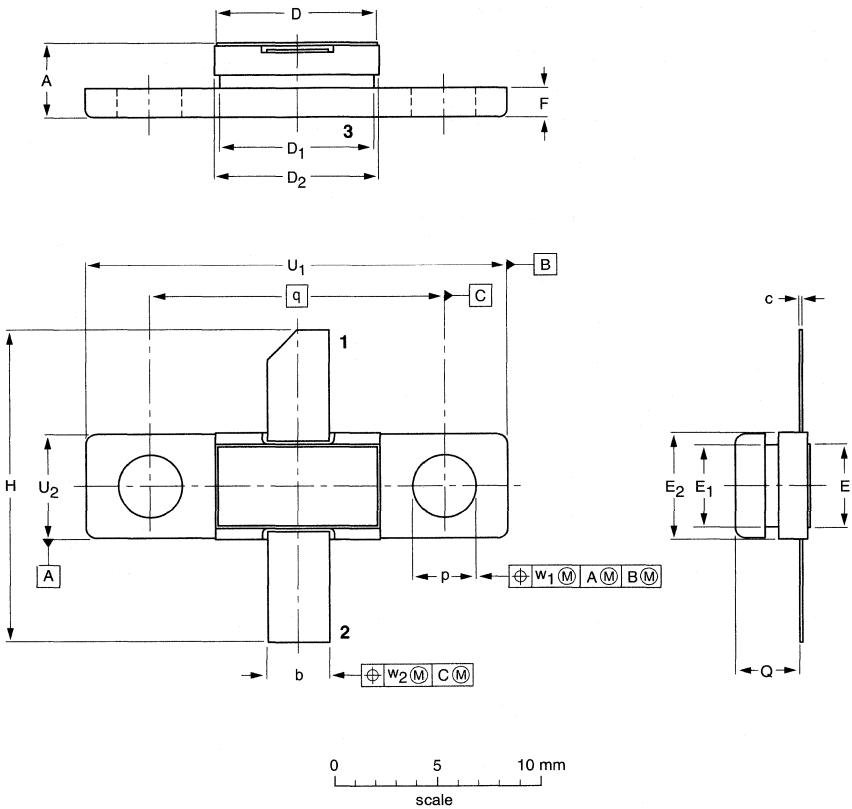


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	L	p	Q	q	U_1	U_2	w_1	w_2
mm	6.32 4.90	3.20 2.90	0.15 0.09	10.00 9.70	10.21 9.91	8.15 7.85	10.21 9.91	1.60 1.40	6.25 5.75	3.40 3.20	3.66 2.84	16.50	23.10 22.70	9.90 9.70	0.41	0.94
inches	0.249 0.193	0.126 0.114	0.006 0.004	0.394 0.382	0.402 0.390	0.321 0.309	0.402 0.390	0.063 0.055	0.246 0.226	0.134 0.126	0.144 0.112	0.650	0.909 0.894	0.390 0.382	0.016	0.037

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT443A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT445A**

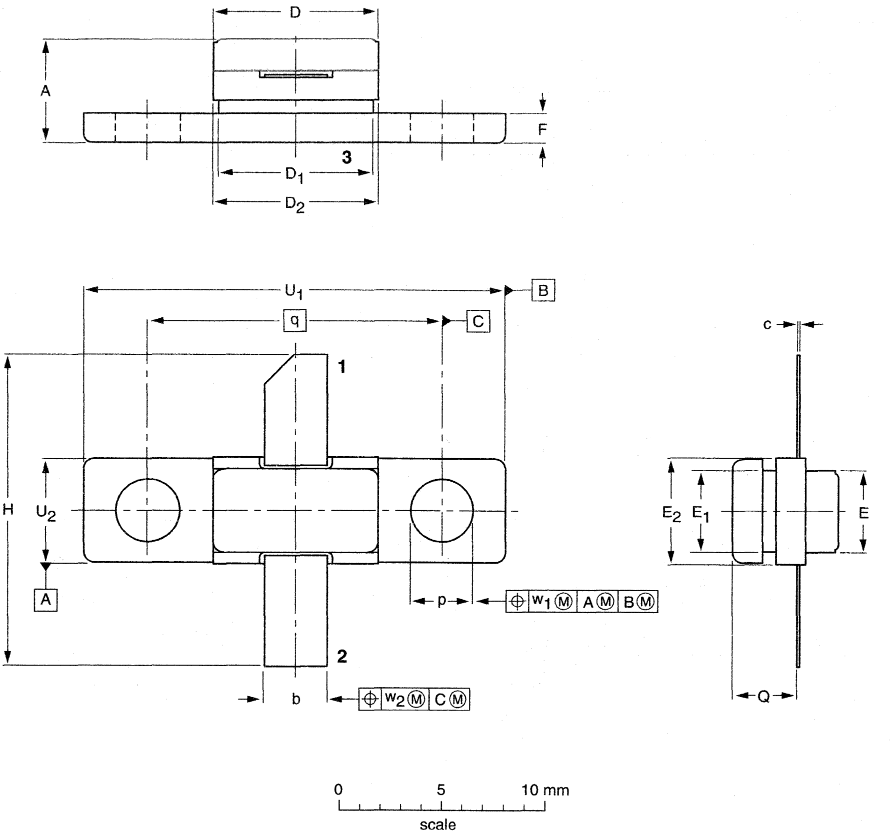


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.01 3.36	3.15 2.95	0.15 0.09	7.9 7.7	7.65 7.35	8.15 7.85	4.1 3.9	4.25 3.95	5.31 5.01	1.67 1.37	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.30	0.51
inches	0.158 0.132	0.125 0.115	0.006 0.003	0.312 0.303	0.302 0.289	0.321 0.309	0.162 0.153	0.168 0.155	0.210 0.197	0.066 0.054	0.624 0.576	0.132 0.120	0.132 0.119	0.56	0.806 0.794	0.204 0.196	0.012	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT445A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT445C**

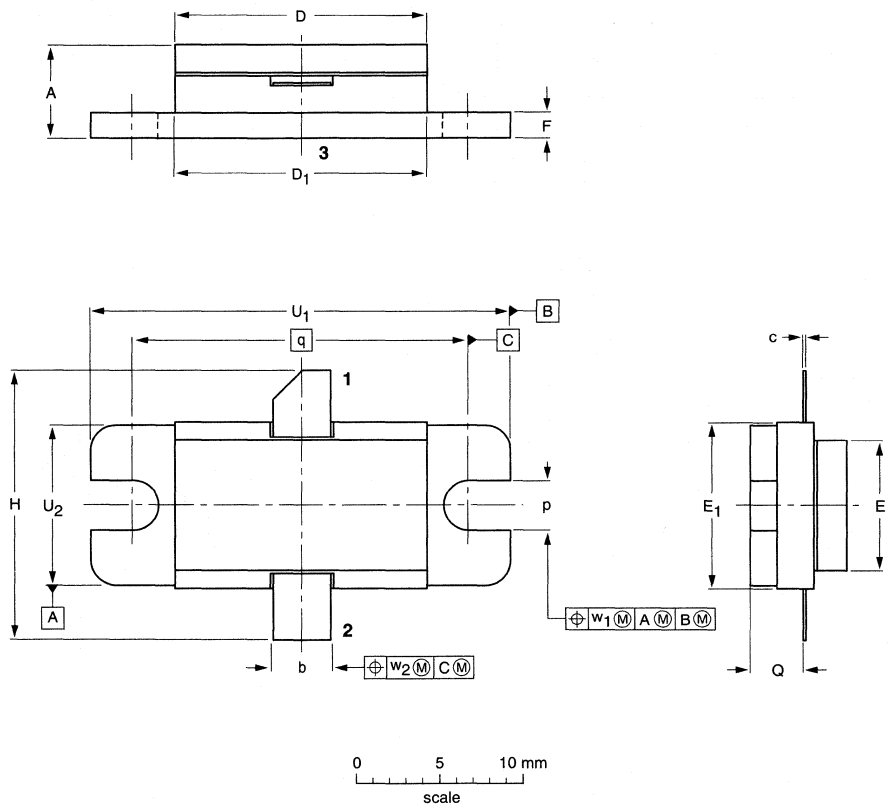


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.57 4.70	3.15 2.95	0.15 0.09	8.13 7.87	7.65 7.35	8.15 7.85	4.20 3.93	4.25 3.95	5.31 5.01	1.67 1.37	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.31	0.51
inches	0.220 0.185	0.125 0.115	0.006 0.003	0.32 0.31	0.302 0.289	0.321 0.309	0.165 0.155	0.168 0.155	0.210 0.197	0.066 0.054	0.624 0.576	0.132 0.120	0.132 0.119	0.56	0.806 0.794	0.204 0.196	0.012	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT445C						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT448A**



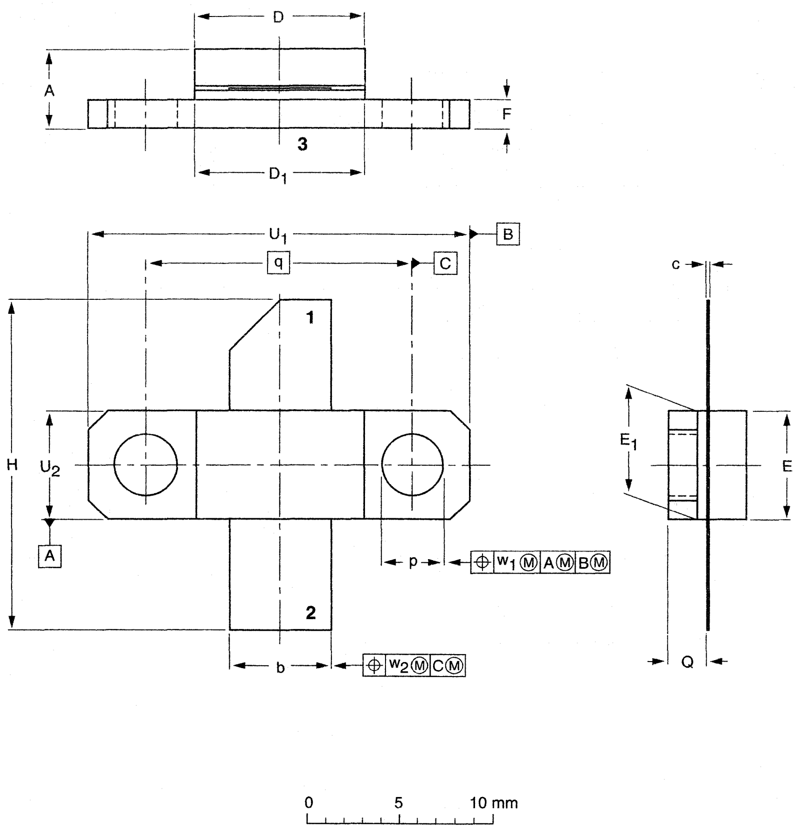
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	6.17 5.31	3.69 3.42	0.13 0.05	15.68 15.16	15.42 15.16	8.08 7.82	10.29 10.03	1.63 1.52	17.02 16.00	3.31 2.79	3.42 3.00	20.32	25.53 25.27	9.91 9.65	0.25	0.79
inches	0.243 0.209	0.145 0.135	0.005 0.002	0.605 0.599	0.607 0.597	0.316 0.310	0.405 0.395	0.064 0.060	0.67 0.63	0.065 0.055	0.134 0.118	0.800	1.005 0.995	0.390 0.380	0.010	0.031

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT448A						99-03-29

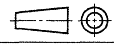
Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C

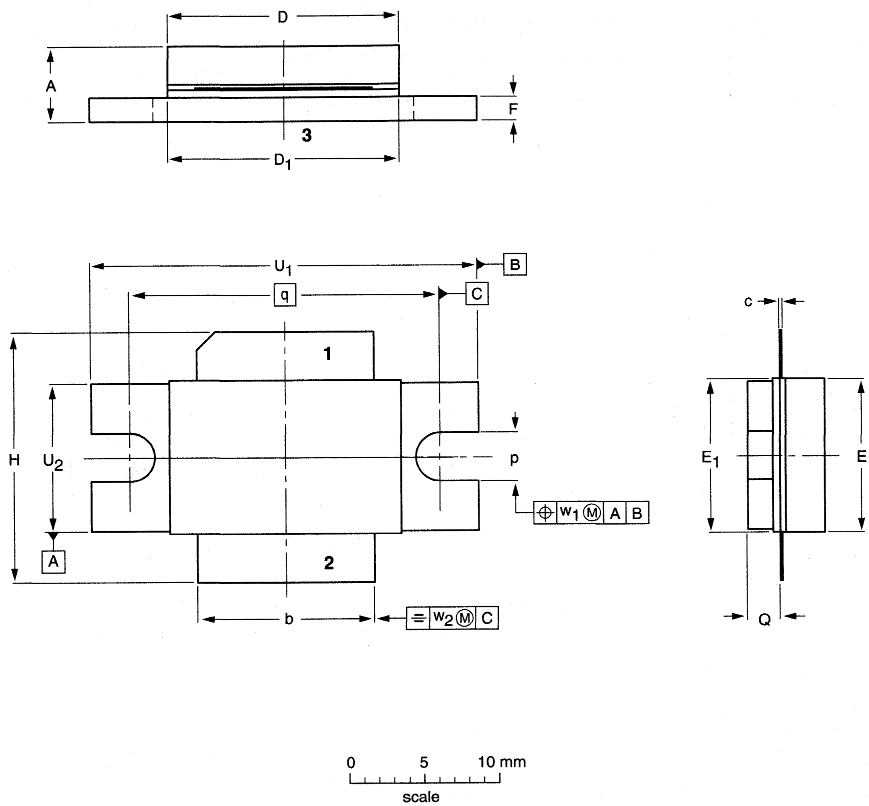


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-06~~ 99-12-28

Flanged ceramic (AIN) package; 2 mounting holes; 2 leads **SOT468A**

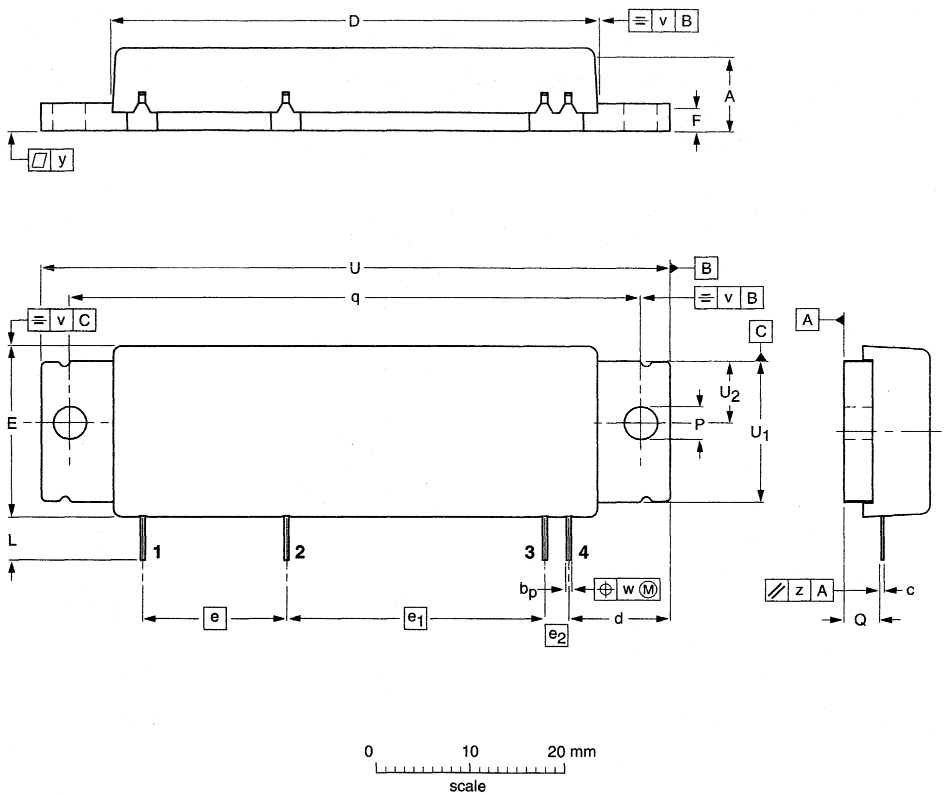


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.23 4.62	11.81 11.58	0.15 0.10	15.39 15,09	15.37 15,11	10.26 10.06	10.29 10.03	1.65 1.60	16.74 16.48	3.30 3.05	2.21 2.06	20.32	25.53 25.27	9.91 9.65	0.254	0.508
inches	0.206 0.182	0.465 0.455	0.006 0.004	0.606 0.594	0.605 0.595	0.404 0.396	0.405 0.395	0.065 0.063	0.659 0.649	0.130 0.120	0.087 0.081	0.800	1.005 0.995	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT468A						97-12-24

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads **SOT501A**

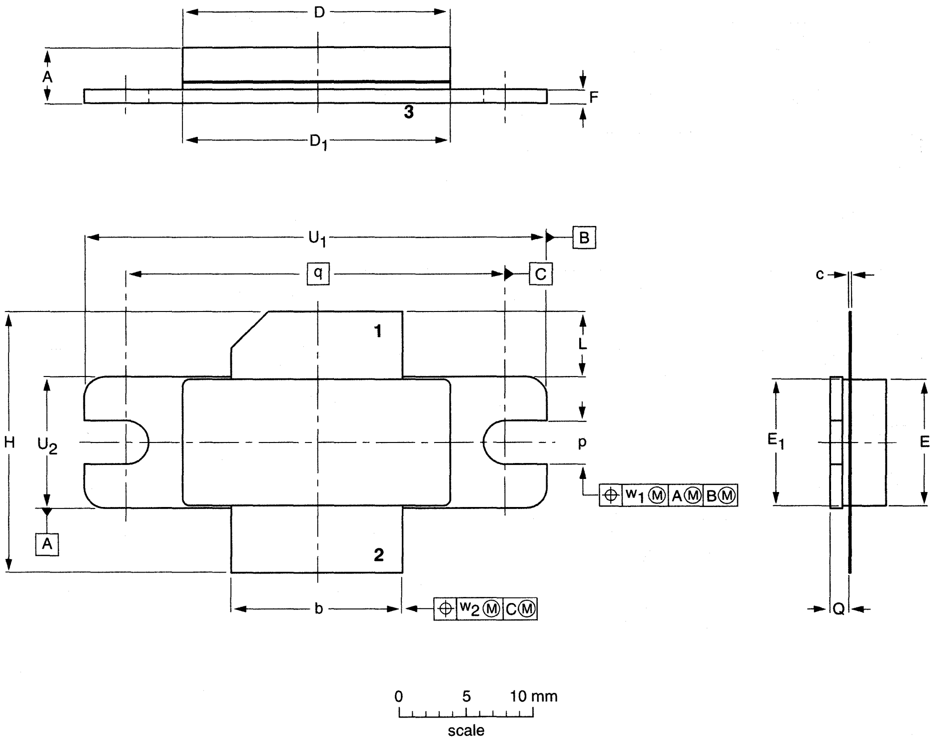


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	d	E	e	e_1	e_2	F	L	P	Q	q	U	U_1	U_2	v	w	y	z
mm	9.4 8.9	0.56 0.46	0.3 0.2	52.1 51.7	10.9 10.5	18.7 18.3	15.24	27.94	2.54	3.1 2.9	6.5 6.1	3.6 3.4	4.1 3.7	61.2 61.0	67.4 67.0	15.5 15.1	6.9 6.5	0.2	0.25	0.1	0.3

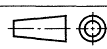
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT501A						98-10-28

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**

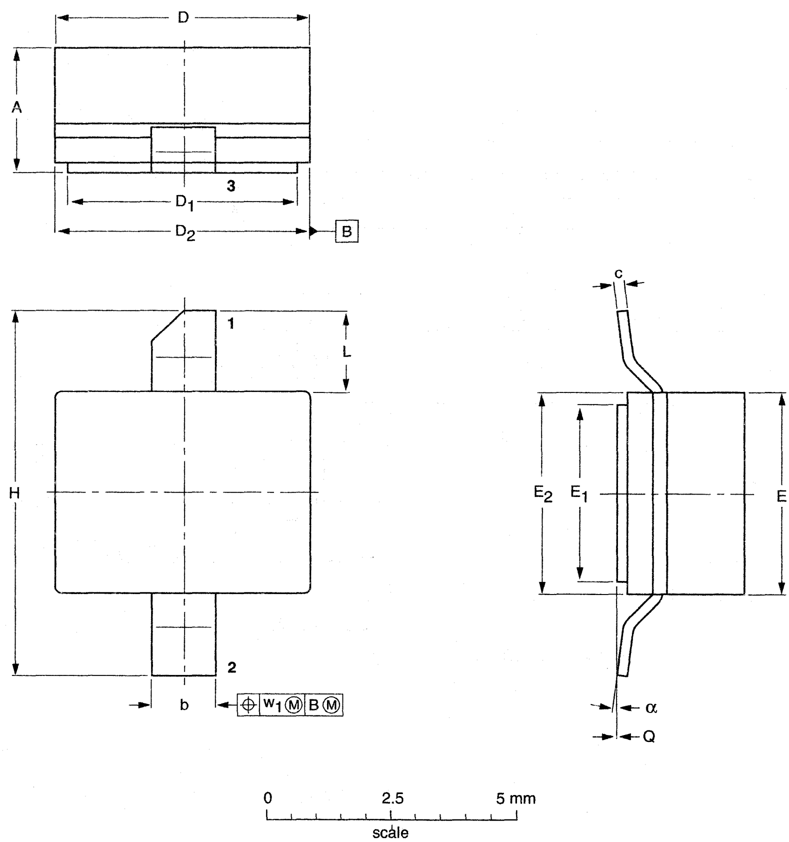


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						~~99-10-13~~ 99-12-28

Ceramic surface mounted package; 2 leads **SOT538A**



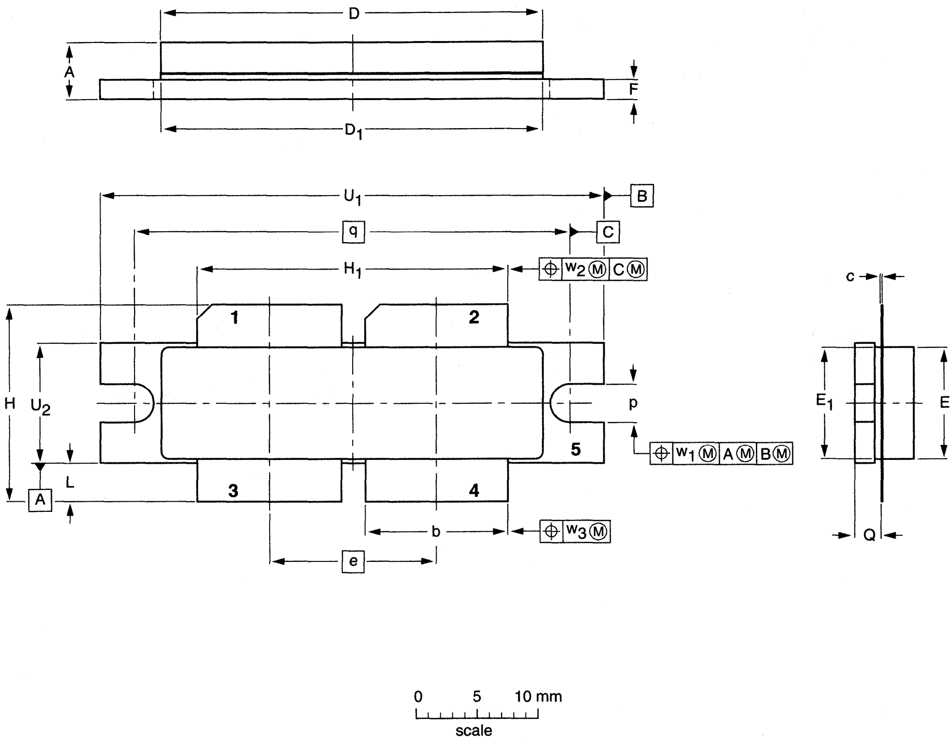
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	H	L	Q	w_1	α
mm	2.95 2.29	1.35 1.19	0.23 0.18	5.16 5.00	4.65 4.50	5.41 5.00	4.14 3.99	3.63 3.48	4.14 3.99	7.49 7.24	2.03 1.27	0.10 0.00	0.25	7° 0°
inches	0.116 0.090	0.053 0.047	0.009 0.007	0.203 0.197	0.183 0.177	0.213 0.197	0.163 0.157	0.143 0.137	0.163 0.157	0.295 0.285	0.080 0.050	0.004 0.000	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT538A						~~99-03-30~~ 00-03-03

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads

SOT539A

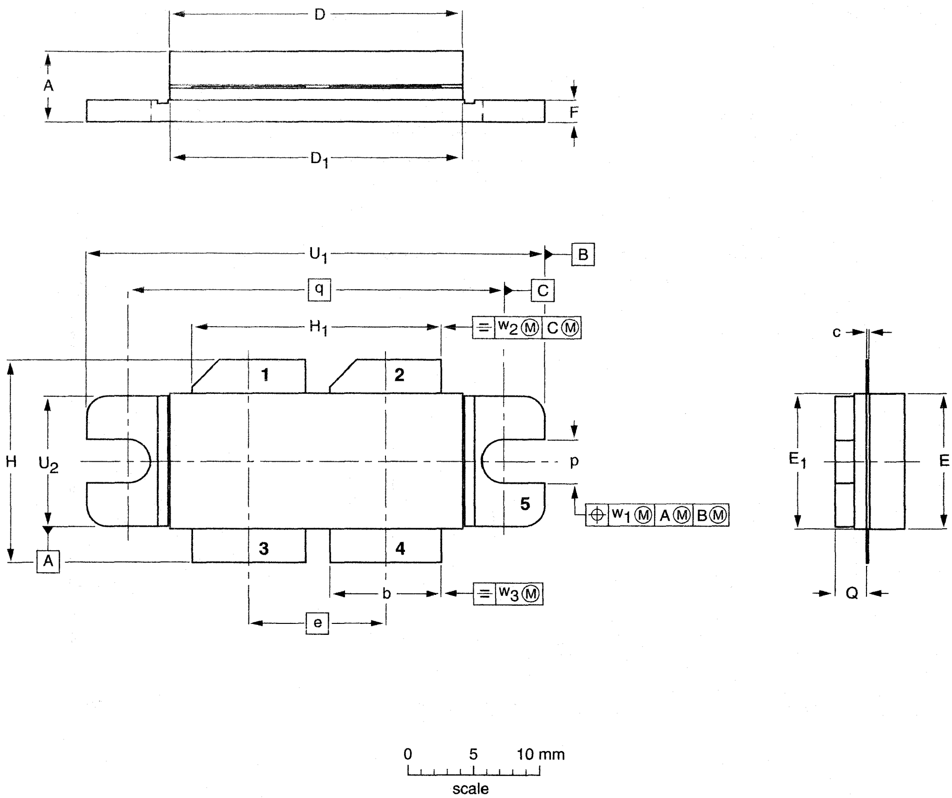


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.33 3.96	11.81 11.56	0.15 0.08	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.73 2.72	3.30 3.05	2.31 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.210 0.156	0.465 0.455	0.006 0.003	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.147 0.107	0.130 0.120	0.091 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

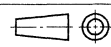
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~99-12-28~~ 00-03-03

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads **SOT540A**

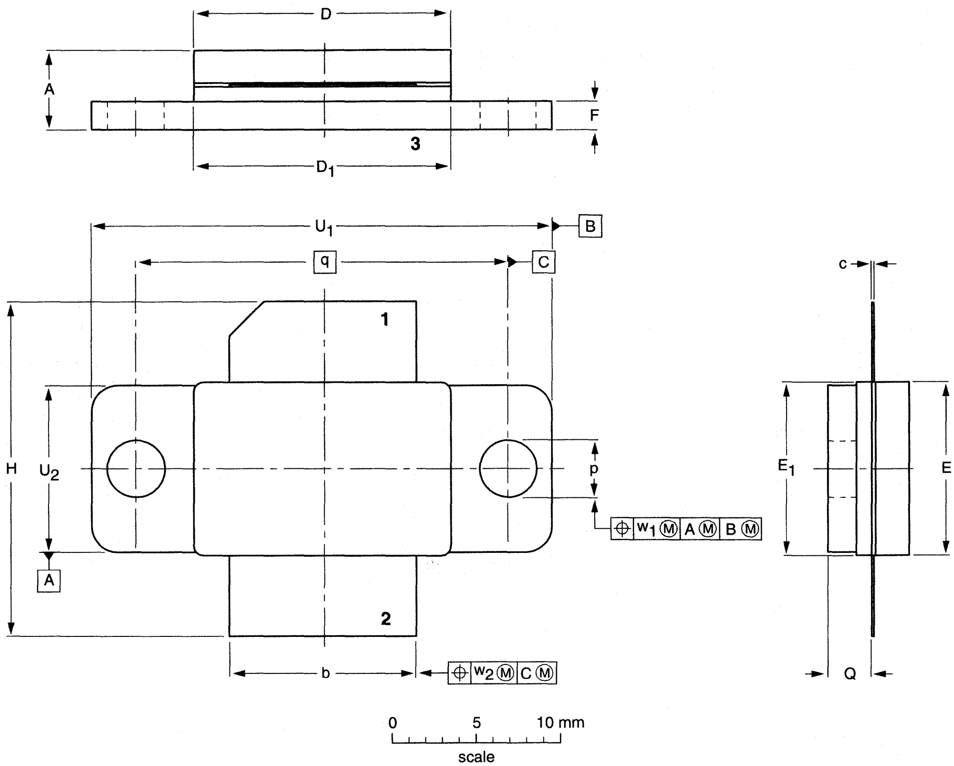


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	8.51 8.26	0.15 0.10	22.05 21.64	22.05 21.64	10.21	10.26 10.06	10.31 10.01	1.78 1.52	15.75 14.73	18.72 18.47	3.38 3.12	2.72 2.46	27.94	34.16 33.91	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.335 0.325	0.006 0.004	0.868 0.852	0.868 0.852	0.402	0.404 0.396	0.406 0.394	0.070 0.060	0.620 0.580	0.737 0.727	0.133 0.123	0.107 0.097	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT540A						~~99-08-27~~ 99-12-28

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT541A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.74 4.60	11.05 10.80	0.18 0.10	15.39 15.09	15.39 15.09	10.26 10.06	10.29 10.03	1.78 1.52	20.83 19.81	3.43 3.18	2.69 2.44	22.10	27.31 27.05	9.91 9.65	0.25	0.51
inches	0.226 0.181	0.435 0.425	0.007 0.004	0.606 0.594	0.606 0.594	0.404 0.396	0.405 0.395	0.070 0.060	0.820 0.780	0.135 0.125	0.106 0.096	0.87	1.075 1.065	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT541A						~~00-01-13~~ 00-03-03

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Data handbook system

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